

**Artificial
Intelligence**

5G

Advanced Engineered substrates for RF applications: from silicon to compound materials

Christophe Maleville - November 15th, 2022

**Energy
Efficiency**

Imec Technology Forum, *Beyond 5G, Semicon Europa*

Outline

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Introduction

2

Engineered substrates for RRFE applications

3

Getting More G from Engineered Substrate

4

Takeaways & Conclusions



Advancing 5G to fulfill its full promise

Enhanced mobile experiences, new capabilities,
and expansion to diverse verticals



Continued evolution towards 6G



Industry 4.0



Boundless XR



Wide-area 5G



Mobile mmWave



5G V2X Sidelink



Green networks

Application of Engineered substrates

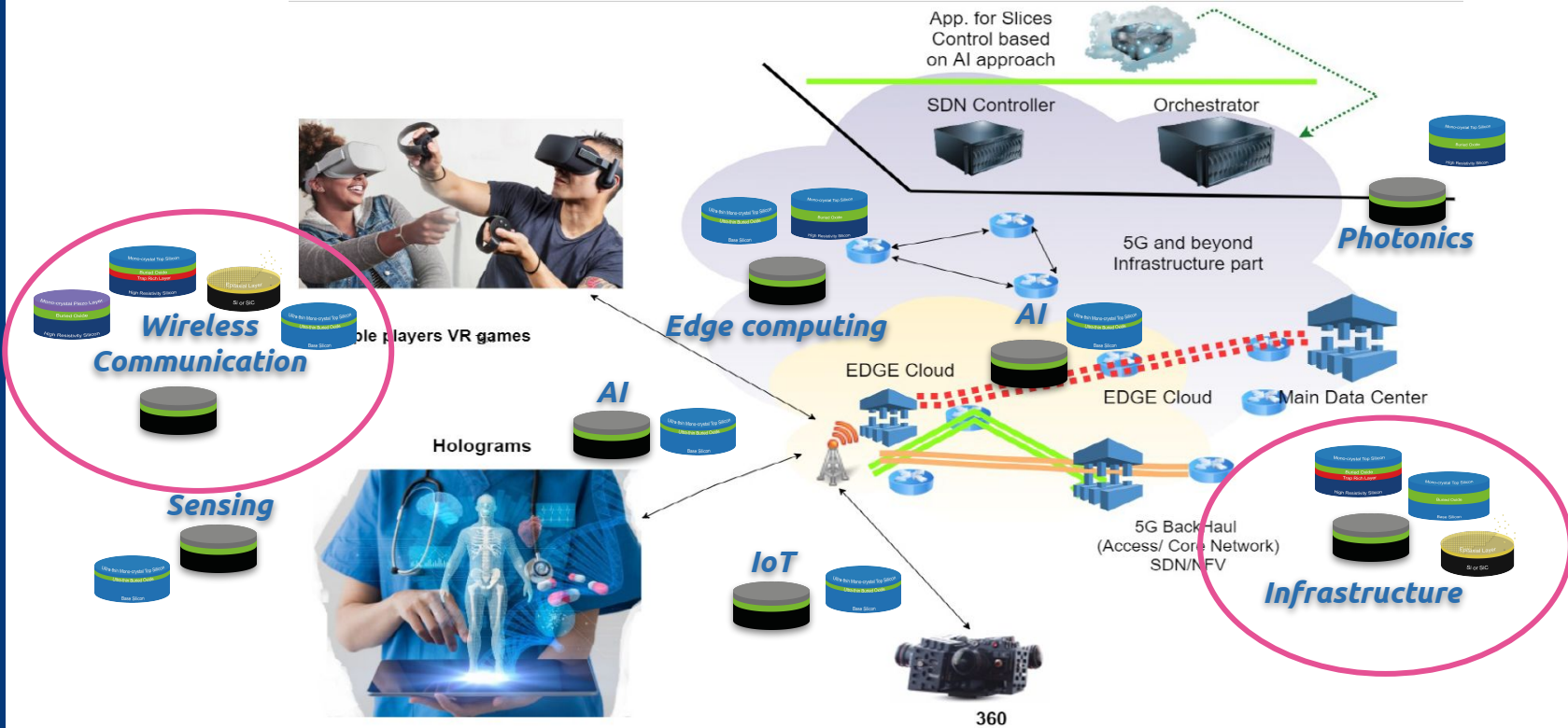


Illustration of mobile edge computing (MEC) servers with multiple users*
Alshahrani, et al., Appl. Sci. 2020, 10(16)

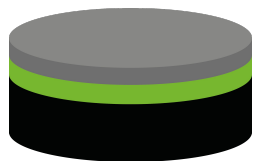
*Considering high offload architecture

2

Engineered substrates for RFFE applications



Anything on Anything - Best active layer on functional substrate



- **Device Layer:**
Silicon, Strained Silicon, SiC, Germanium, InP, GaAs, GaN, InGaN, LiTaO₃, LiNbO₃...
- **Buried Insulator:** SiO₂, ONO...
- **Handle Substrate:**
CZ Silicon, High-resistivity Si, Sapphire, Glass, GaAs, Ge, SiC

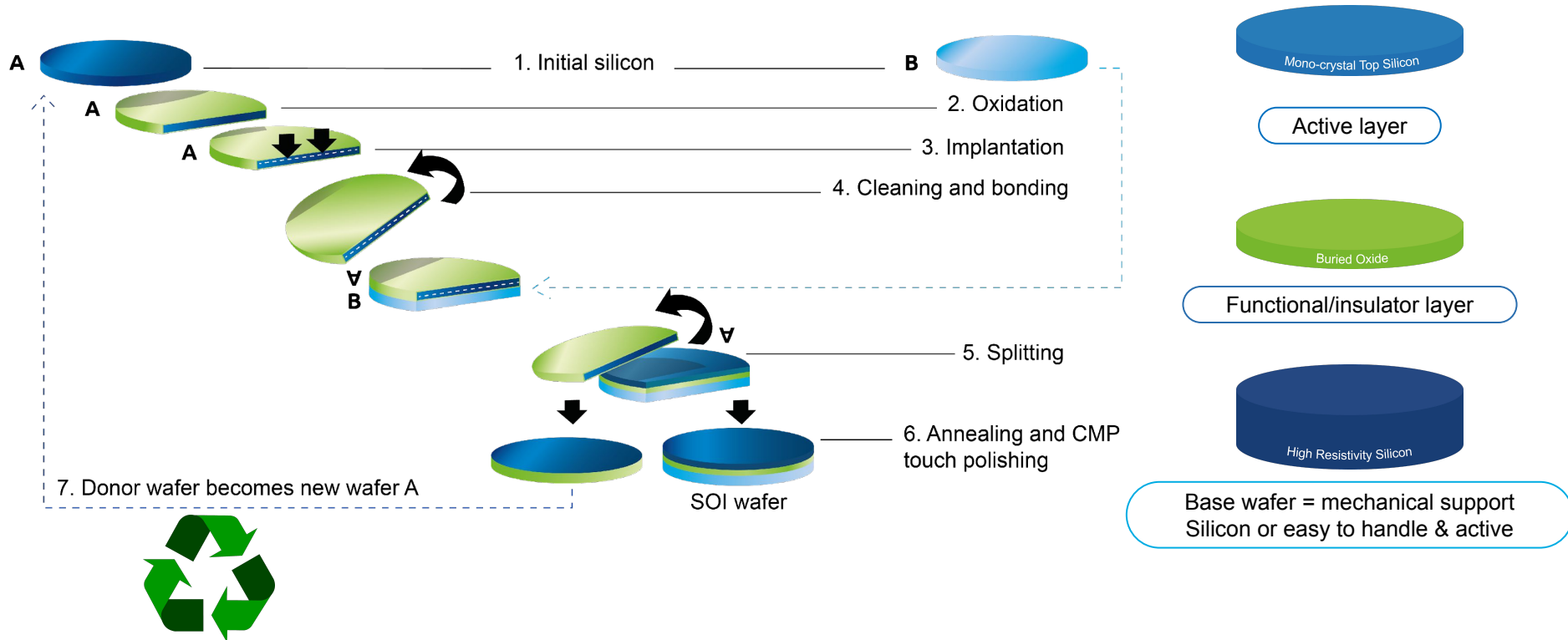
Ranging From 6" to 12"
wafer diameter to benefit
economies of scaling

		ACTIVE LAYER						
		Silicon	Piezo	SiC	InP	GaN	GaAs	Ge
HANDLE WAFER	Silicon							
	Sapphire							
	SiC							
	GaAs							
	Device wafer							

Engineered substrates offer best-in-class solution for
performance, energy efficiency, integration and cost benefits

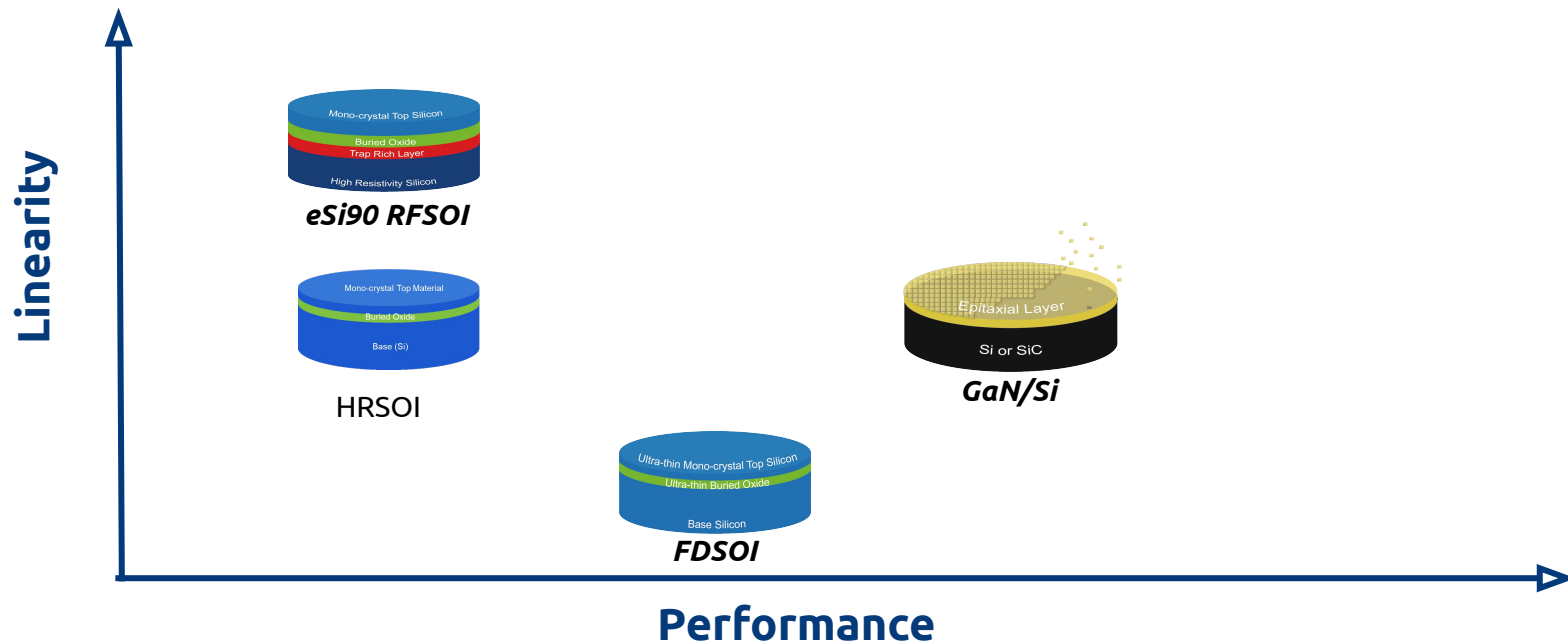
Revolutionary Smart Cut™ - a mature technology

TECHNOLOGY



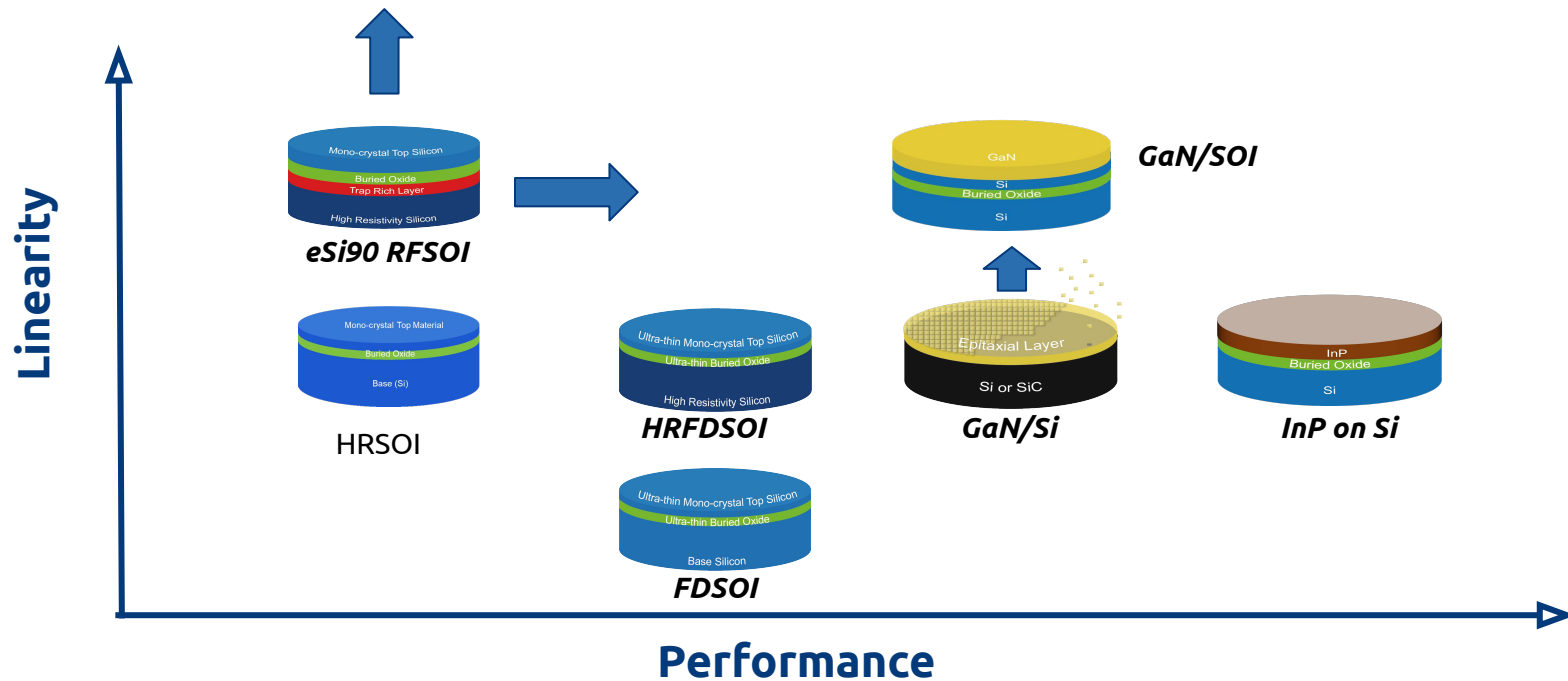
Substrates for RFHE - Linearity & performance

Cost, Capacity, Integration & thermal aspects are also dimensions considered.



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Cost, Capacity, Integration & thermal aspects are also dimensions considered.

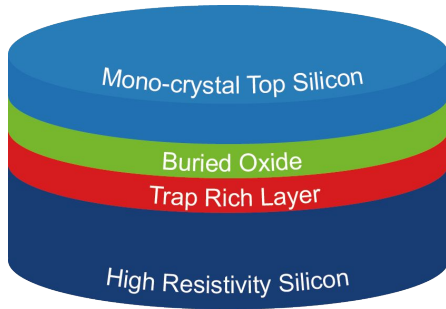


2

Getting more G from engineered Substrate

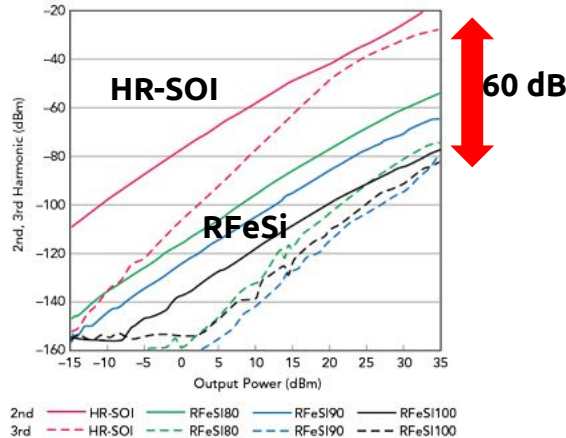
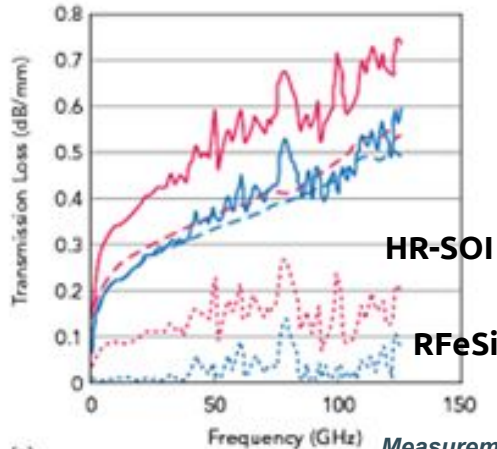


RF-SOI for RFFE



200, 300mm diam.

- RFeSi substrates provide the benefit of Si CMOS and a high-resistivity substrate
- Parasitic reduction and high-speed transistors
- High-quality RF passives with improved quality factor and low-loss interconnections
- Highly linear substrate (for RF switches and passives) also at mmW
- Compatible with <40nm nodes



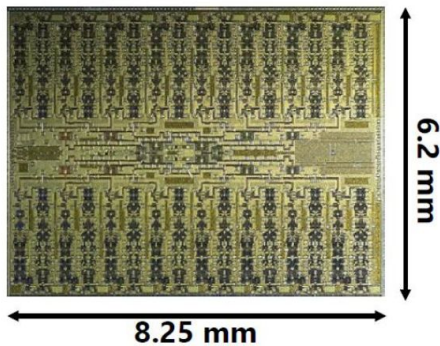
Measurements performed in collaboration with UCLouvain

- 45nm RFSOI solution for 28 GHz fixed-wireless and phase array beamformer already in production (ADI, Mixcom, Anokiwave)
- Transmitter at >100 GHz recently presented

RF-SOI solution for 28GHz phase-array beam formers FEM

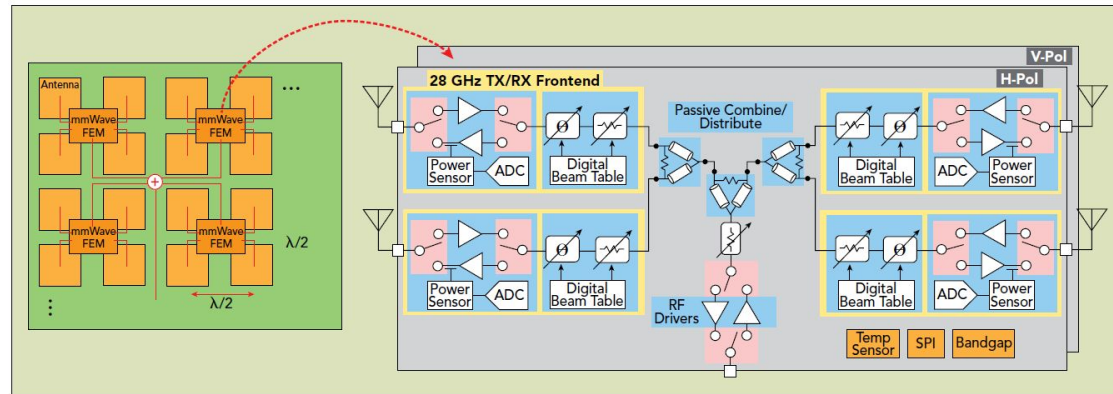
- RF-SOI provides high-level of digital/analog integration
 - required for bias/gain/phase control
 - and available memory blocks for large beam tables storing
- High-output power (>20 dBm) and gain (>30 dB), as well as breakdown voltage
- Fast and highly linear RF switches (best-in-class)
- Technology of choice for fixed-wireless CPEs and mobile infrastructure in urban environments

**28GHz 16 channel beamformer
on 45 nm SOI CMOS**



Ref: Khalil et al, ISSCC'21

Diagram of large-scale mmW phased array using 2x2 dual-pol. beamforming FEM



Source: MixComm

RF-SOI also for > 100 GHz applications

Beamforming phase-array transmitter at 140 GHz using 45 nm RF-SOI CMOS

8-Element 140 GHz Phased-Array Transmitter w/ 32 dBm Peak EIRP and > 16 Gbps 16QAM and 64QAM Operation

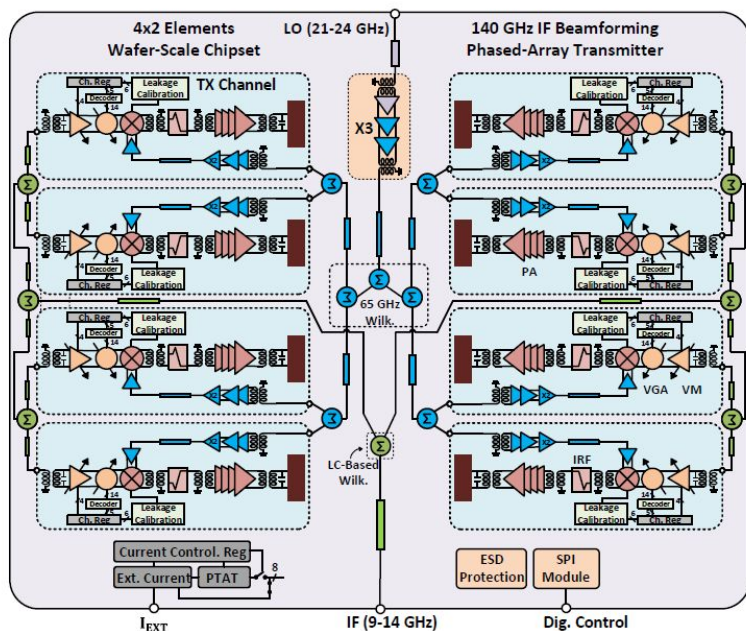


Fig. 1. Block diagram of 8-element wafer-scale IF beamforming phased array transmitter chipset at 140 GHz in CMOS-SOI.

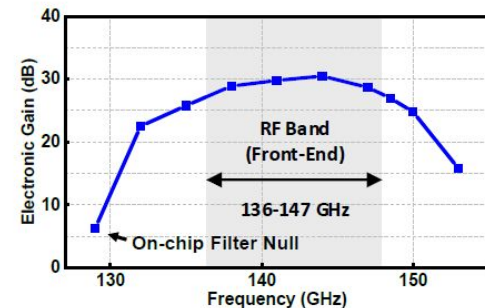
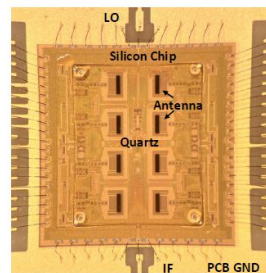
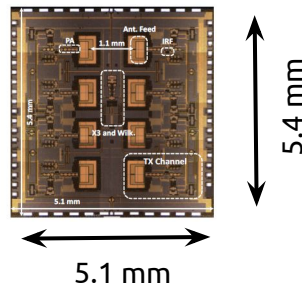


Fig. 4. Measured array electronic gain with a fixed IF frequency (11 GHz).

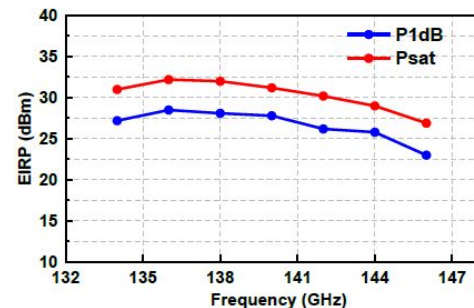
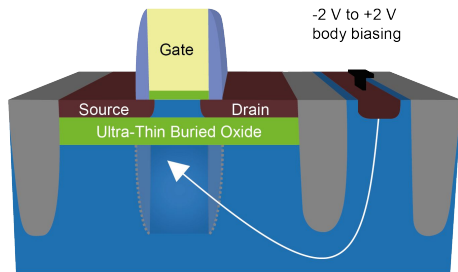


Fig. 5. Measured 8-element phased-array transmitter EIRP at P1dB and Psat versus frequency.

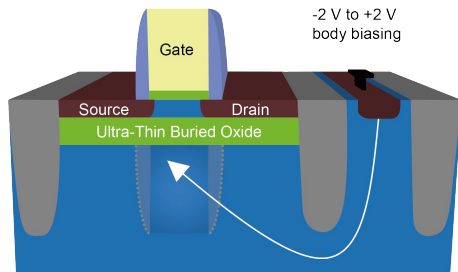
Ref: Siwei Li et al, RFIC'21



FD-SOI for mmW and 6G

- FD-SOI gives superior power/performance tradeoff
- Smaller process variability
- Better analog/RF performance
 - Higher bandwidth/lower power
 - Lower noise
 - Less parasitics
 - Higher f_t/f_{max} : 350/400
(22FDX 28GHz benchmark)
- Cost effective: planar CMOS technology
- Tech. of choice for mmW FEM integration (analog/digital)

- FD-SOI already being used for 5G mmW FEM in Google Pixel and Mediatek 5G products
 - Samsung S5633 mmW RxTx module built on 28FDS technology
 - MediaTek Dimensity 1050 mmW Antenna-in-Package module built on 22FDX



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- FD-SOI already being used for 5G mmW FEM in Google Pixel and Mediatek 5G products
- FEM, LNA, SPST switch @ >100GHz already being presented



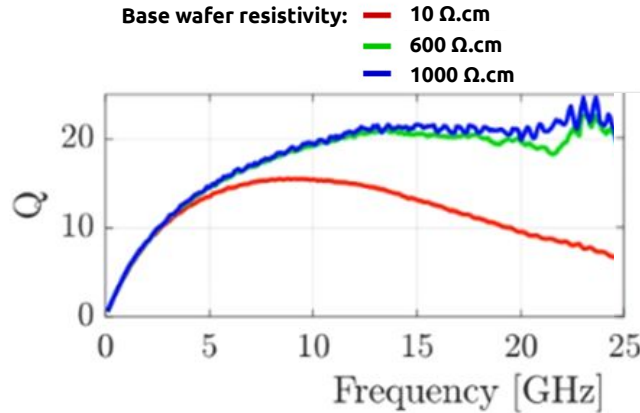
Better RF passives
Higher on-chip antenna efficiency
Noise reduction

- Opportunity with 12nm FD-SOI for lower consumption and higher performance

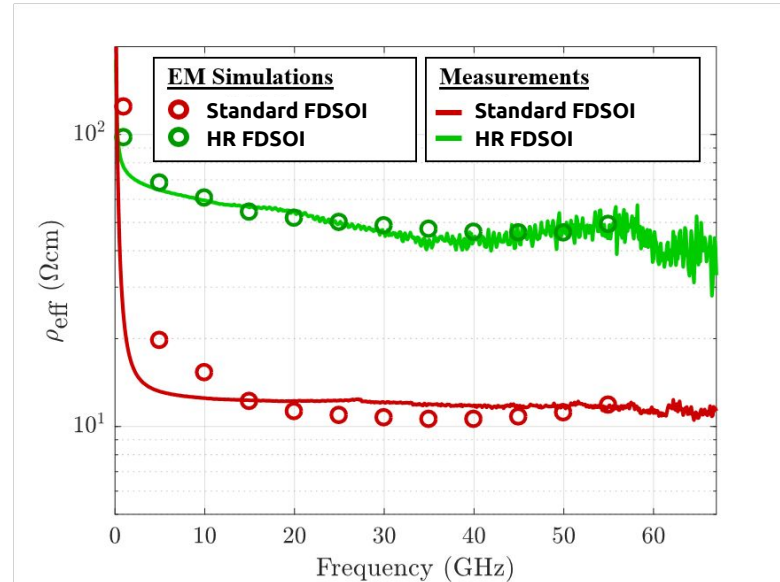
HR FDSOI: improved RF performance

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50% inductor Q-factor improvement and increased effective resistivity



Adapted from L. Nyssens et al. MIKON 2022



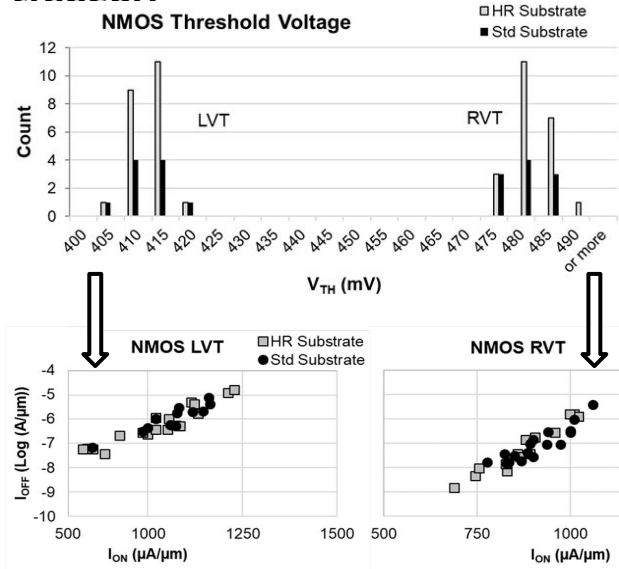
L. Nyssens et al. EUROSOI 2022

Same logic performance as standard FDSOI

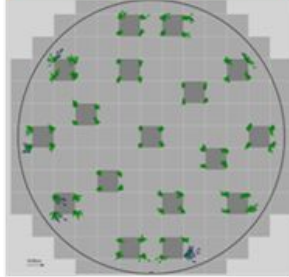
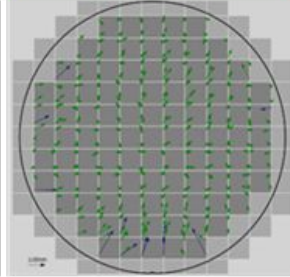
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Moving to HR base impacts neither wafer processing nor logic devices performance

MOSFETs Threshold voltage and I_{ON}/I_{OFF} tradeoff



Same wafer processability with HR base.

Susbtrate	Std FDSOI	HR FDSOI
Overlay	$ \mu +3\sigma = 8.2 \text{ nm}$	$ \mu +3\sigma = 8.4 \text{ nm}$
		

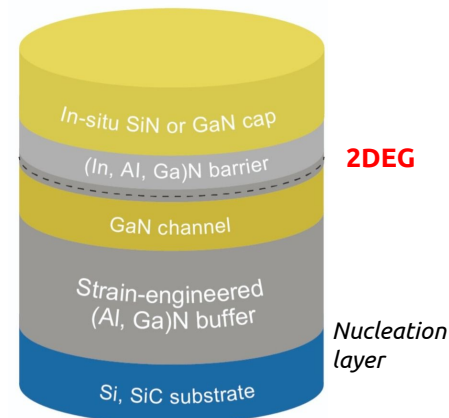
Source : STM, 2021

Adapted from I. Bertrand et al. ECS 2022

GaN RF technology

GaN RF technology is typically deployed in the sub 6GHz and X-band

- Typically based on 20nm Al_{0.25}Ga_{0.75}N / GaN HEMT (epitaxially) grown on:
 - SiC $\Rightarrow$ high-end & cost
 - Si $\Rightarrow$ low-cost (opportunity for handset)
- Features very high power density ($\sim 10\text{W/mm}$) and high PAE ($>65\%$)
- Operated at 28V or 48V
- High temperature capability
- Typical application is in infrastructure (base stations)



GaN HEMT epitaxial structure on carrier

GaN RF technology for mmW

- Gate length scaling for lower-power density and PAE
- Barrier technology and epitaxy engineering
- Proved PA operation at 90 GHz (PAE 29%)
- Towards 300mm wafer size for Si compatibility

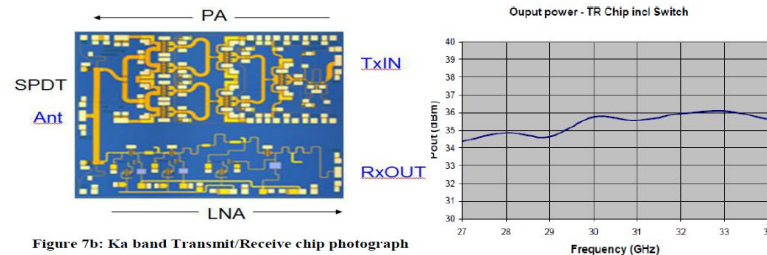


Figure 7b: Ka band Transmit/Receive chip photograph

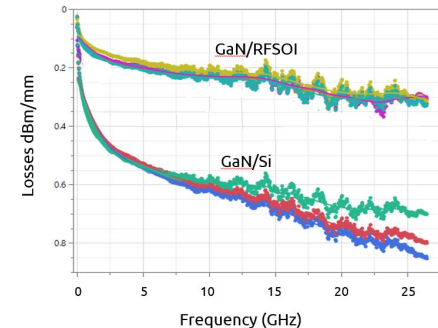
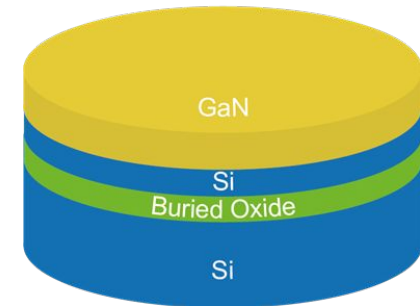
Fully integrated millimetre-wave 5G 26-34 GHz transmitter/receiver (Courtesy of Ommic)

New substrate innovation - path to co-integration

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GaN on (RF-)SOI

- Replace HR-Si substrate by RF-SOI
 - Lower cost than SiC and larger diameter enabler
- Better vertical isolation and increased linearity
- Higher BW due to smaller feedback (vertical) capacitance
- Could allow PA, LNA and switch integration on GaN
- Possible path for Si CMOS co-integration and mobile handset application
- Thermal performance considered in substrate design

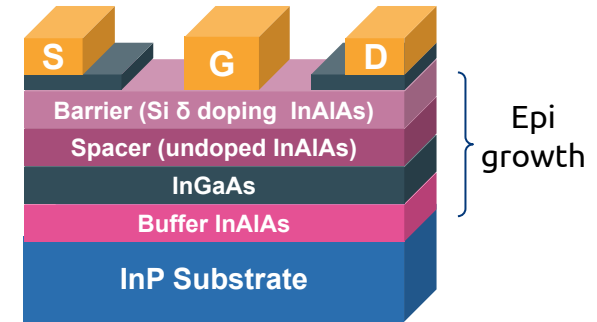


	H2 (dBm)	H3 (dBm)
GaN/Si	-65	-70
GaN/RF-SOI	-90	-115

InP for mmW and sub-THz

InP has major advantages for RF

- Best PA technology for applications > 100GHz
 - 250nm InP → f_{max} of 600GHz, w/ BDV of 4.5V,
 - Multistage InP PAs > 20 dB of gain and PAE>25% @ 140GHz
- Higher thermal conductivity than GaAs
- InP is the only technology f_{max} at THz

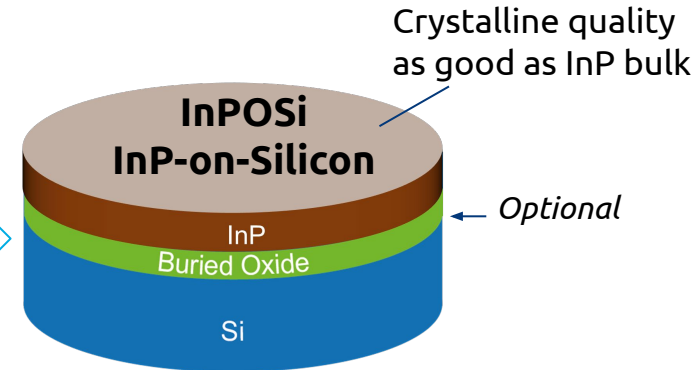


InP HEMT

... but bulk InP has also major drawbacks

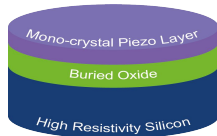
- Expensive material
- Brittle material
- Poor availability
- Low diameter bulk substrates,
(mostly limited to 100 mm today)

**engineered substrate
solution**



*Example of a possible stack
(Other carriers (e.g. GaAs), dielectrics and
bonding interfaces can be considered)*

Piezo On Insulator (POI) for 5G and beyond



POI technology adopted by key players for single Integration single multiplexer

POI technology development on going

- Low Band <1GHz
- Ultra High Band >3.5GHz
- 200mm diameter

Innovative substrates required for covering extended spectrum beyond 10GHz

- FR3 deployment
- Ku bands (5G NTN)

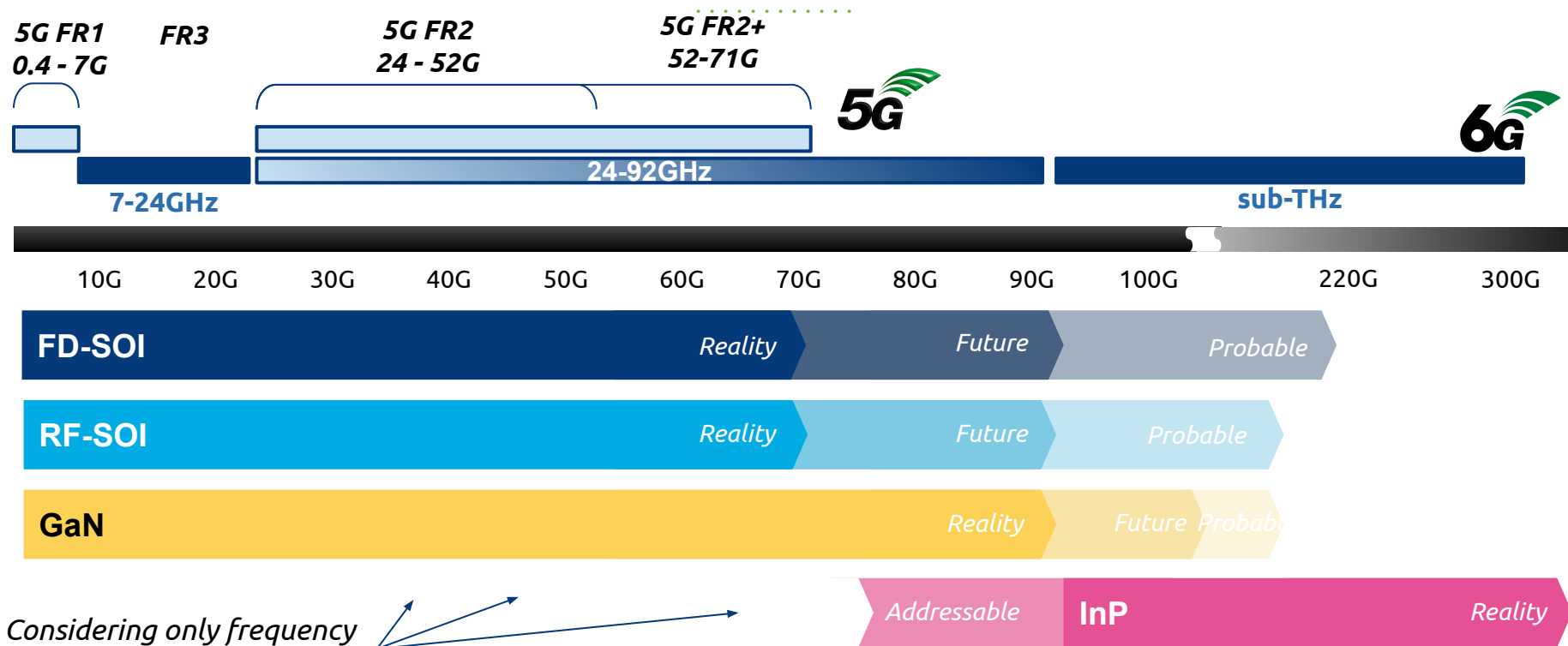
	SAW	TC-SAW	BAW	SAW on POI
Operating Frequency (GHz)	Low - High	Low - High	High Ultra High	Low - High Ultra High
Quality Factor (Bode Q) @2GHz	1500	<1500	4000 (AlN)	>4000
Coupling factor k^2	<7% (LiTaO ₃)	<7% - LiTaO ₃ <20% - LiNbO ₃	<7% - AlN <12% - AlNsc	>8% - LiTaO ₃ >20% - LiNbO ₃
Temperature Compensation (ppm.K ⁻¹)	>40 - LiTaO ₃	<20 - LiTaO ₃	>20	< 10 - LiTaO ₃
Substrate complexity	Low	Low	Low	High
Process complexity	Low	Mid	High	Low
Integration	Low	Low	Low	High

3

Takeaways and Conclusions

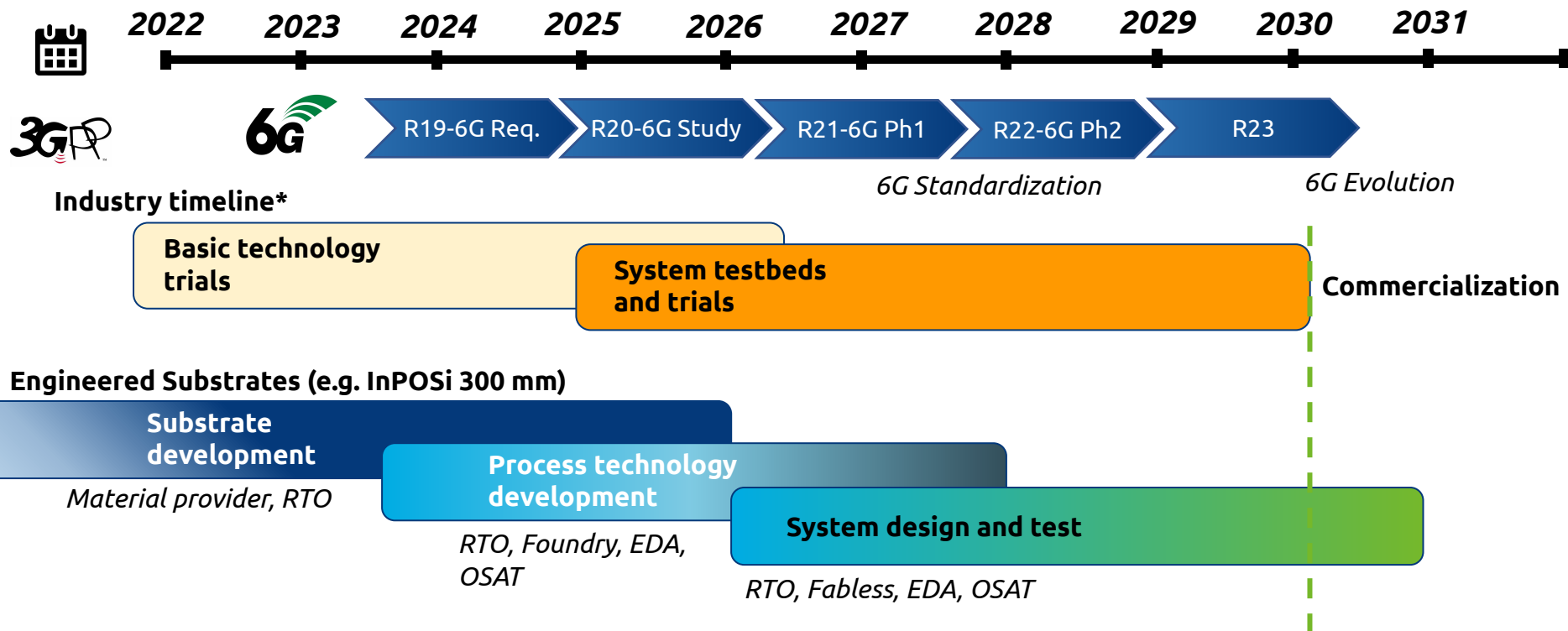


Engineered Substrates solutions for 6G vs frequency



Substrate choice is done function of application, efficiency, cost and other parameters

6G likely-timeline - for engineered substrates



It is a multi-player business, involving the whole semiconductor ecosystem

**Source: SAMSUNG, Ericsson*

Conclusions



- Engineered substrates (for 5G) are being continuously improved for 6G
- It is time to identify 'Materials for 6G' and integrate them into optimized engineer substrate.
- CMOS & III-V co-integration schemes shall be considered when designing and choosing engineering substrates for 6G
- Time is of the essence: Engineered substrates are at the beginning of the value chain and require collaboration, investment and strong motivation to happen

Thank you

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