

Sustainability Driven Innovation: transistor scaling and defectivity targets for sustainable manufacturing

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Outline

- ◆ Transistor scaling and Defectivity targets
- ◆ R&D Challenges to developing next-generation cleaning
- ◆ Sustainable manufacturing
- ◆ Fundamental studies for the next level
- ◆ Summary

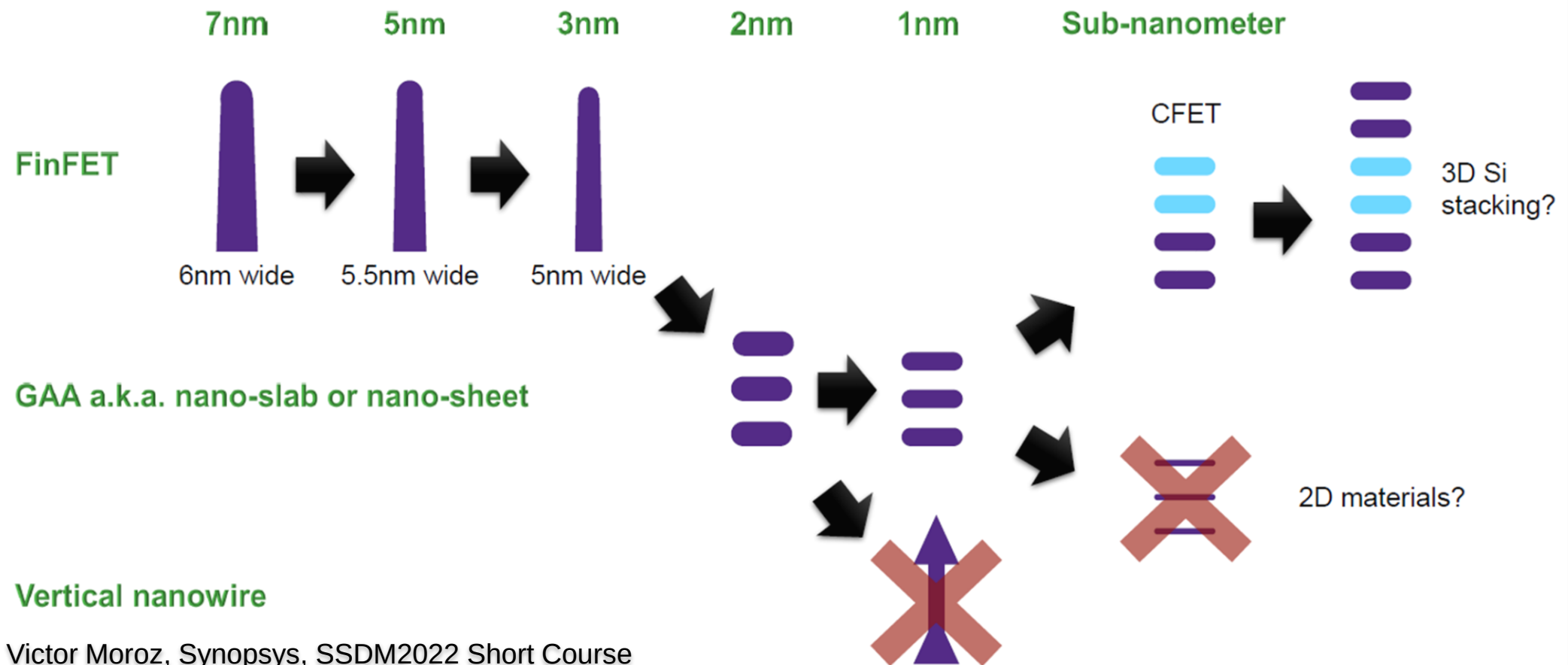
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Logic Transistor Scaling (1)

◆ Complexity increases toward CFET

Expected Transistor Evolution Going Forward

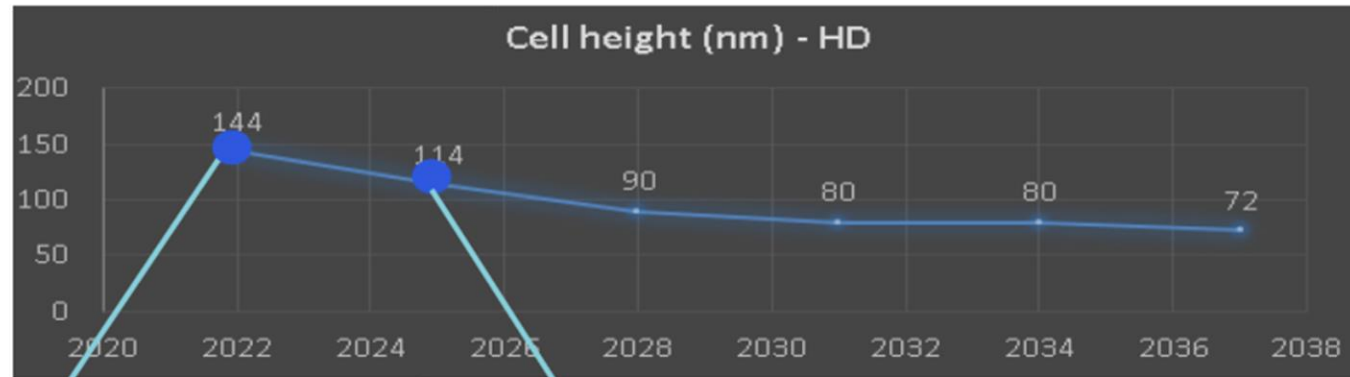


Victor Moroz, Synopsys, SSDM2022 Short Course

Logic Transistor Scaling(2)

◆ Lateral scaling is going to the end ~ 2030

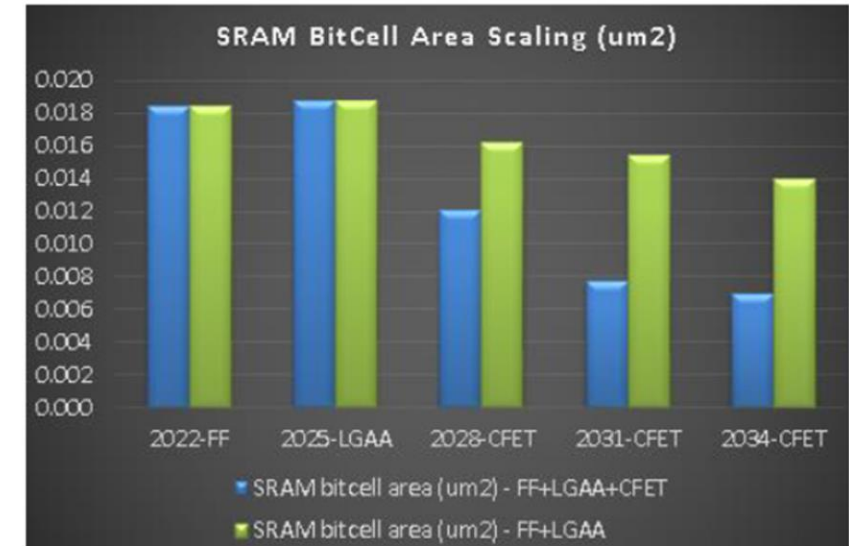
Bitcell and cell height saling



Source: IEEE IRDS More Moore 2022 edition

Standard cell employing finFET

Standard cell
Employing GAA + buried rail + backside metallization

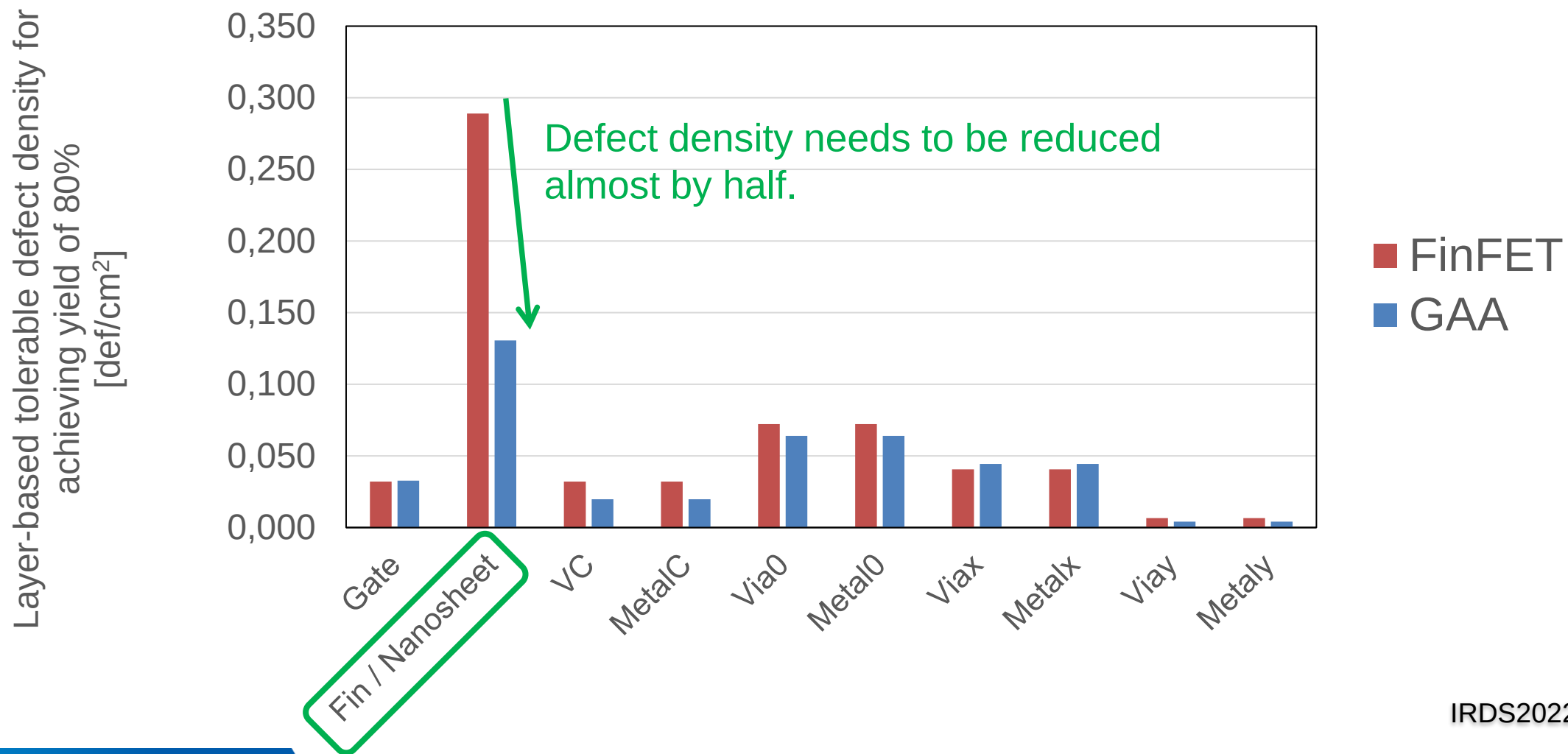


- CFET helping HD bitcell area scaling by 2028
- Buried rail enabling ~110nm cell height by 2025
- Cell height<90nm forecasted by 2028

Mustafa Badaroglu, Qualcomm, SSDM2022 Short Course

FinFET to GAA/NS defect requirement

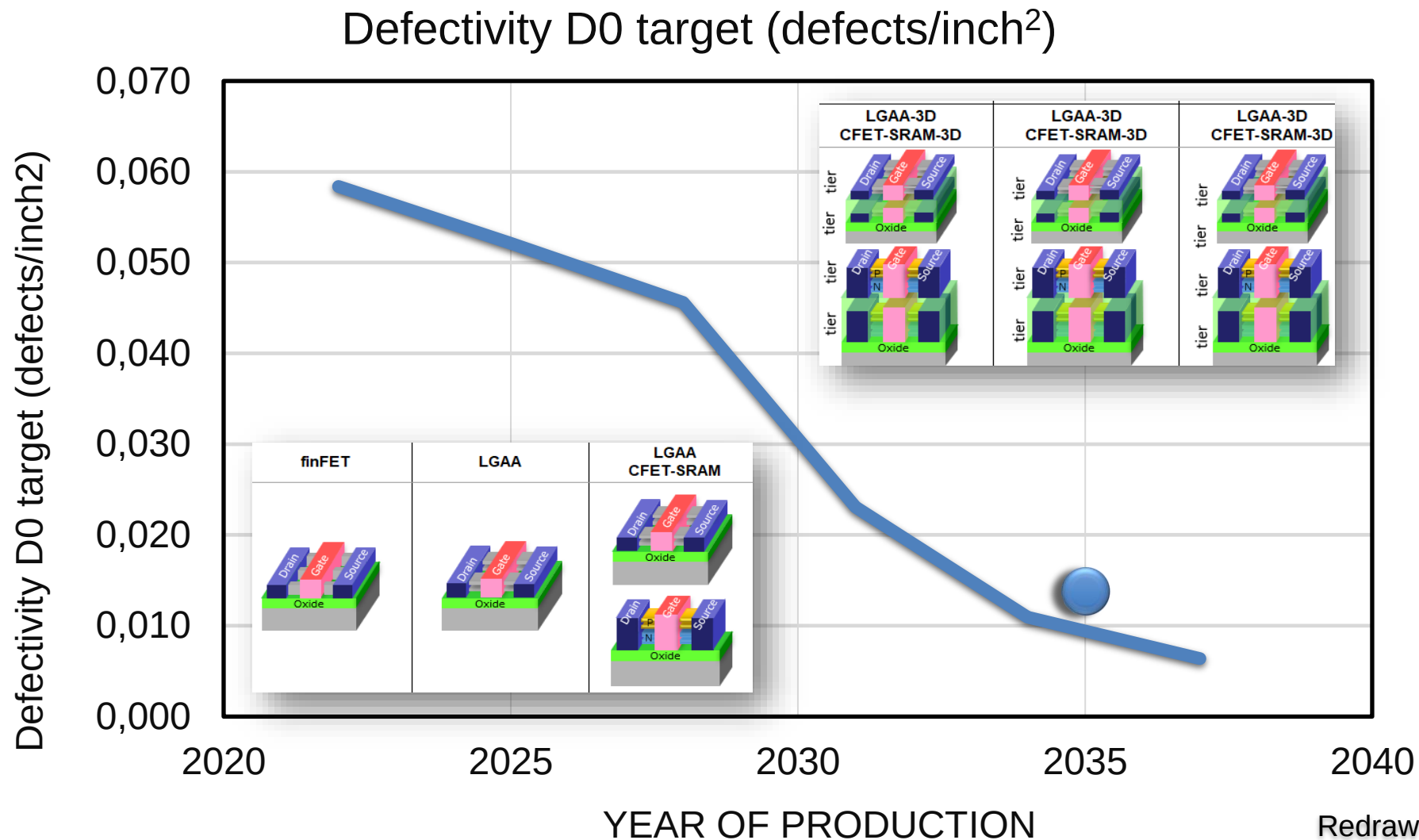
◆ Difficulty doubled for GAA/NS defect control



IRDS2022 YE

More defect challenges are on the way

◆ Defect control becomes even more challenge beyond ~2030

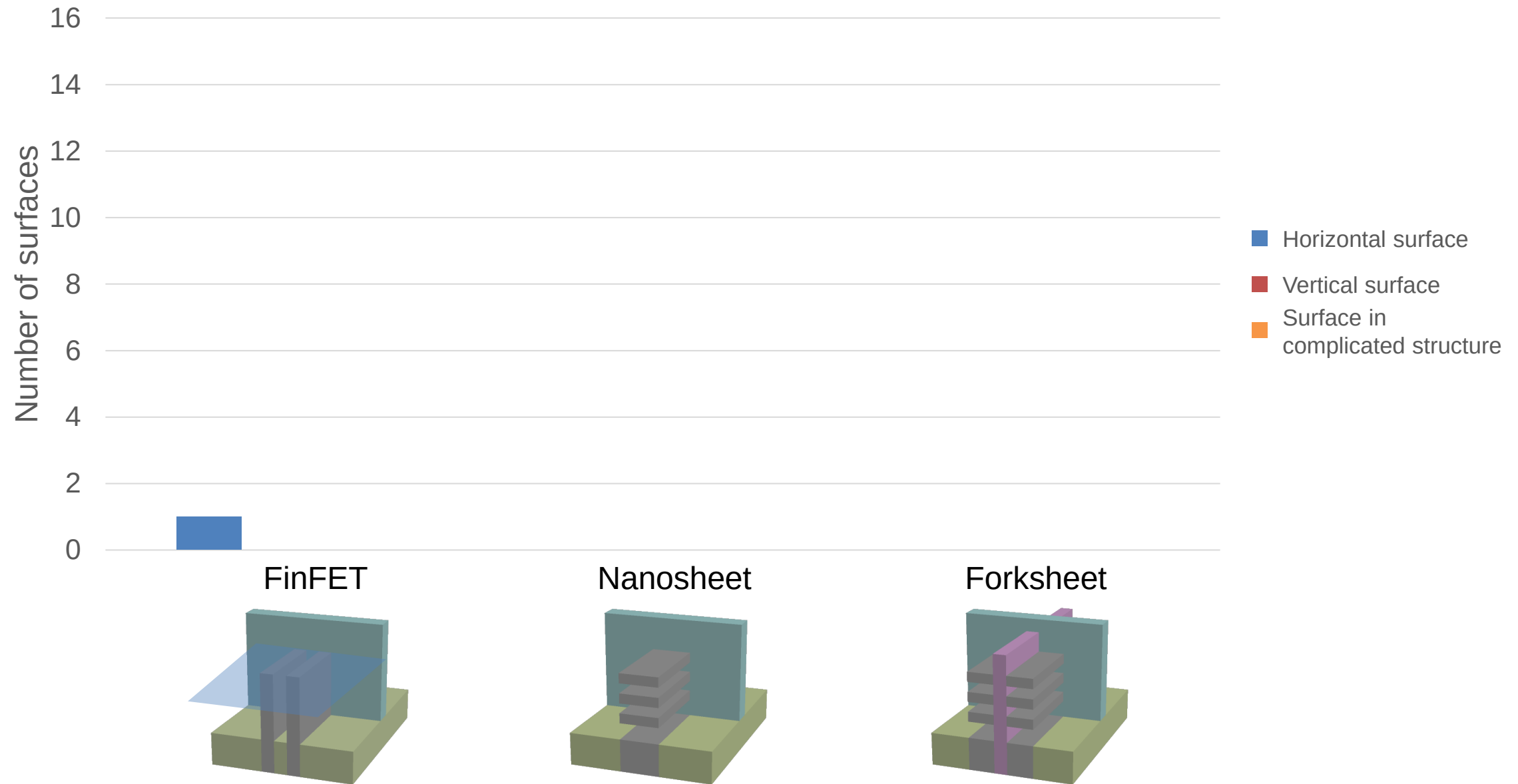


Redraw from IRDS2022 MM

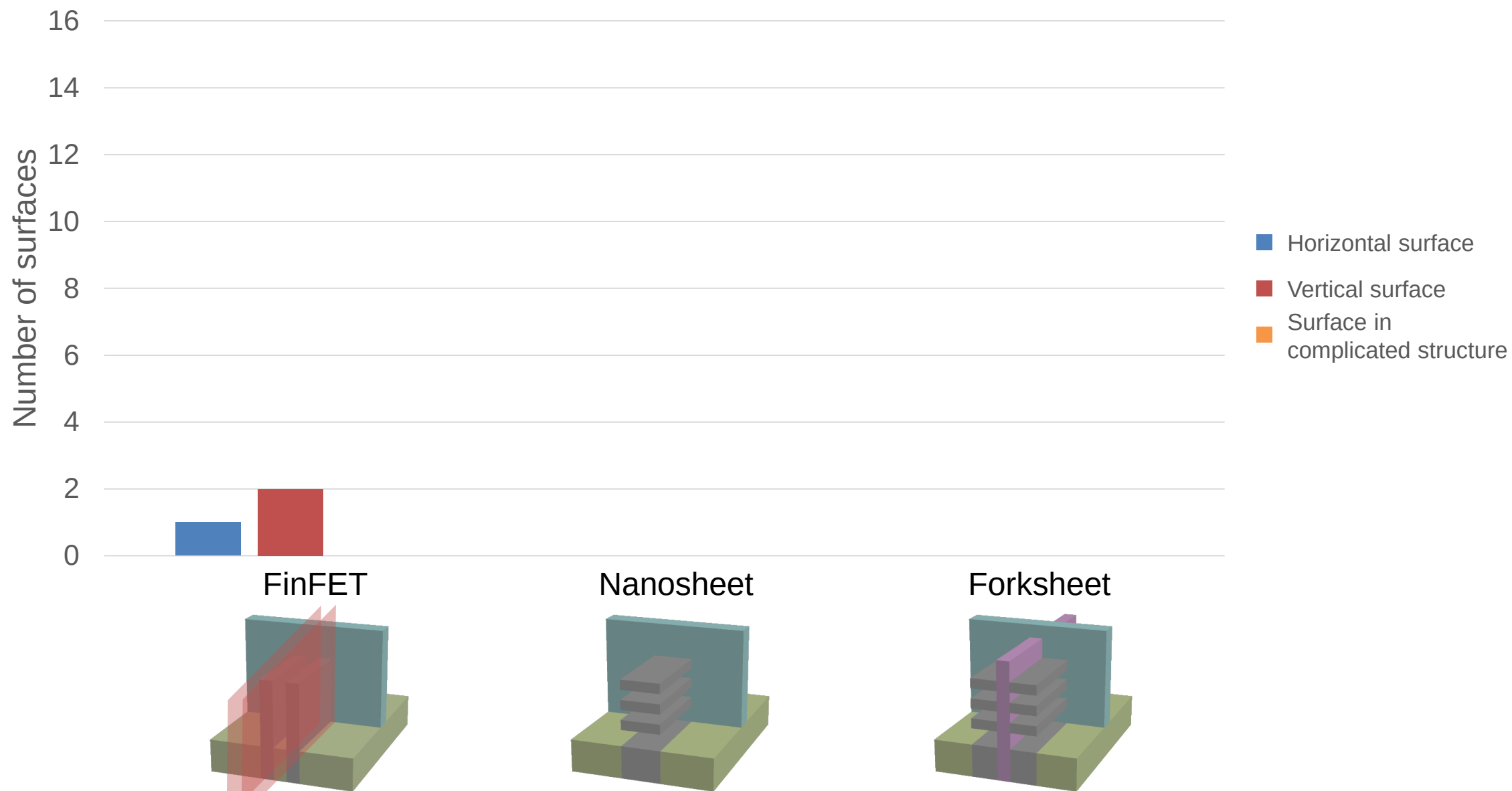
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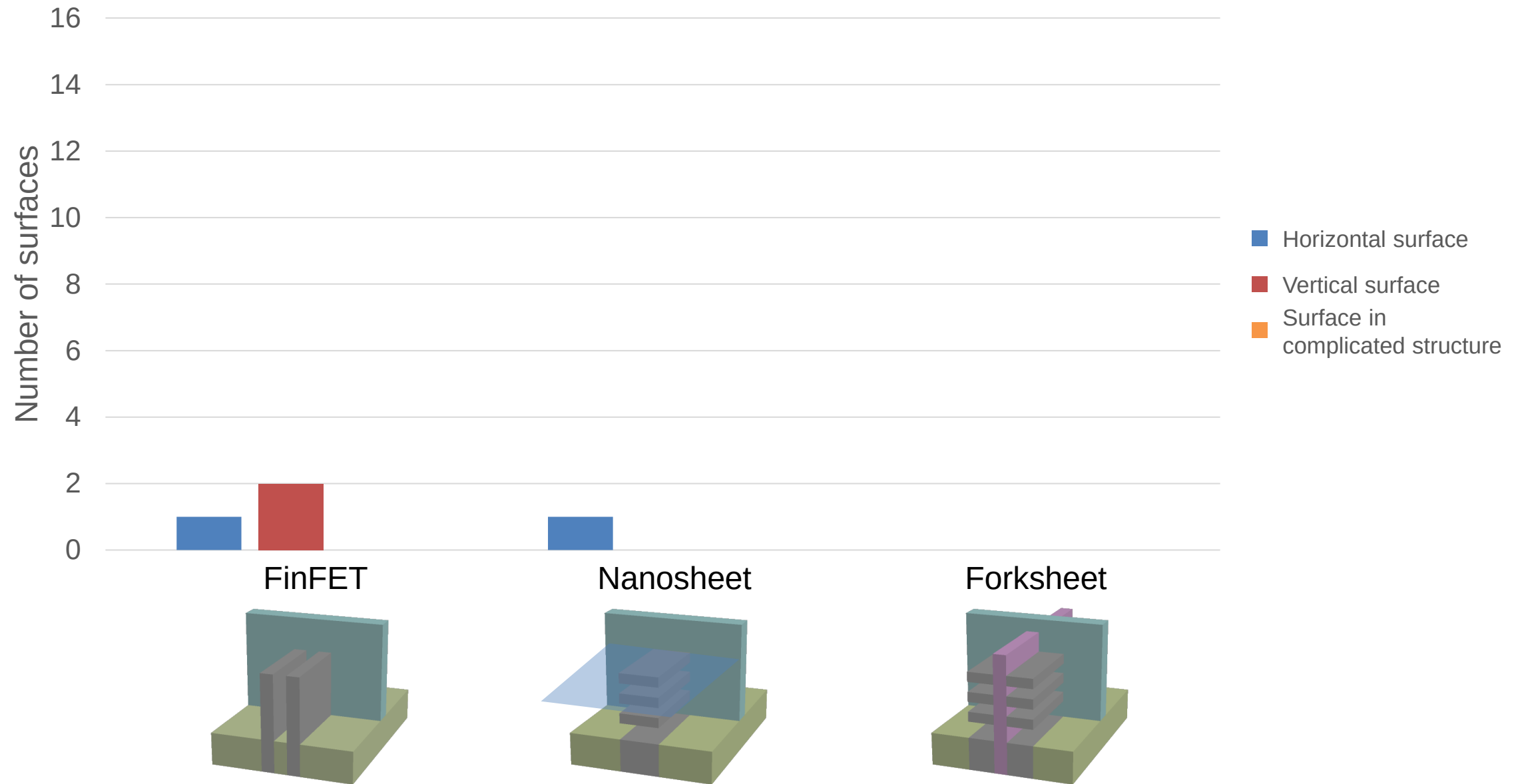
Cleaning challenge for GAA and Forksheet era



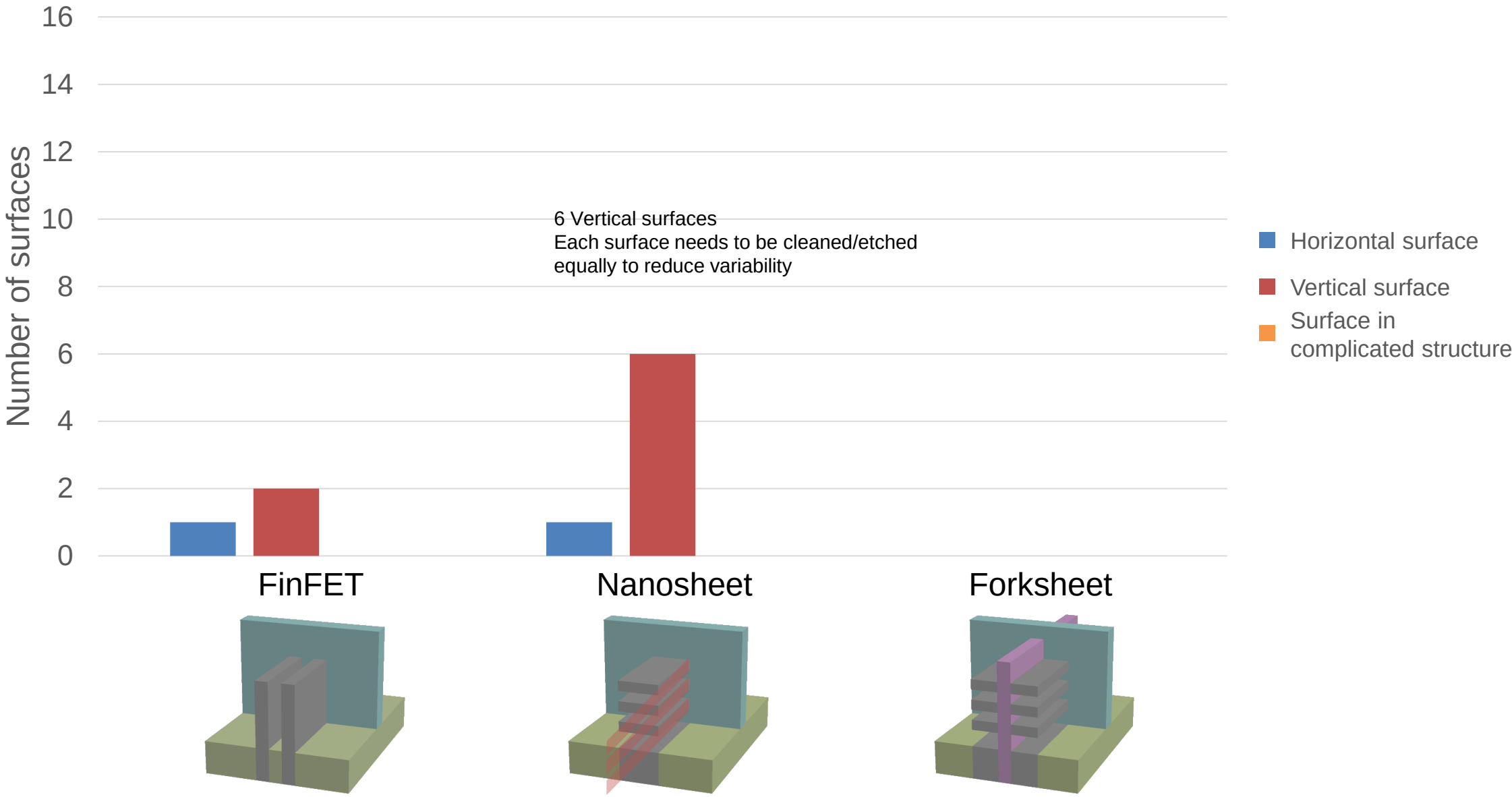
Cleaning challenge for GAA and Forksheet era



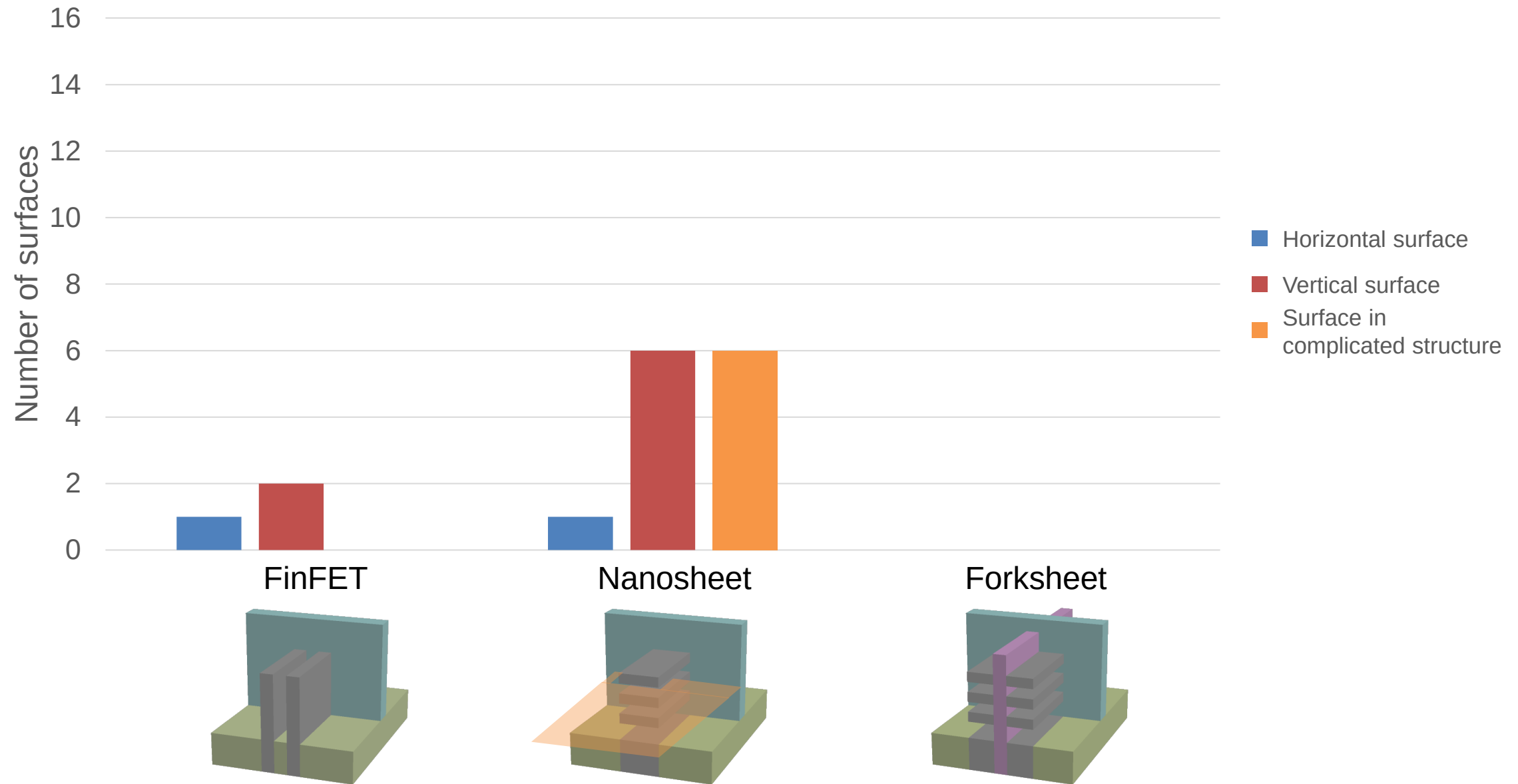
Cleaning challenge for GAA and Forksheet era



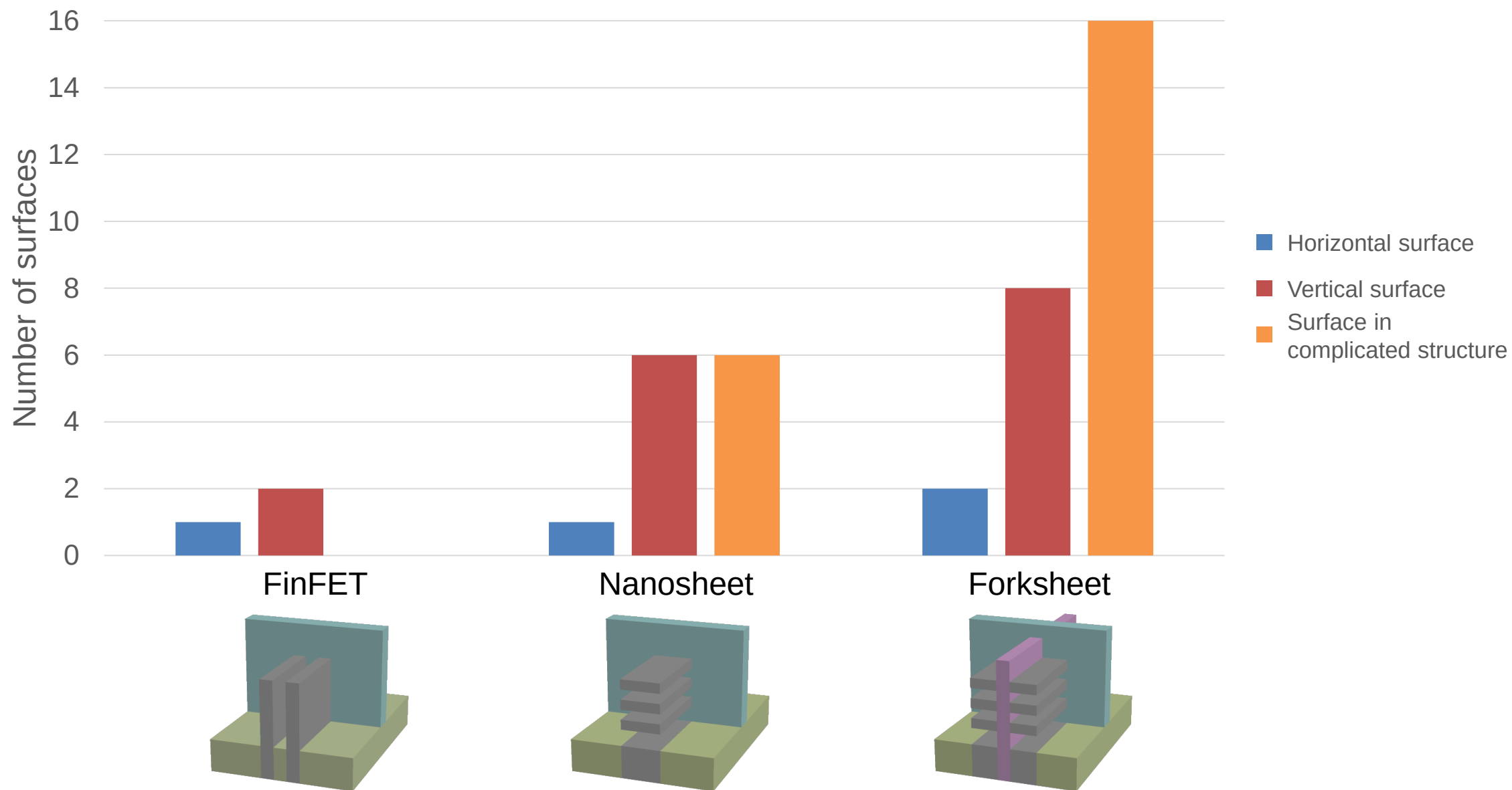
Cleaning challenge for GAA and Forksheet era



Cleaning challenge for GAA and Forksheet era

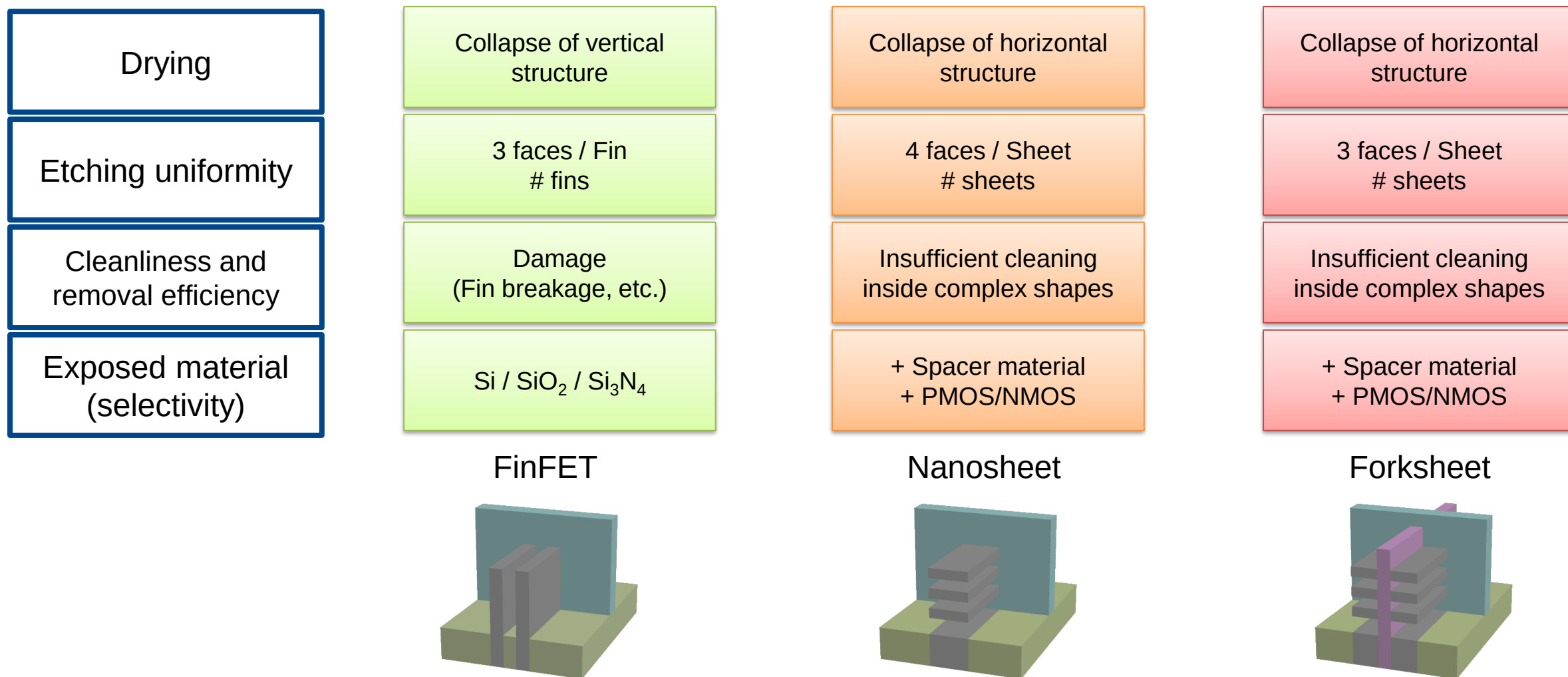


Cleaning challenge for GAA and Forksheet era



New devices create more challenges in cleaning

◆ New materials, more surfaces, defect density

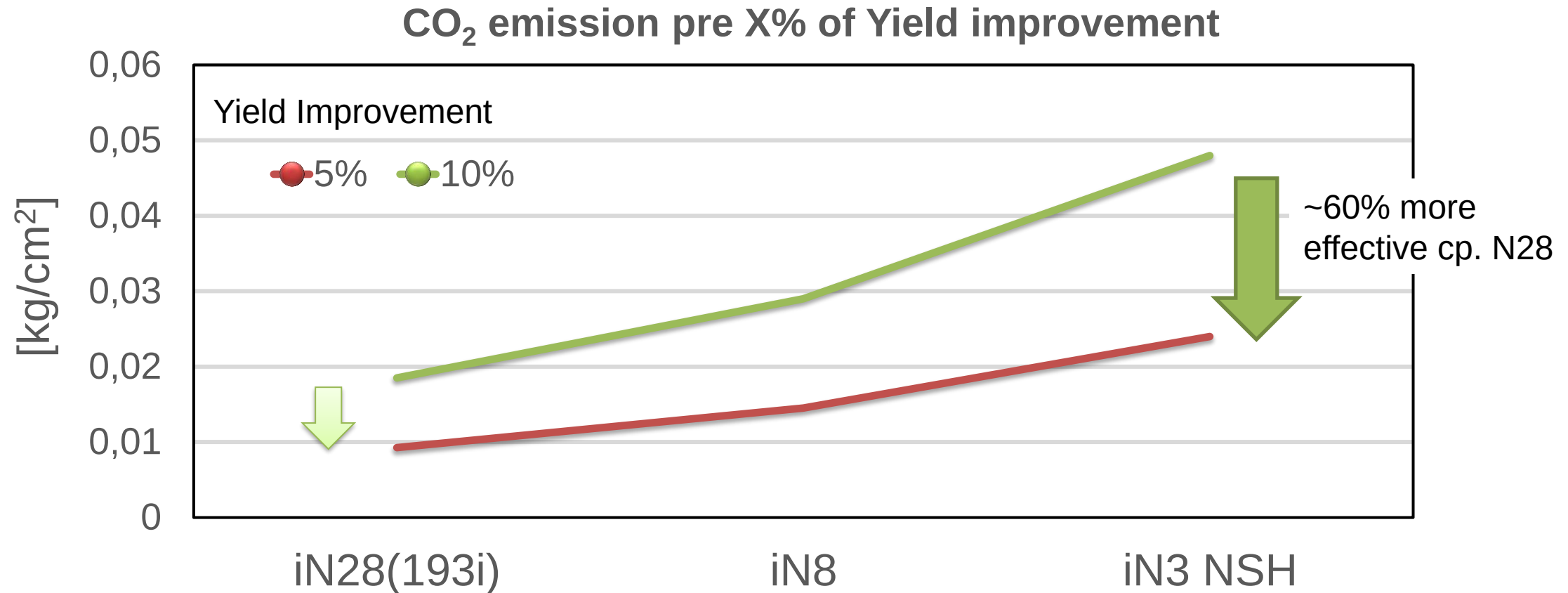


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Defect reduction to lowering CO₂ emission

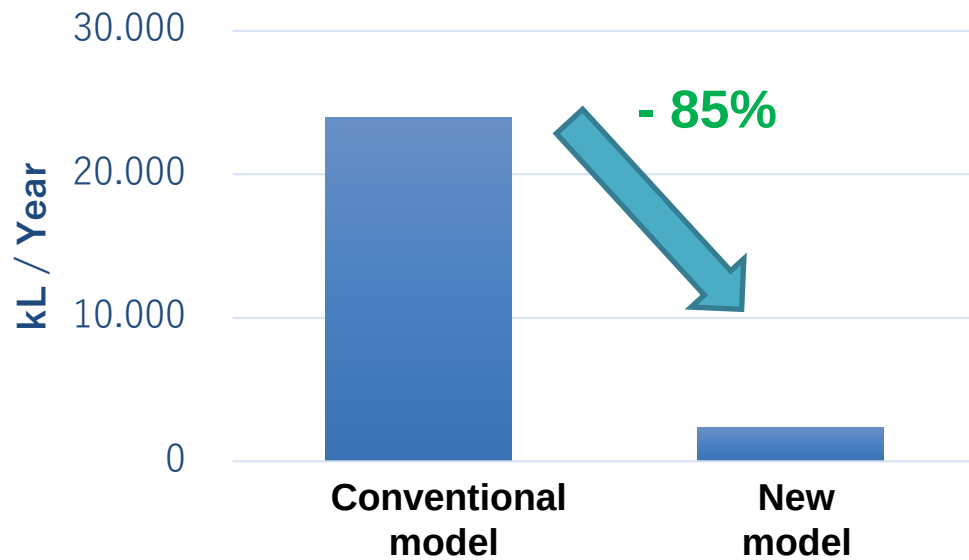
- ◆ Yield improvement is more important for Nanosheet even for CO₂ emission



Recent achievement by SCREEN(1)

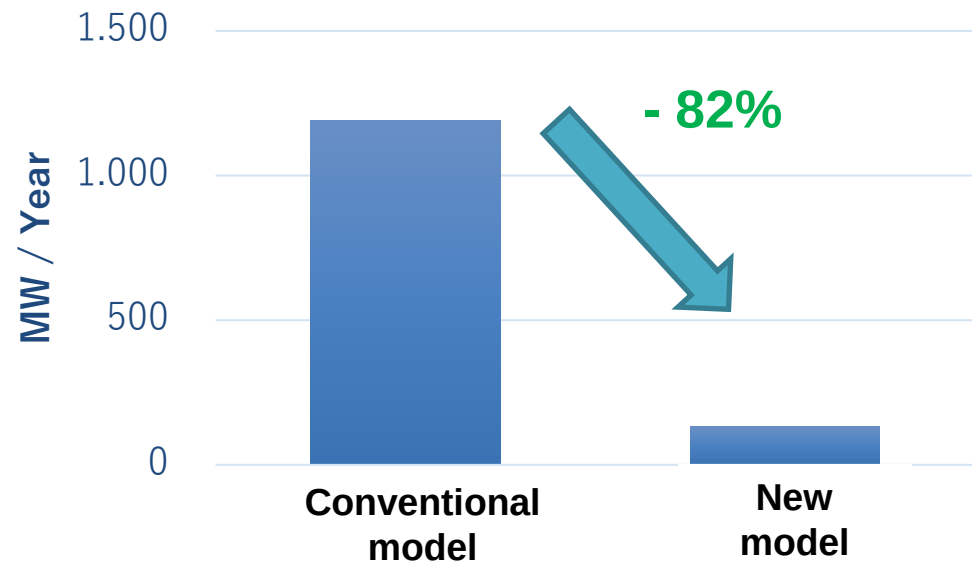
◆ Hot DIW recirculation to reduce waste DIW & energy

DIW consumption



DIW usage >
Reduced by 20,000 kL/year

Energy consumption

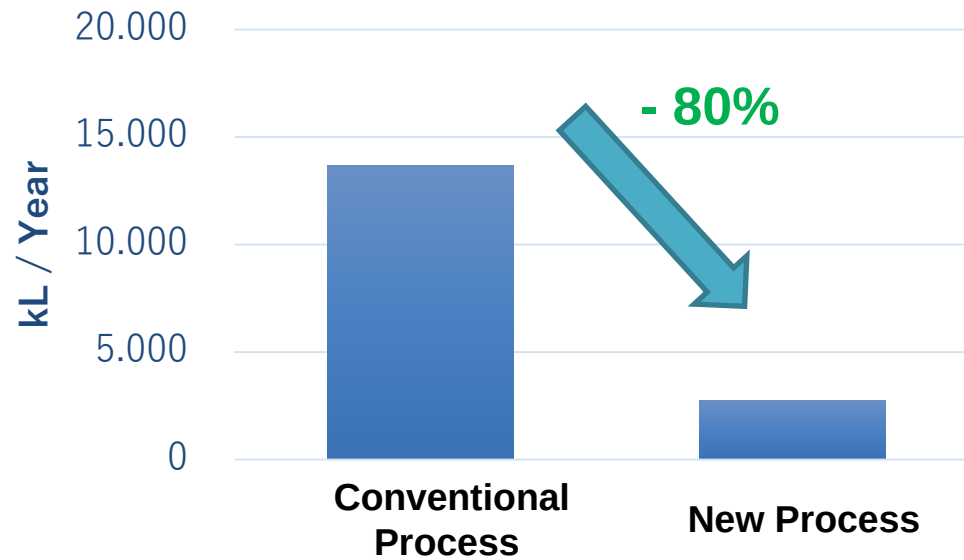


Power consumption at 60°C HDIW >
Reduced by 900 MW/year

Recent achievement by SCREEN(2)

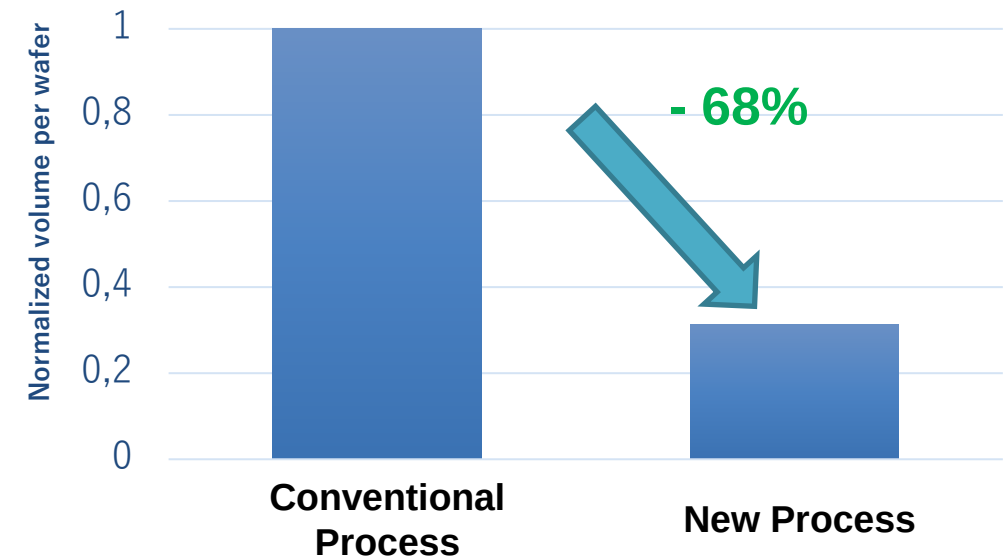
◆ DIW water and SPM usage reduction

DIW Consumption with reclaim



DIW usage >
Reduced by 10,000 kL/year

SPM Reduction



Sulfuric acid and hydrogen peroxide (SPM)
volume reduced by 68% per wafer

Sustainable manufacturing

- ◆ Yield improvement is the key to sustainable manufacturing of advanced node devices
 - ◆ Water, Energy, and Chemical saving are progressing now
 - ◆ Most importantly, collaboration for sustainability will drive technology development
- SCREEN is committed and an active player, join us.

Collaboration for sustainability

◆ International

- IMEC SSTS (Sustainable Semiconductor Technologies and Systems)
- SIA the Semiconductor PFAS Consortium
- SEMI Semiconductor Climate Consortium (Founding member)
- IRDS Water + Energy Taskforce

◆ Japan

- SDRJ (The System Device Roadmap Committee of Japan) EHS WG leader
- AIST Green Sustainable Semiconductor Manufacturing Technology WG
- TIT Research Institute for Integrated Green-niX

◆ Private

- Collaboration with Nagase & Zeroboard
- Many customer collaboration

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Overview of joint research



北海道大学
HOKKAIDO UNIVERSITY

LC-TEM

SCREEN

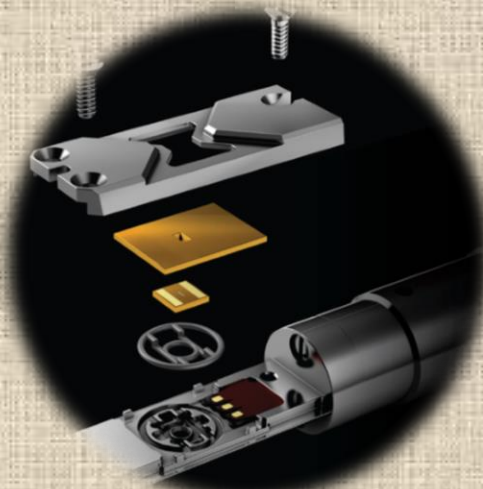
Substrate observation
technology

Substrate processing
technology

Hokkaido University's
proprietary technology

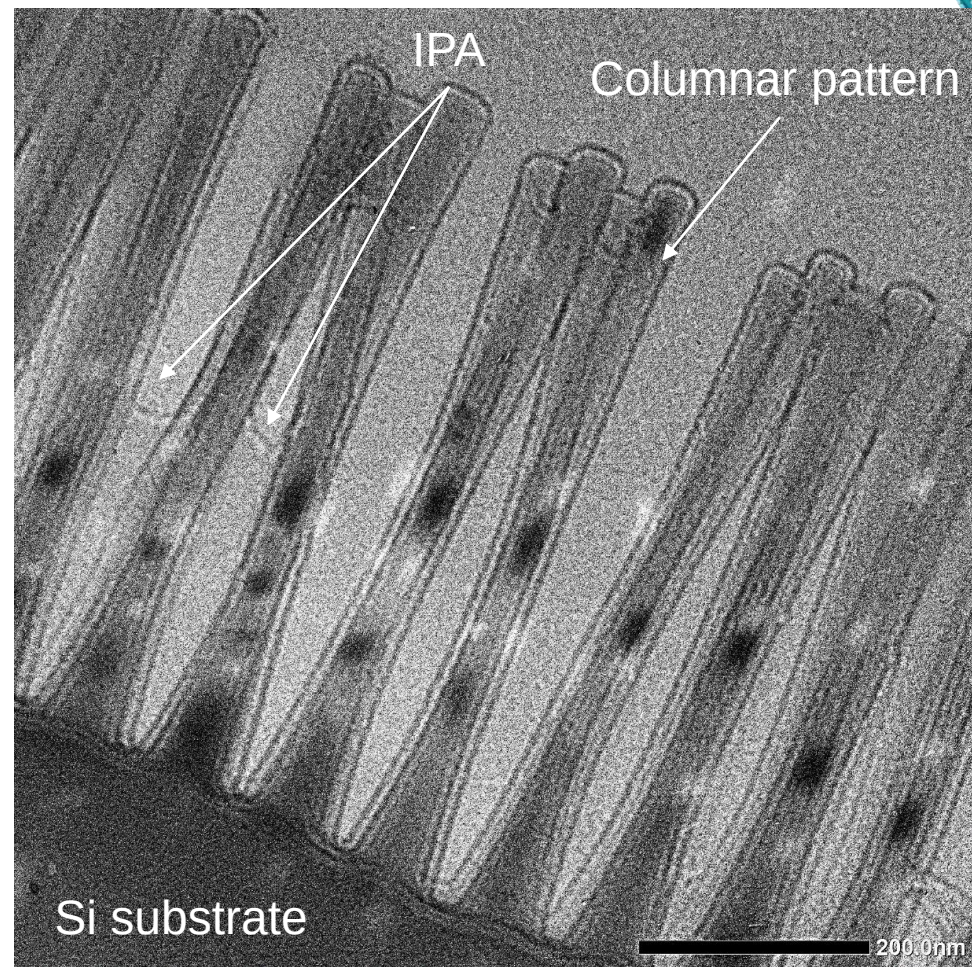


TEM



In-liquid observation holder

<https://www.protochips.com/products/poseidon-select/>

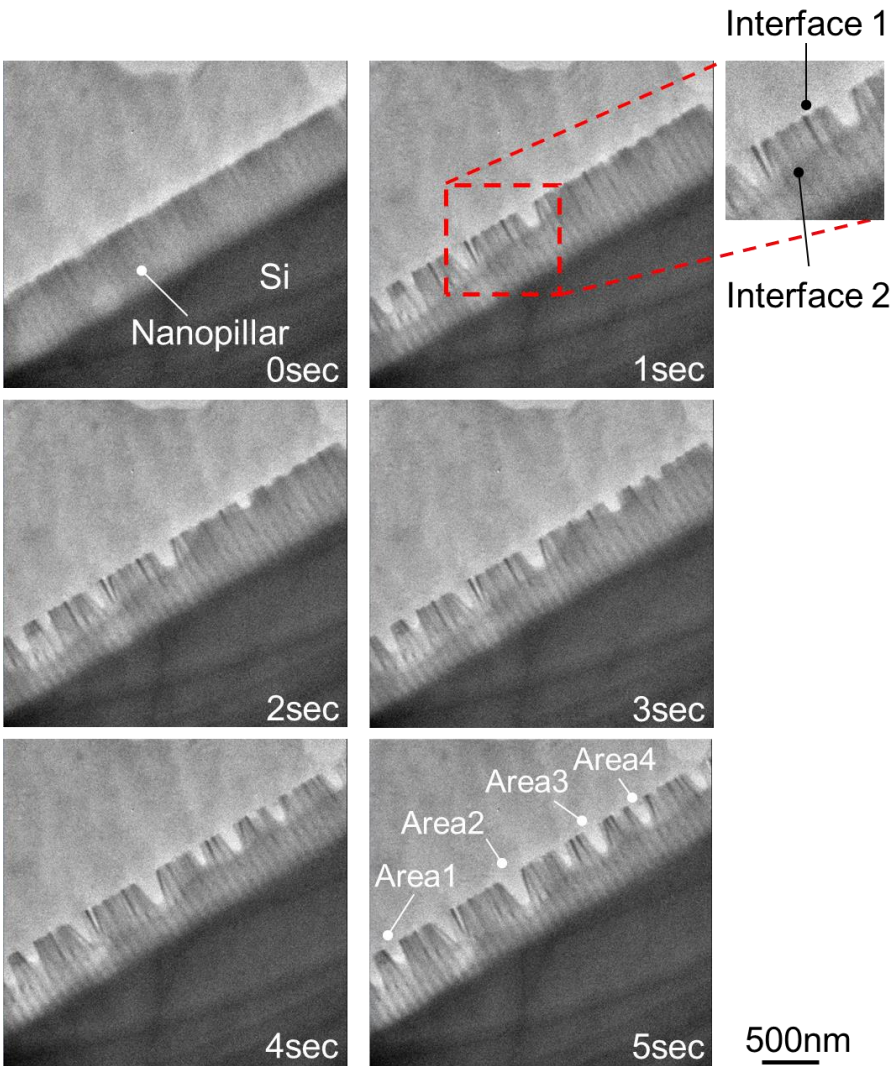


Cross-section of Si pattern after IPA drying (TEM image)

Purpose: To develop observation technology that is capable of in-liquid observation of nano-scale structures under atmospheric pressure and in real time

<https://www.screen.co.jp/news/NR220729>

In-situ TEM observation of nano-pillar collapse behavior



Source: Y. Sasaki et al., ACS Applied Nano Materials

■ Deepening the understanding of drying behavior and seeking sophistication of SCREEN's drying technology

Scientific model base development for wet equipment

◆ Leverage progress in “compute”

CFD calculation

size: μm - mm
time: sec - min



CFD calculation

size: $0.1\ \mu\text{m}$ - $100\ \mu\text{m}$
time: msec



CFD calculation

size: $10\ \mu\text{m}$ - $1\ \mu\text{m}$
time: μsec



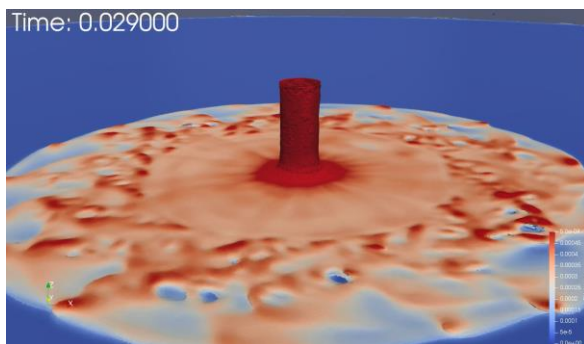
MD calculation/responsive force-field MD

size: 1 nm - 10 nm
time: nsec

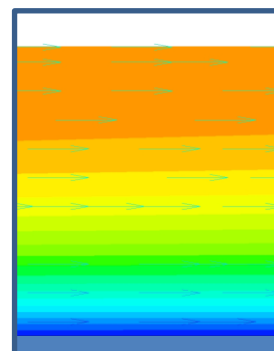


Ab initio DFT

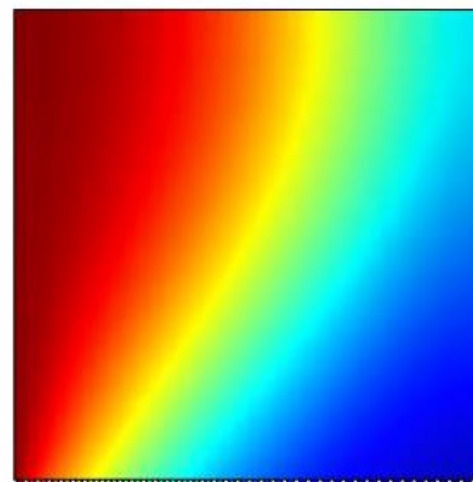
size: 0.1 nm - 1 nm
time: fsec - psec



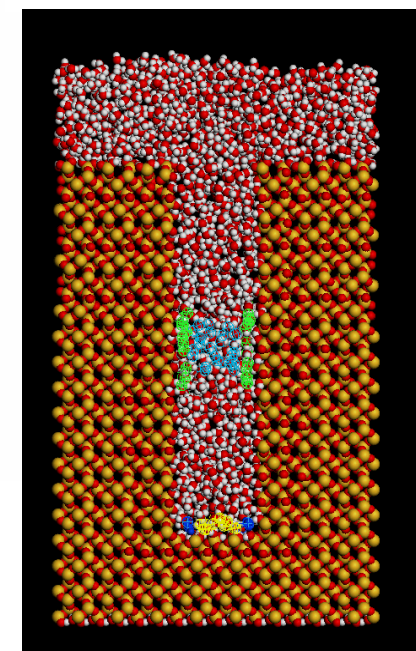
Concentration on full
wafer surface



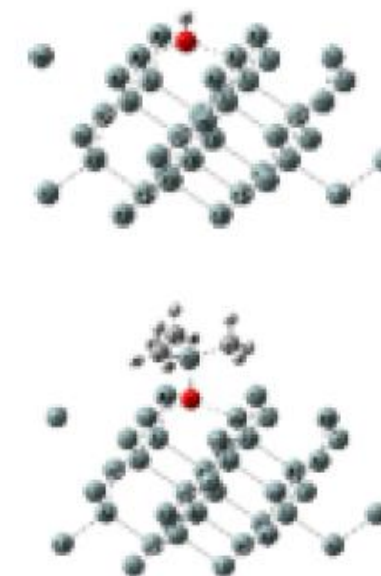
Concentration
in liquid film



Substances
near wafer



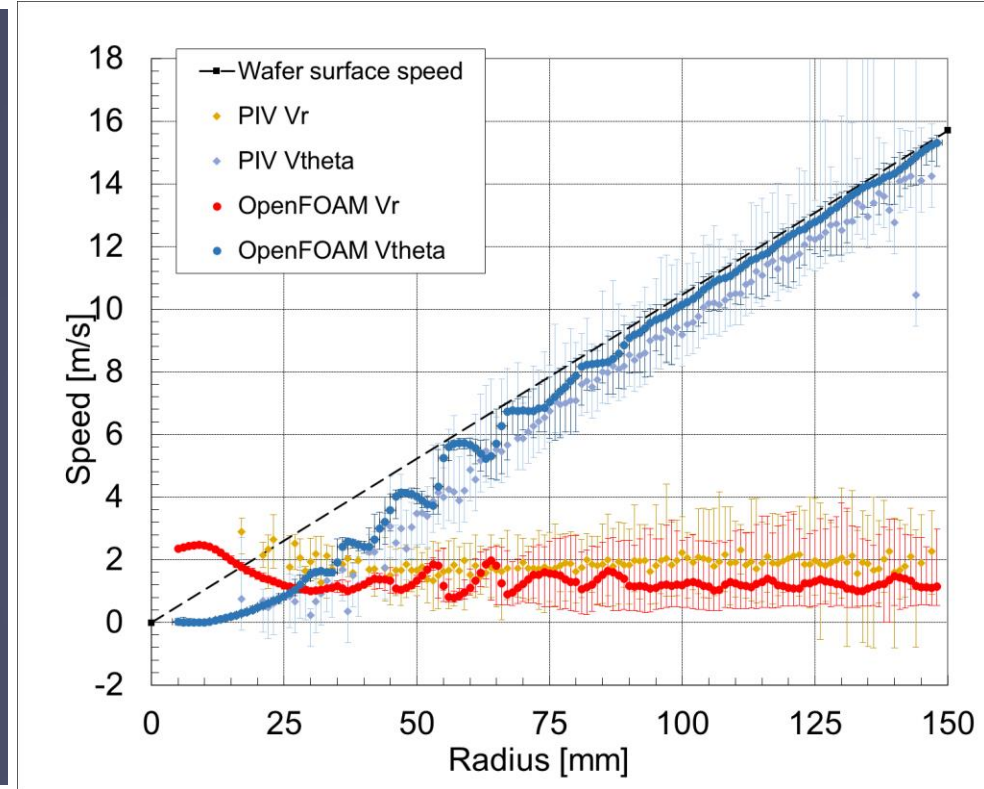
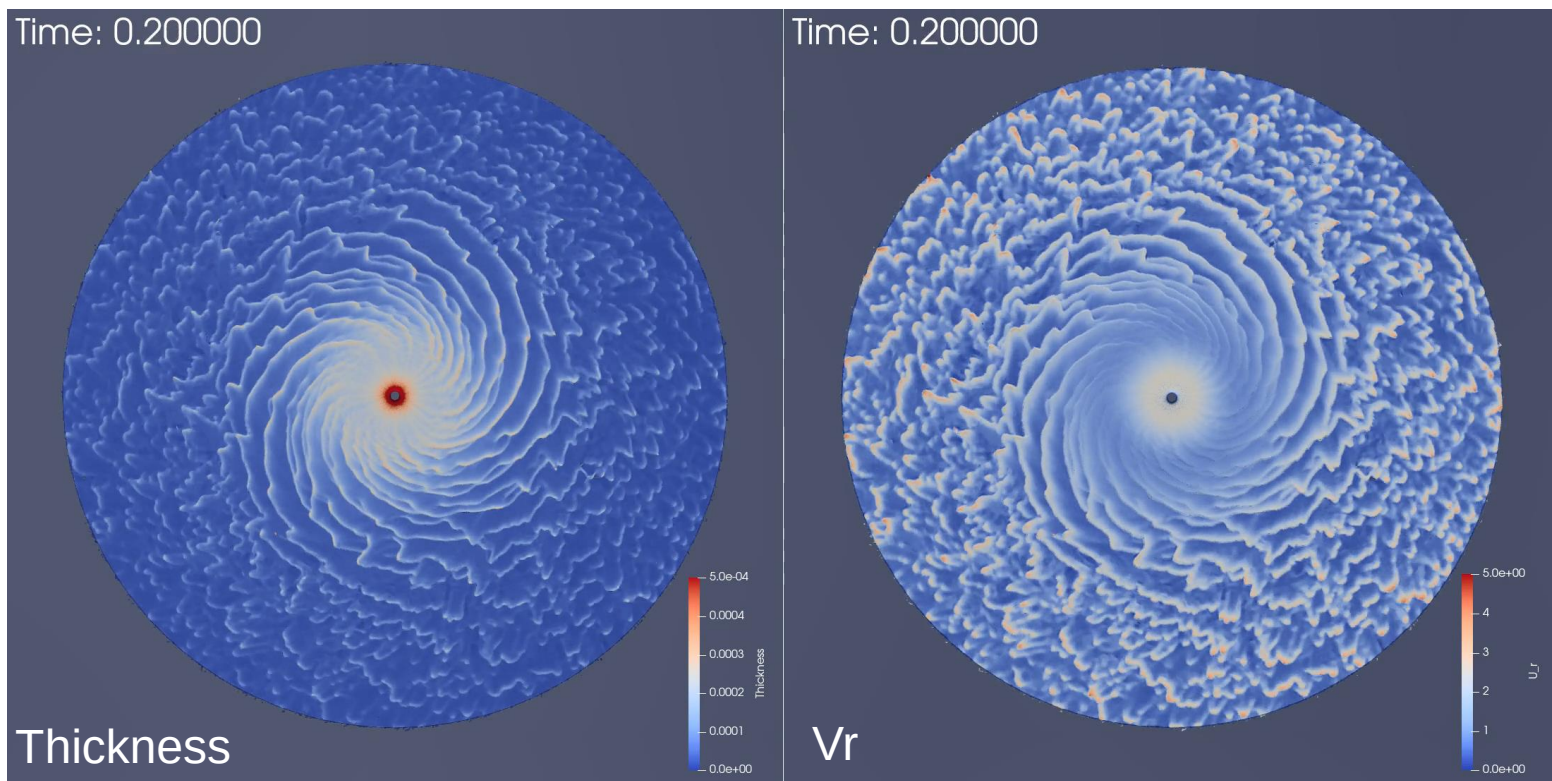
Reaction
at surface



Full scale dynamic modeling of liquid film on wafer

- ◆ Recent compute power allows full wafer modeling

Comparison of calculated and measured values



Source: M. Sato et al., 17th OpenFOAM Workshop

This achievement has been obtained through a subsidized project by the New Energy and Industrial Technology Development Organization (NEDO). Some of the results of this research were obtained using SQUID at the Cybermedia Center, Osaka University..

Summary

- ◆ **Sustainability is a critical factor for both device manufacturers and equipment manufacturers.**
- ◆ **Defect reduction by wet-cleaning technology is the most effective pathway for reducing CO₂ emission in advanced nodes.**
- ◆ **Scientific model base development for wet cleaning technology becomes relevant thanks to recent “compute” progress. This positive feedback loop is the key to further growth of the “semiconductor industry”.**

ADVANCING
GLOBAL TECHNOLOGY
& INNOVATION

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Innovation for a Sustainable World

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