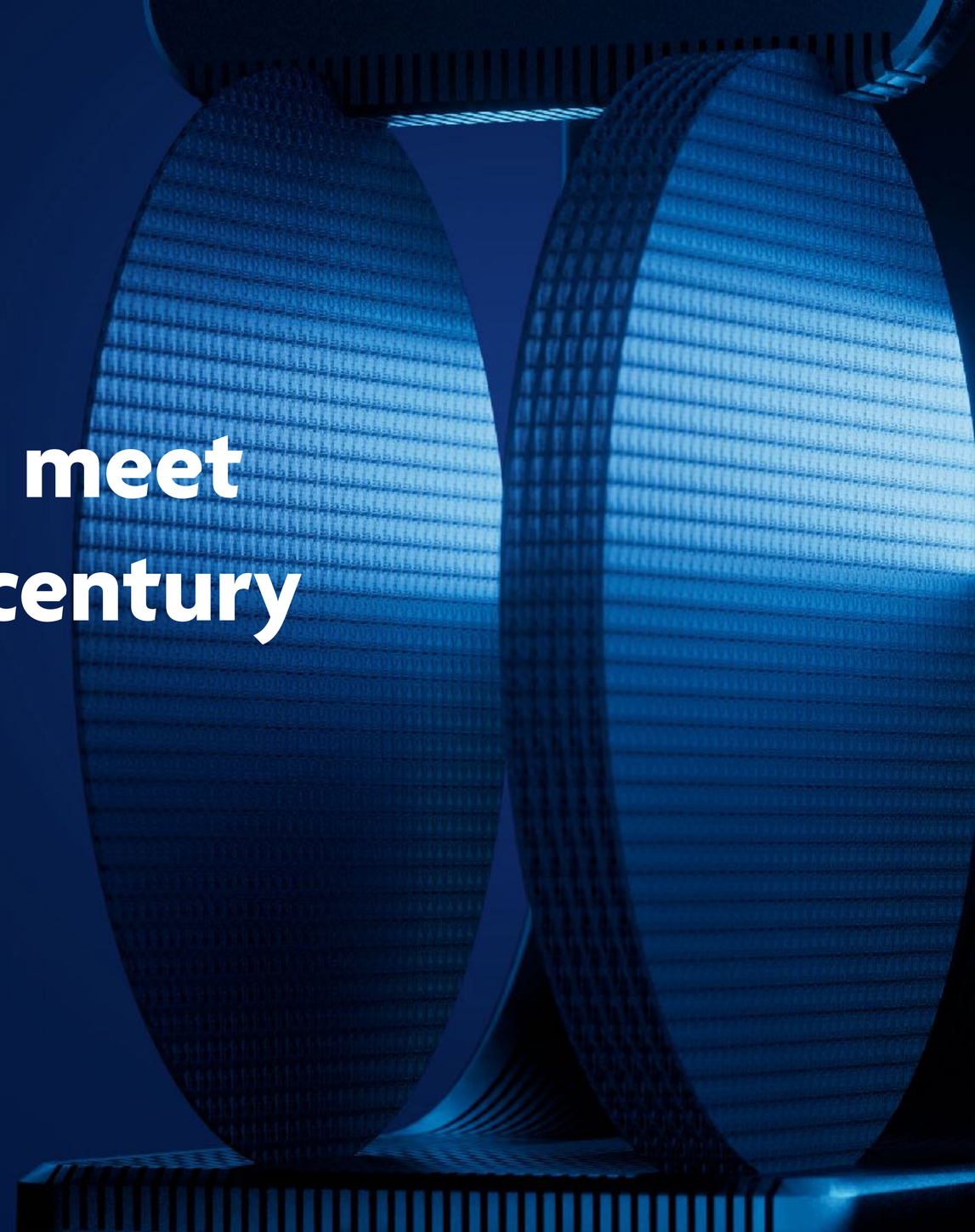
Deep tech: the lodestar to meet the challenges of the 21st century

Luc Van den hove, President and CEO imec

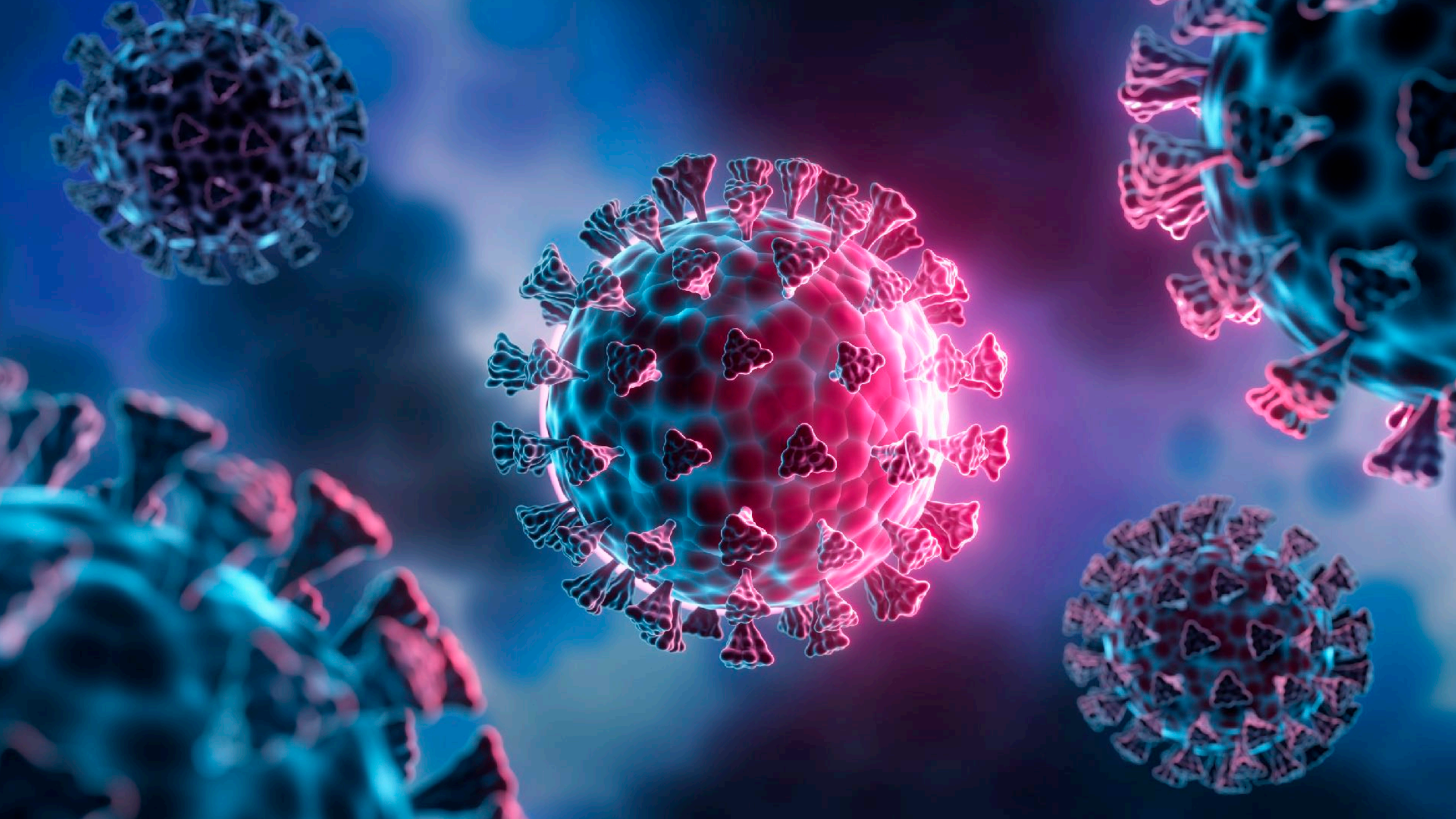
imec

embracing a better life



The world is facing a major storm










Escalating geopolicial tensions



Increased awareness of the importance of semiconductors



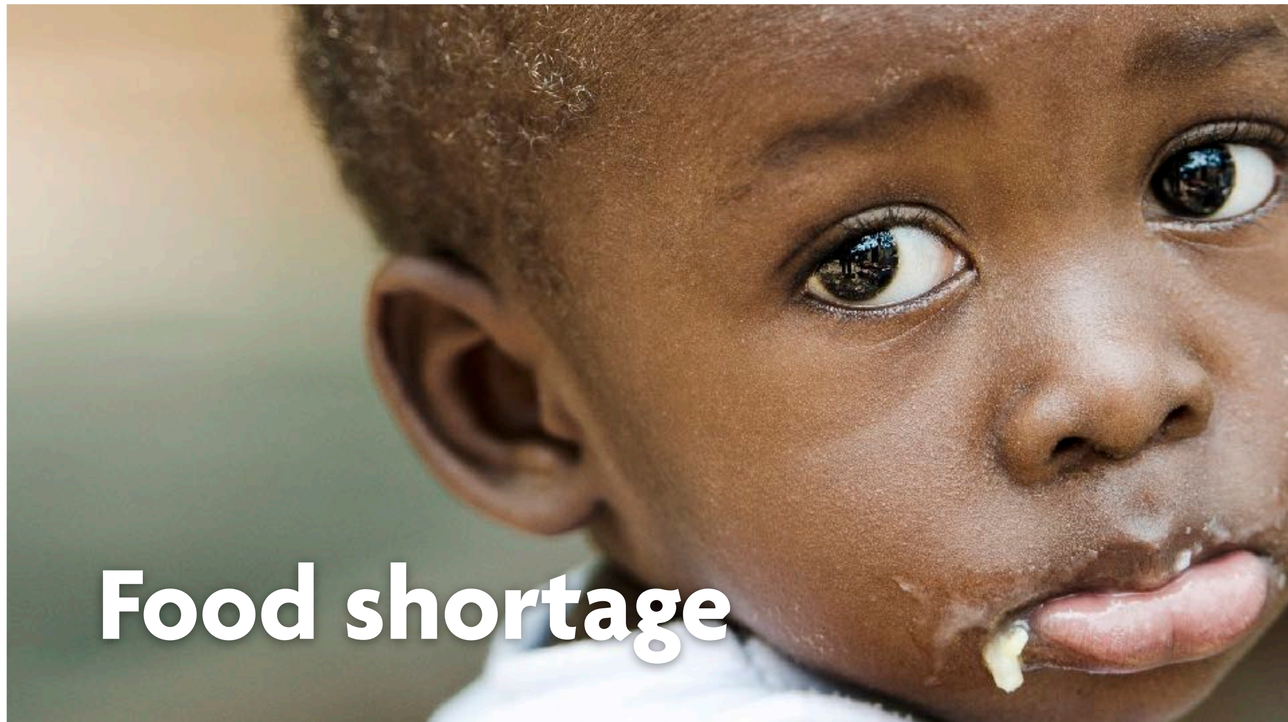

Microchips have impact everywhere


Deep-tech solutions
will be essential to address
many future challenges


Climate crisis

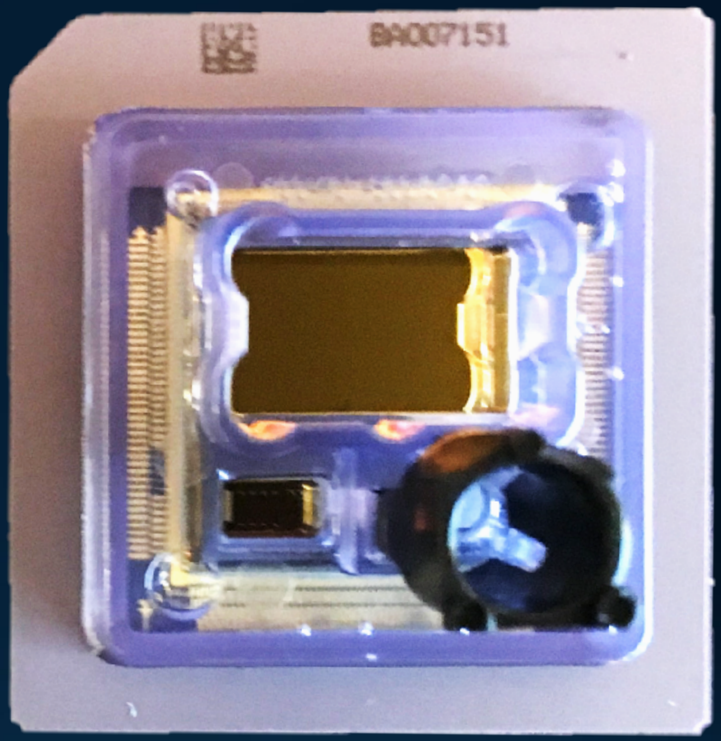

Pollution

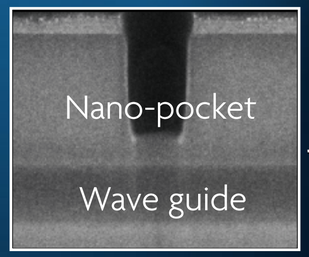

Health

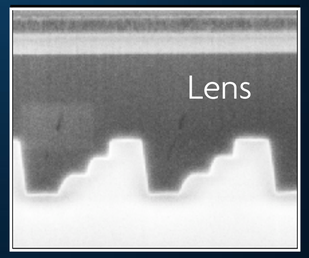

Food shortage

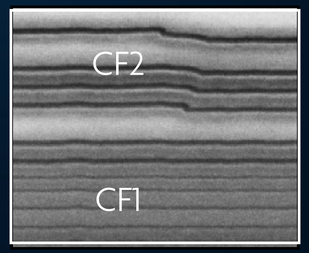

COVID-19 **genome sequenced**
in a matter of **weeks**

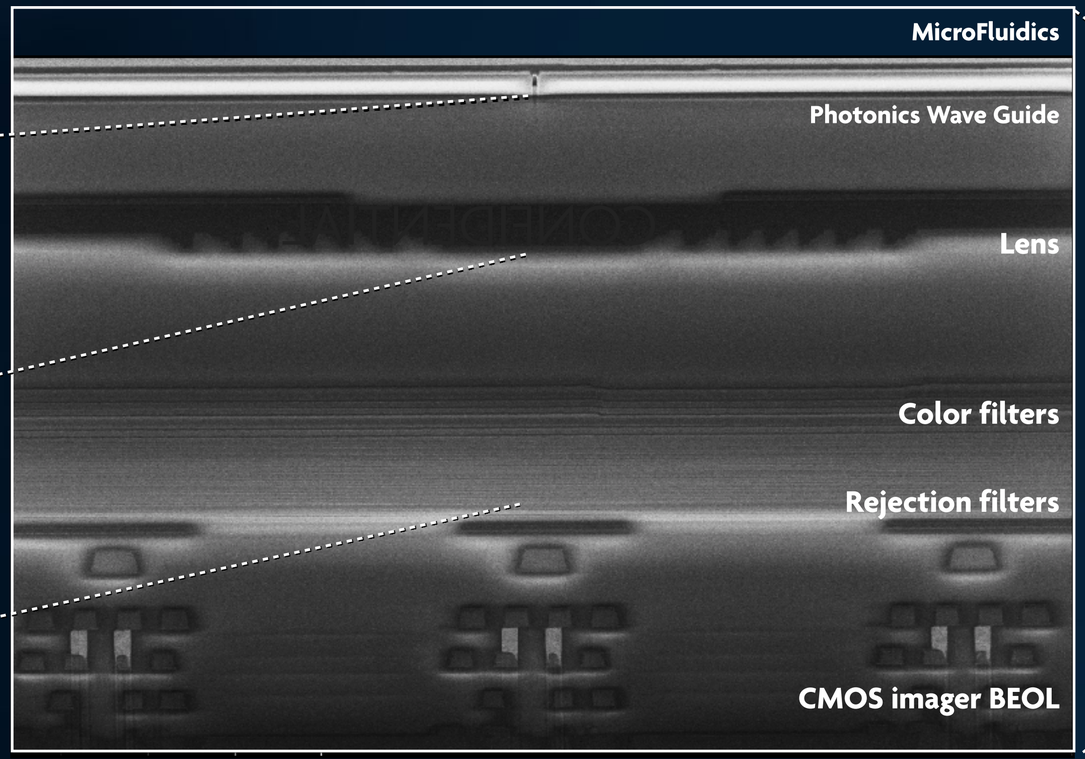
Accelerating genome sequencing by **leveraging** the **power of silicon**

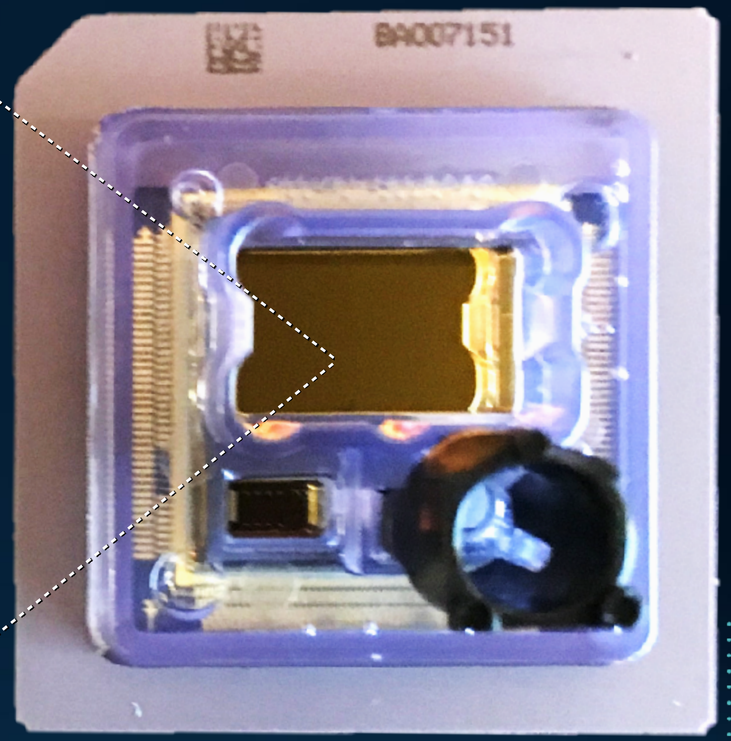












Highly parallelized single molecule DNA sequencer

On a single chip


mRNA technology was
ready to be **deployed**



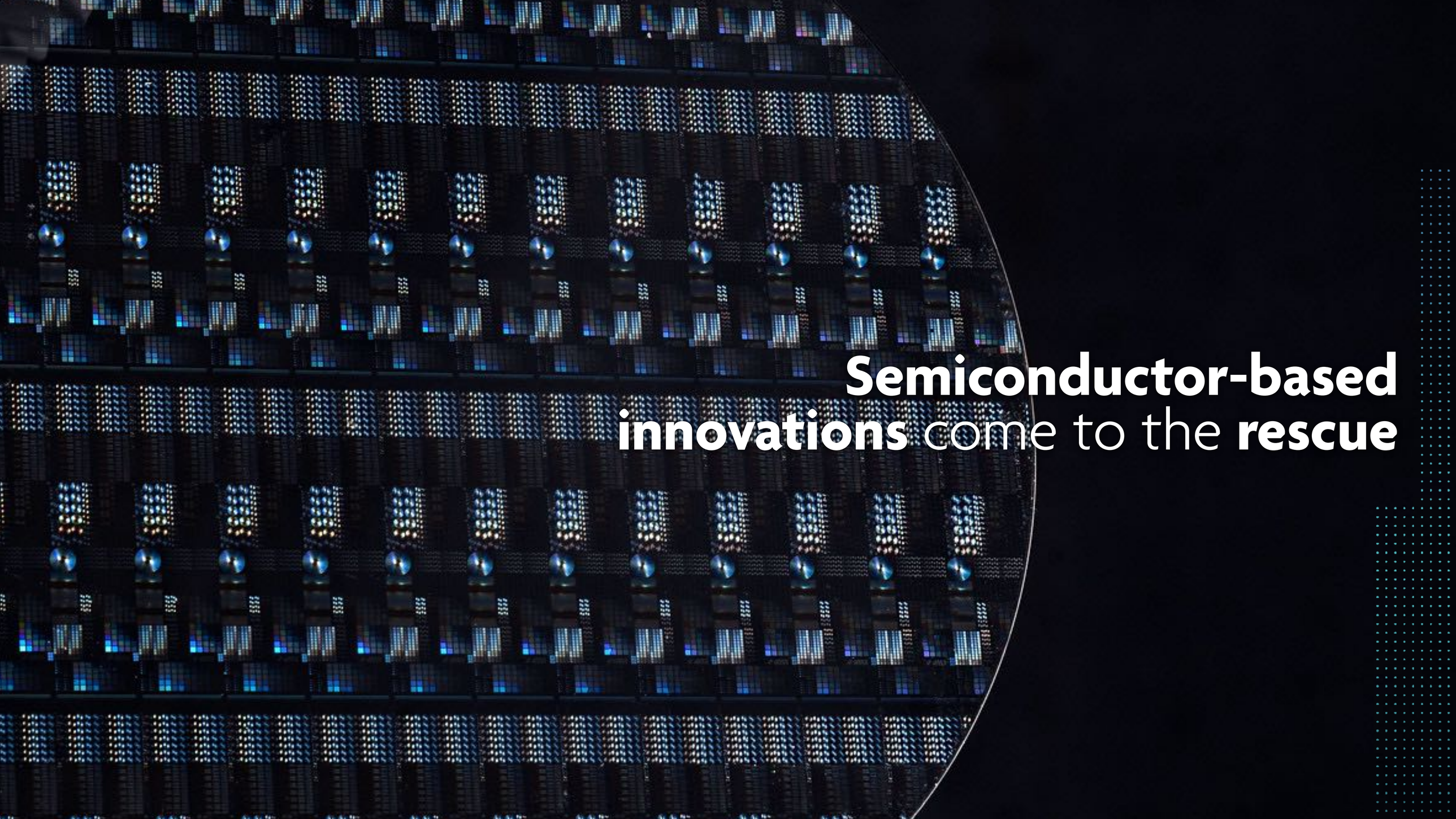
discovery

production

regulation



mRNA vaccine: triumph of science but ...



Semiconductor-based innovations come to the **rescue**



automation

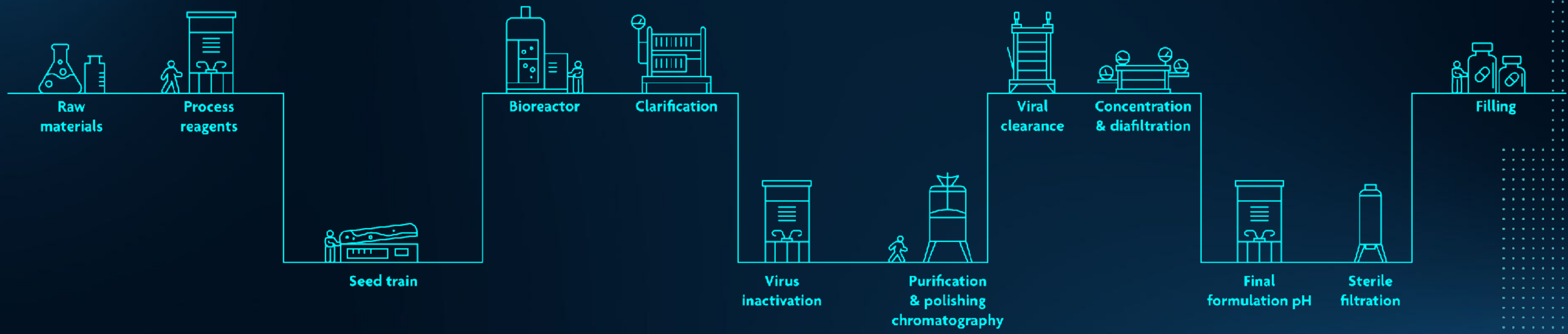
fluidics

robotics

sensor technology

AI

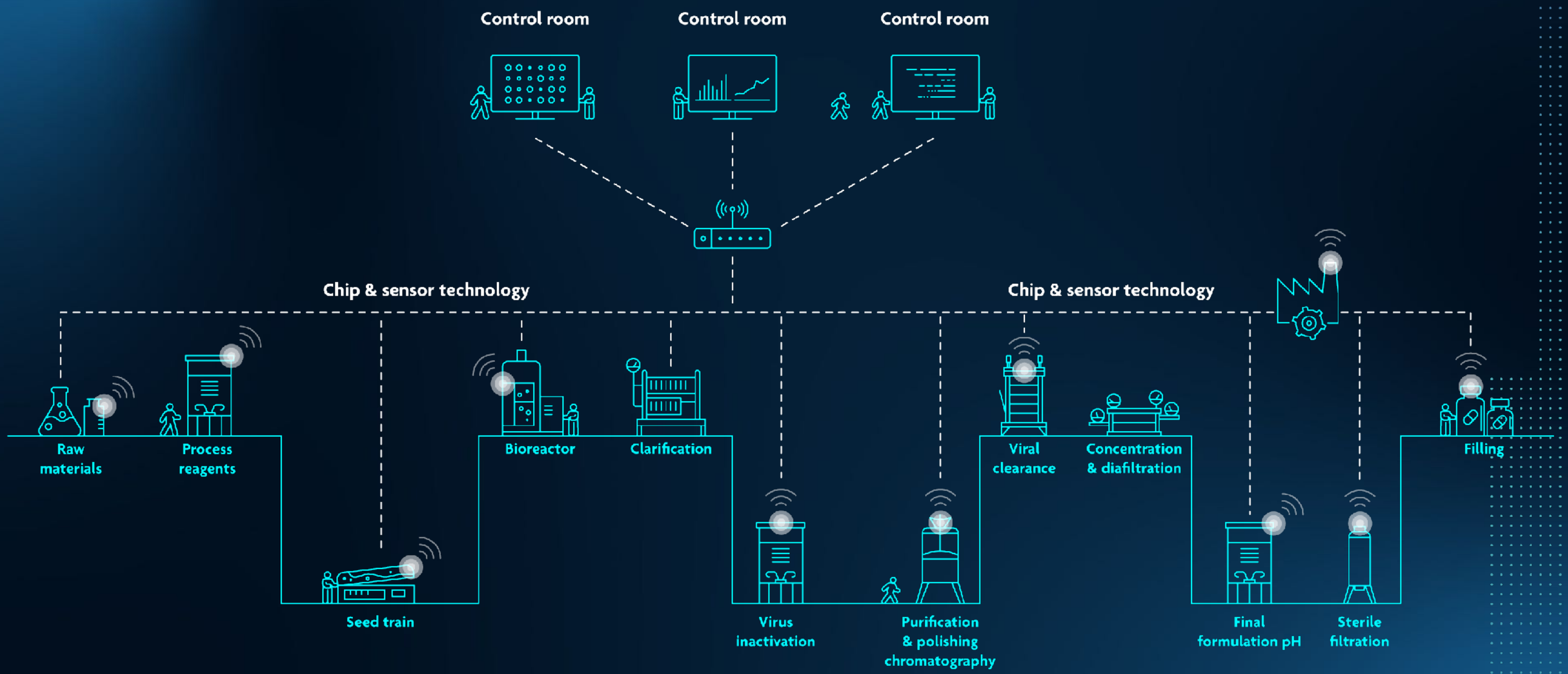
Upstream and downstream monitoring using process analytical technologies



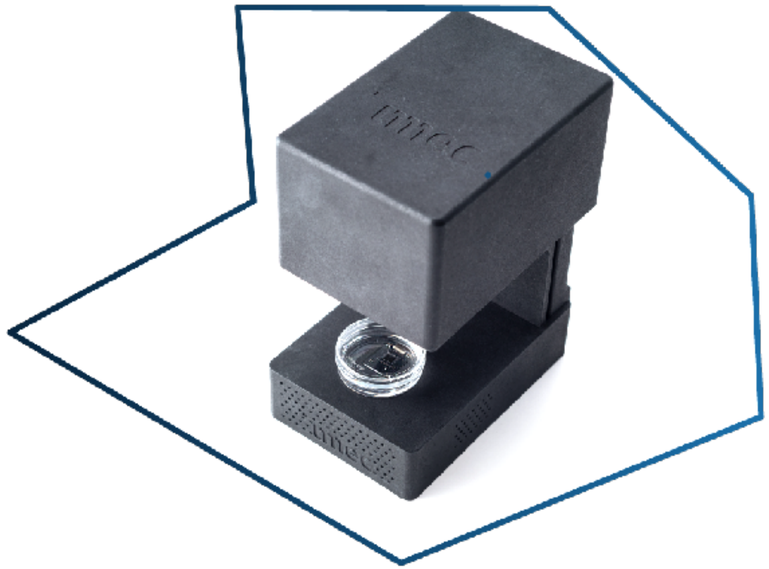
Manual monitoring



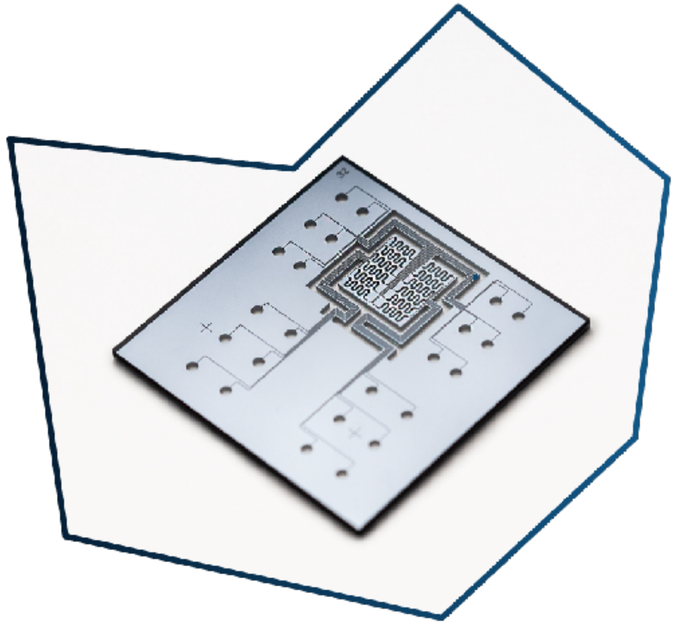
Chip technology enables on-line and in-line testing



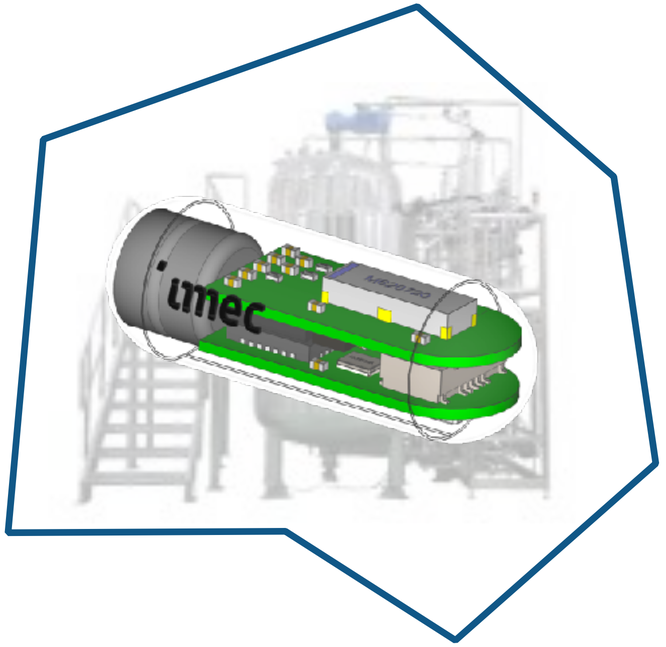
Continuous in-line / on-line monitoring



lens-free imaging

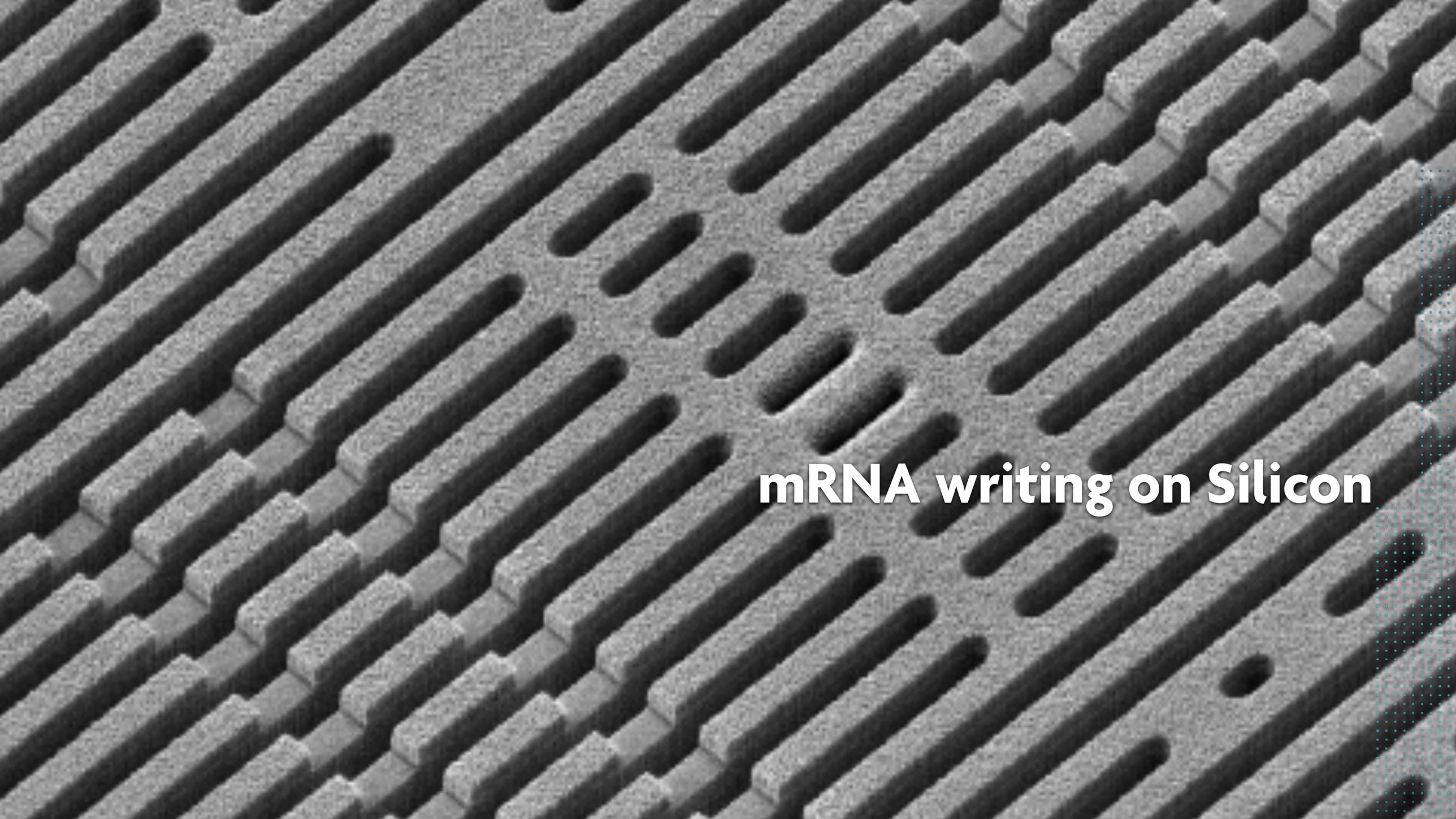


on-chip PCR

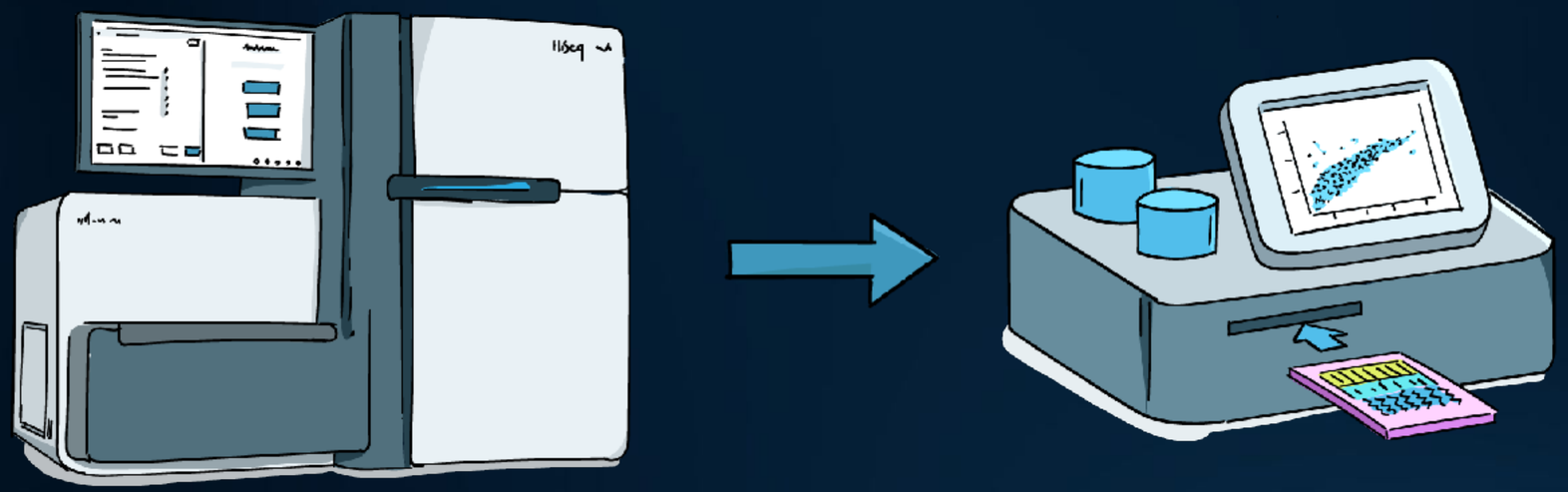


PATcube sensor


mRNA
a code, a sequence of bases

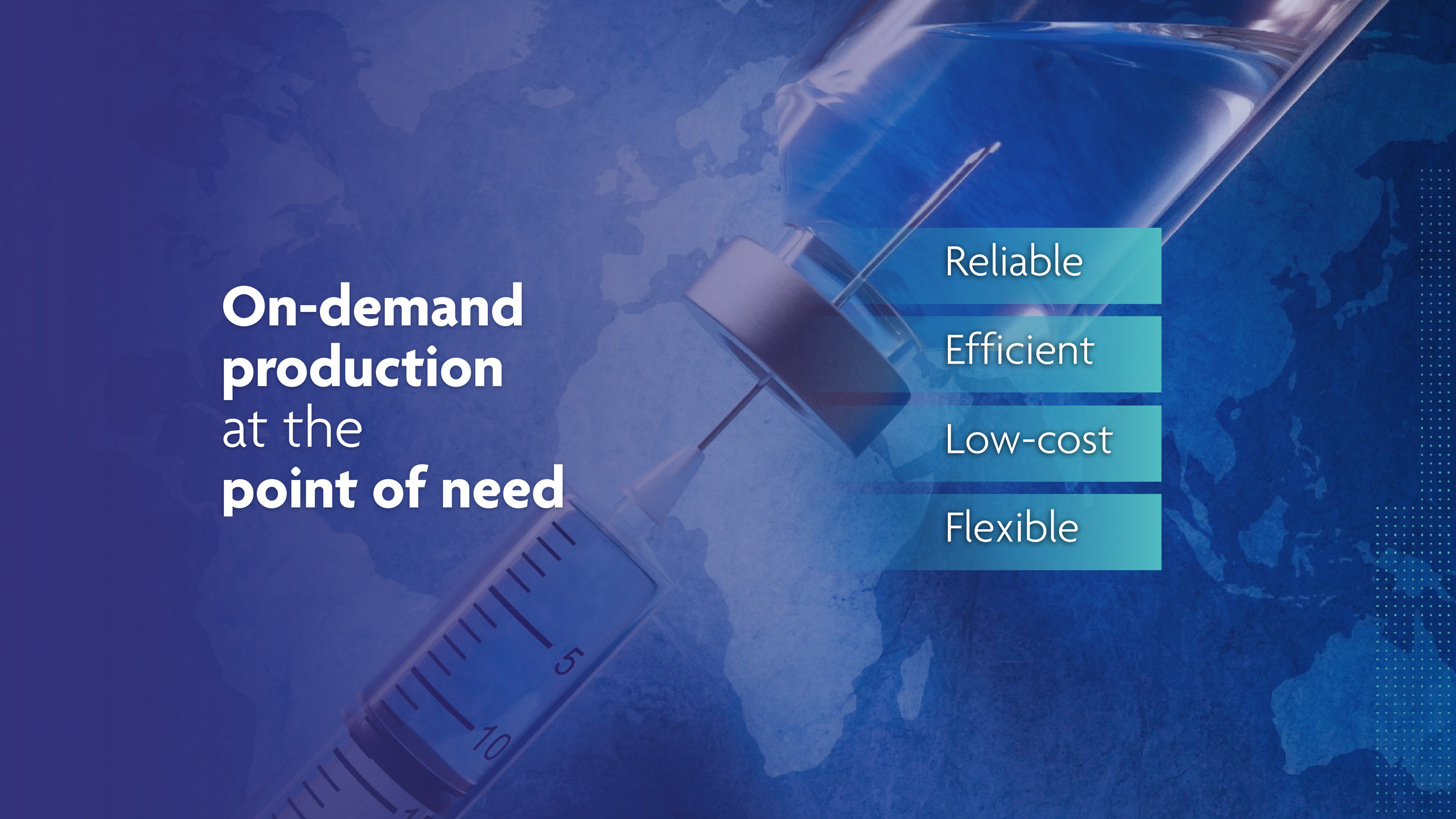

mRNA writing on Silicon

mRNA is a designable drug



Genome

Synthesis



On-demand production at the **point of need**

- Reliable
- Efficient
- Low-cost
- Flexible

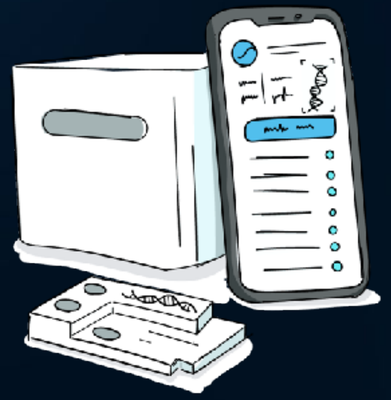
Paving the way for affordable personalized therapies



Medicine enters the digital era



Patient-physician interaction



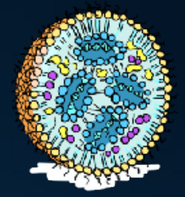
Point-of-care data + genome



Next-generation
deeptech-enabled
pharma/biotech



Point-of-care synthesis

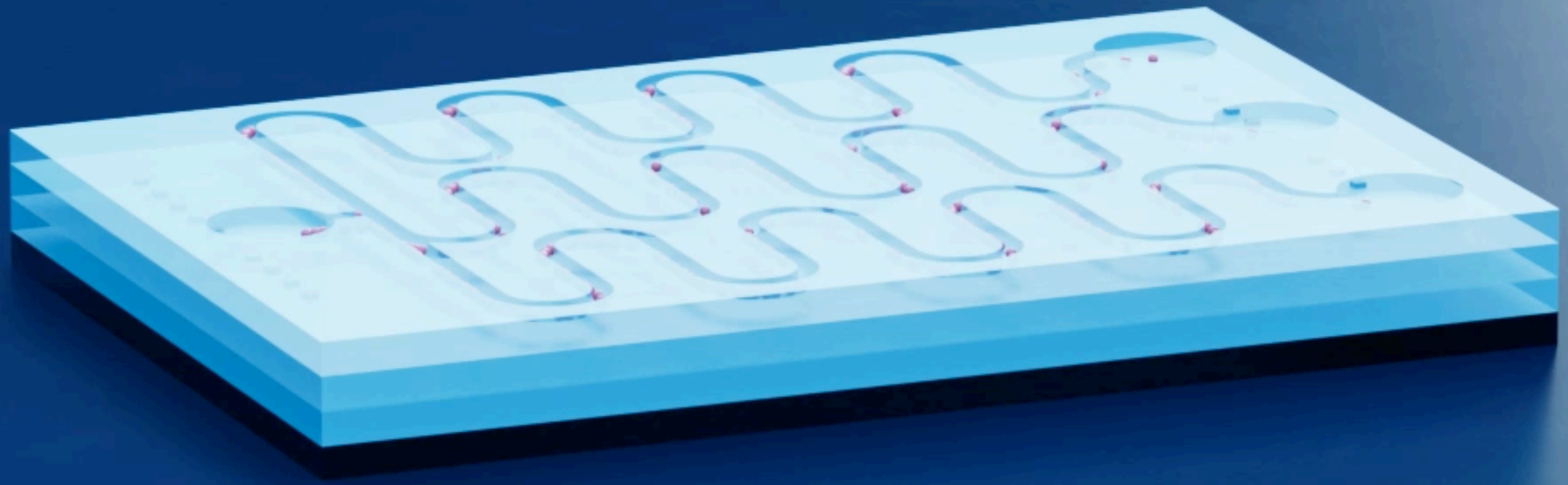


mRNA therapeutic



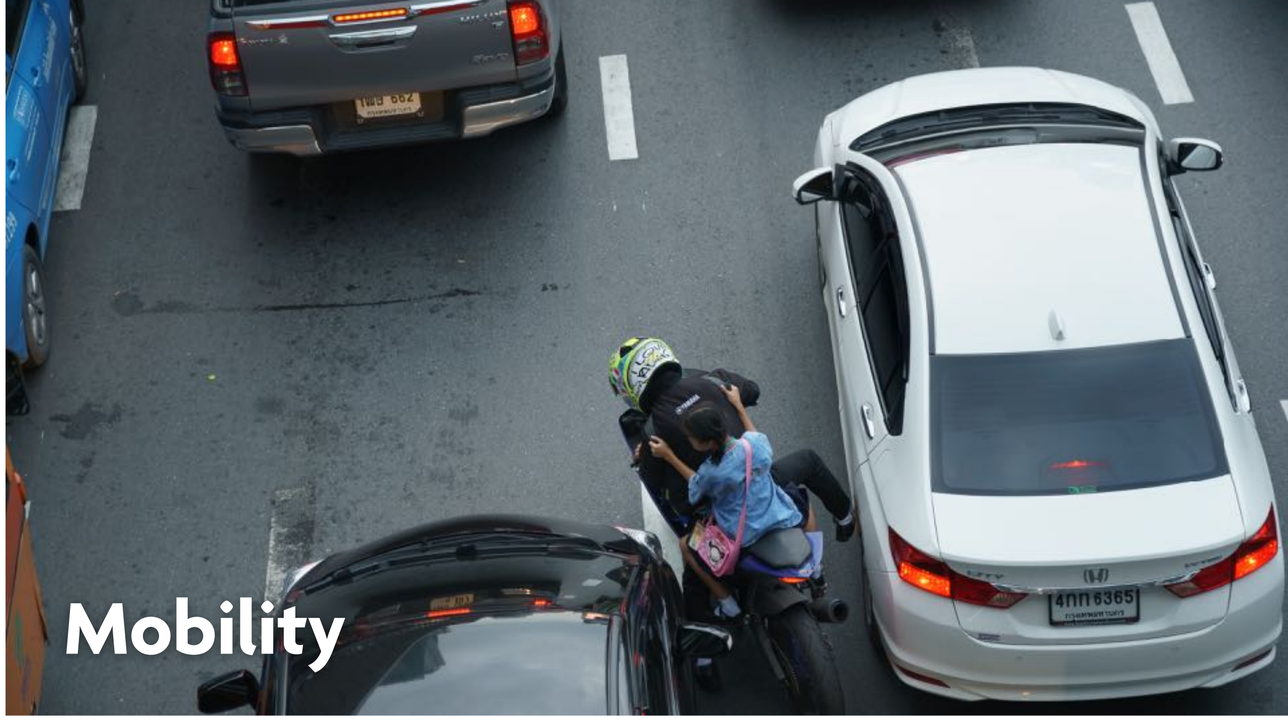
Administration

Si-based medical device platform




Exponential increase of
data generation


Climate crisis


Mobility


Health

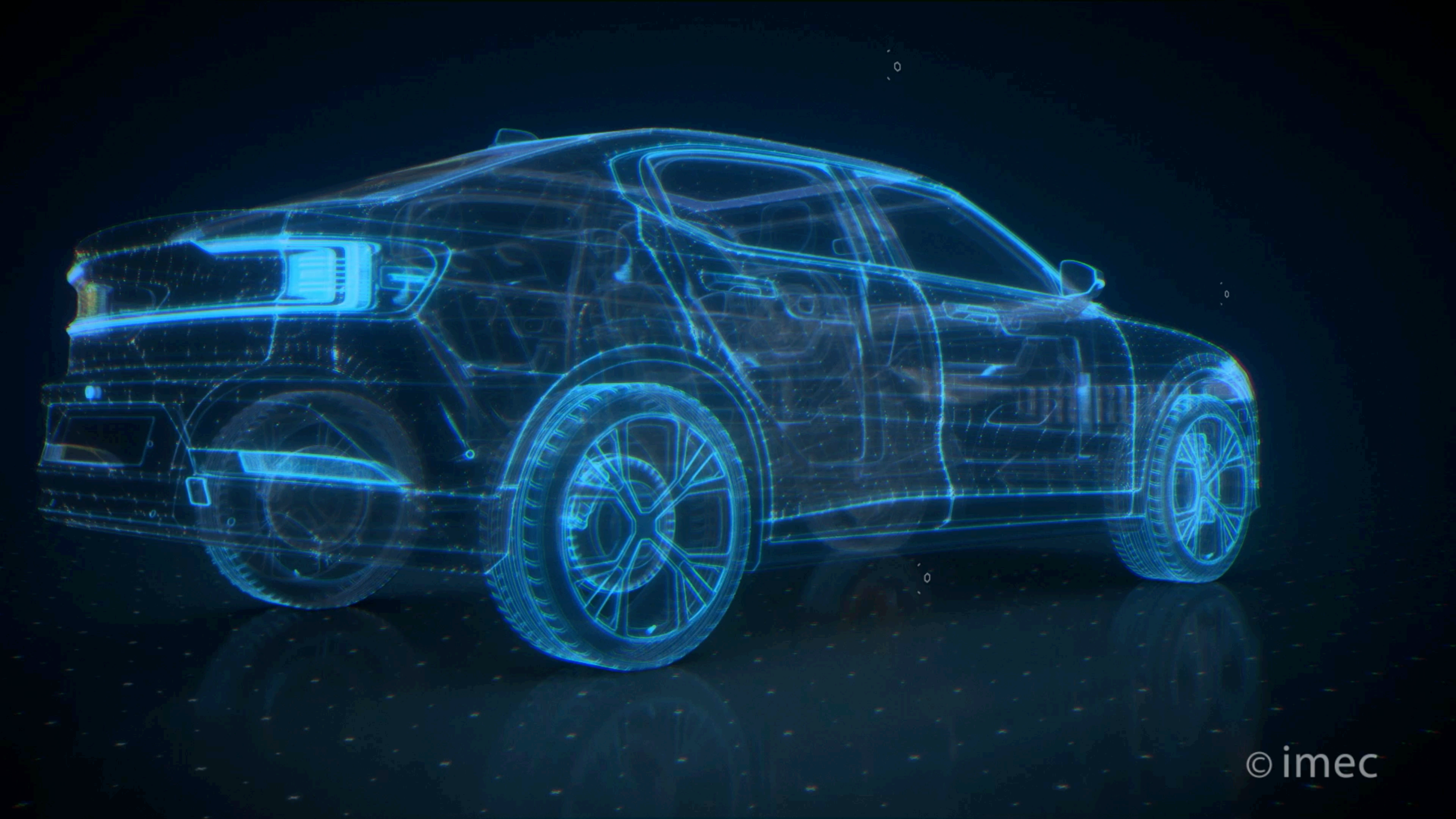

Food shortage



Mobility

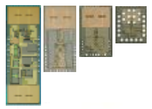


Vision zero strategy
increasing safe, healthy and equitable mobility for all


© imec

SENSORS

Radar



Vision



Lidar

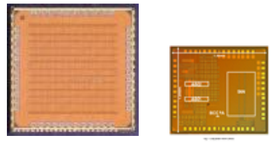


ALGORITHMS

Co-optimize sensors with AI within accuracy/cost/ power/latency/size constrained space

EDGE AI

CNN/SNN accelerators



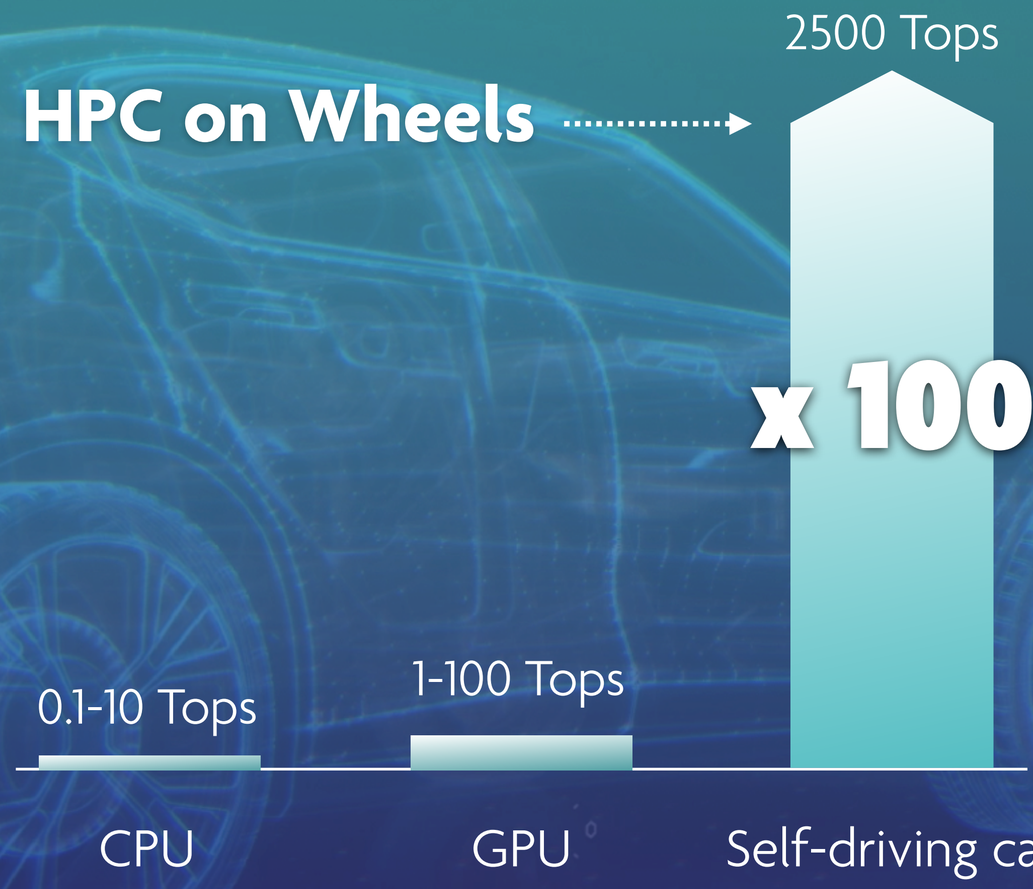
DATA FUSION

Automotive Expertise

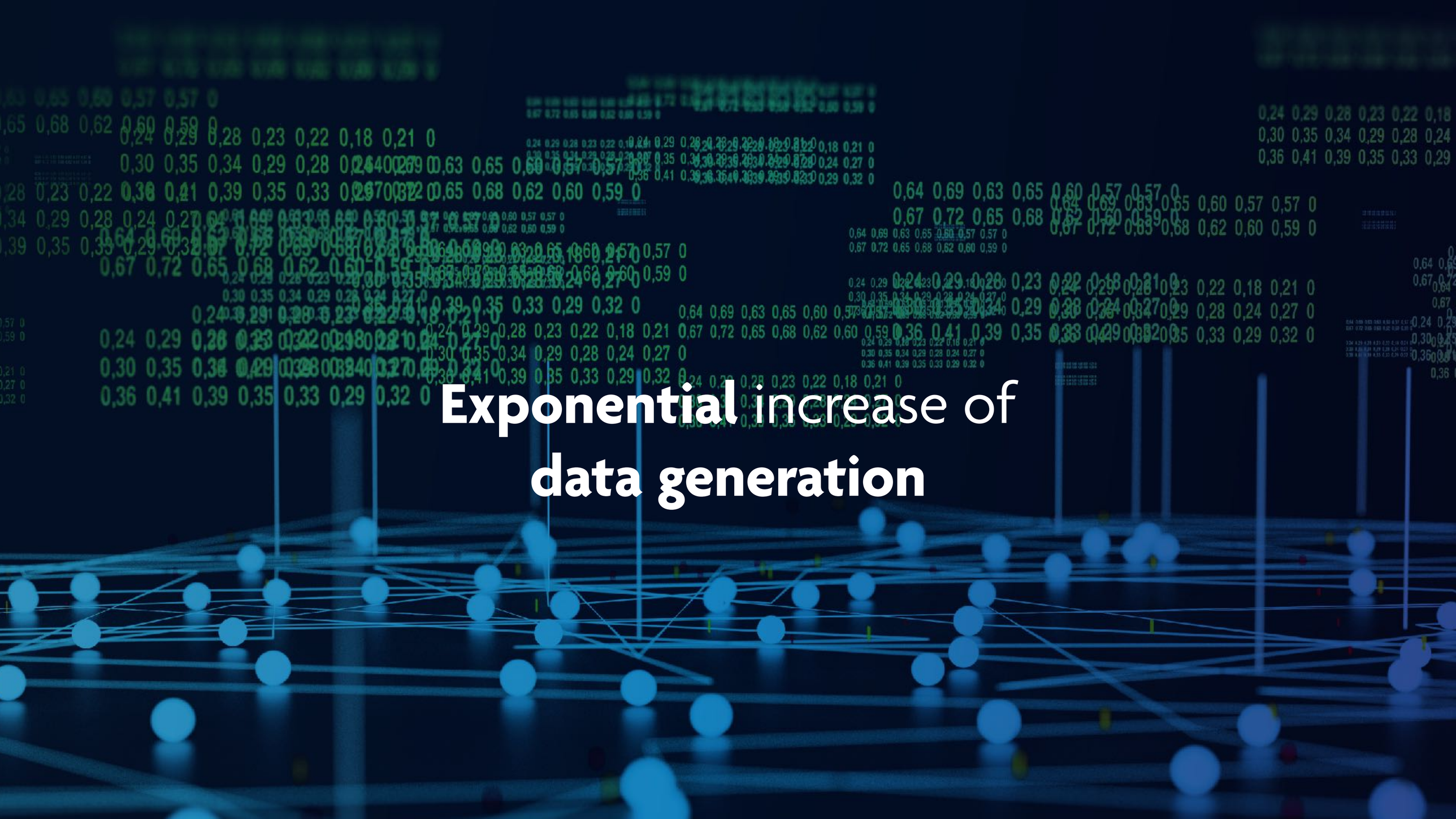
© imec

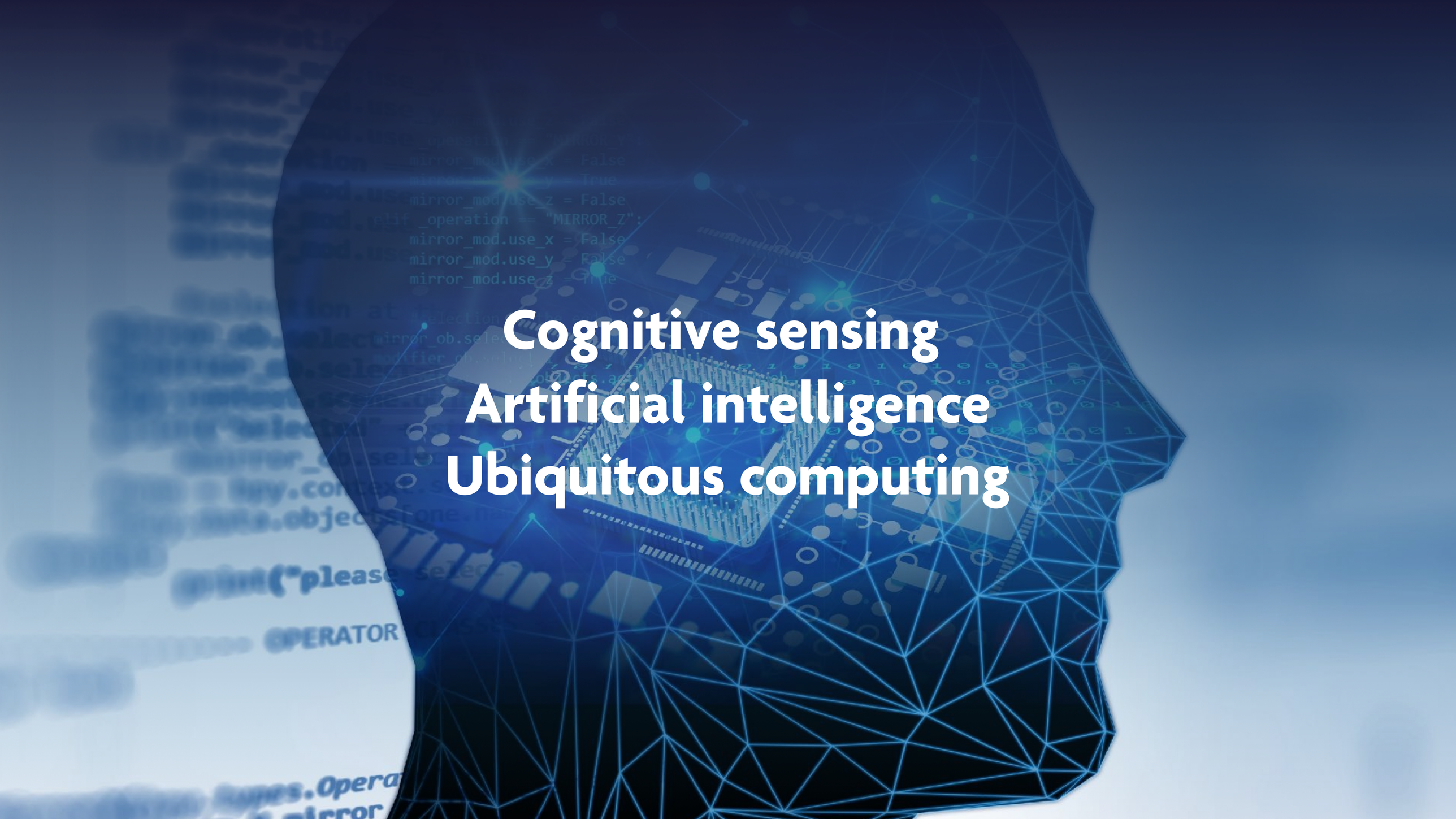
Required compute power for autonomous driving

HPC on Wheels

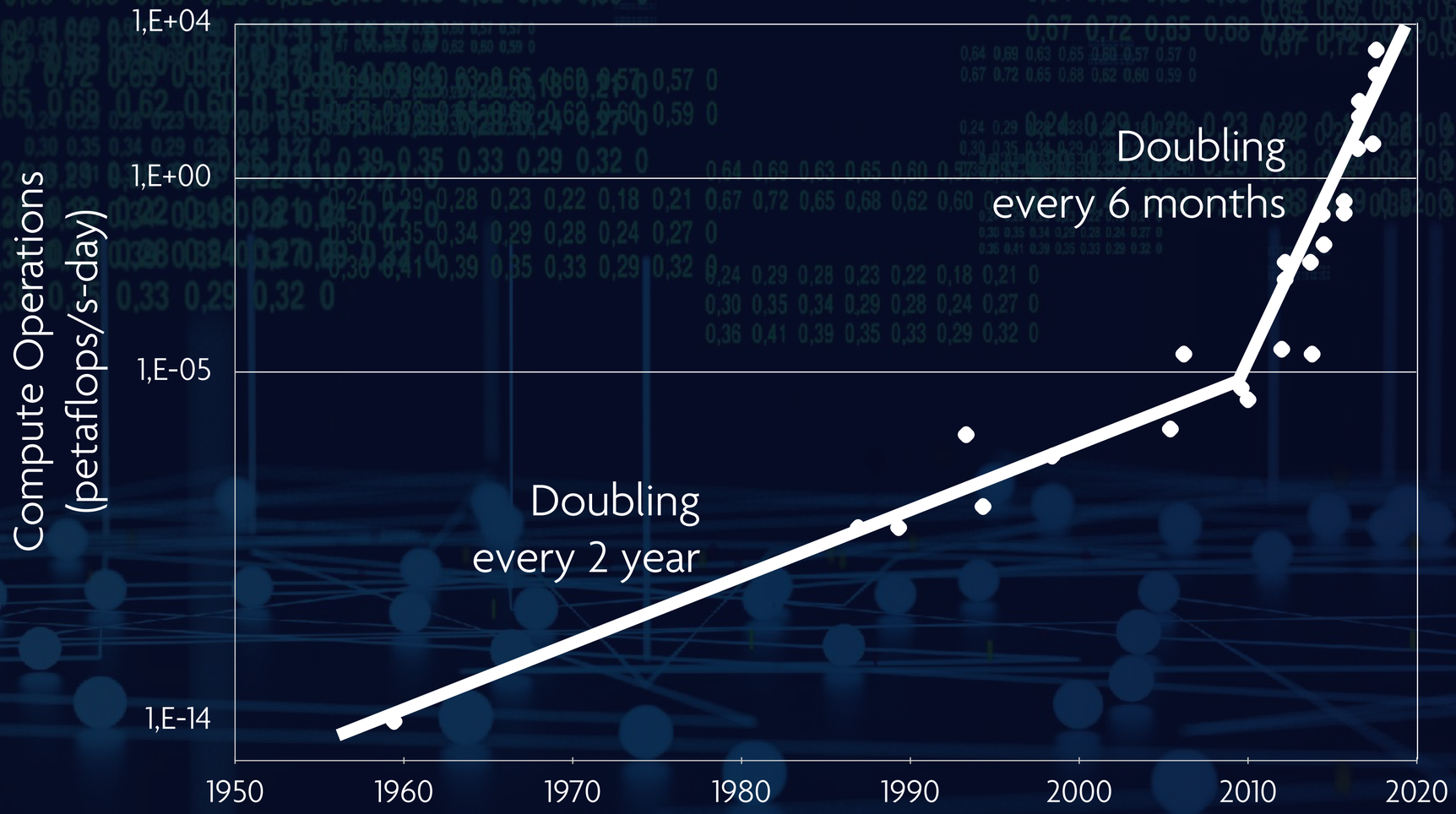


© imec


Exponential increase of
data generation


Cognitive sensing
Artificial intelligence
Ubiquitous computing

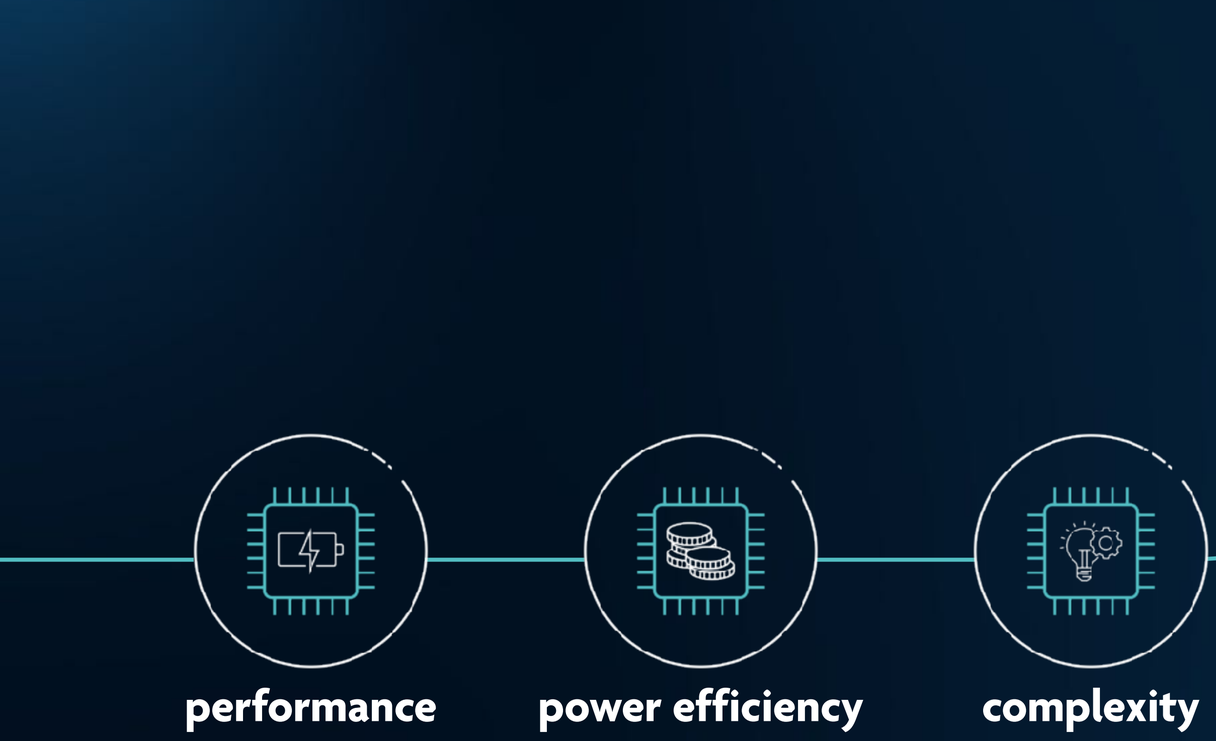
Compute needs for artificial intelligence



Data source: https://openai.com/blog/ai-and-compute/

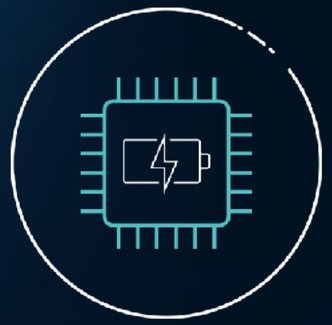
The need for a more aggressive semiconductor roadmap

100x
improvement

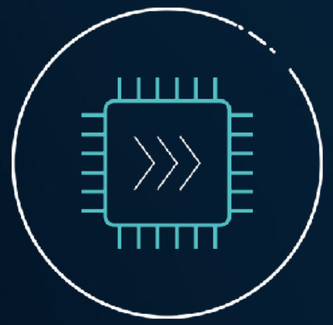




traditional scaling



reduced power



increased performance



increased density

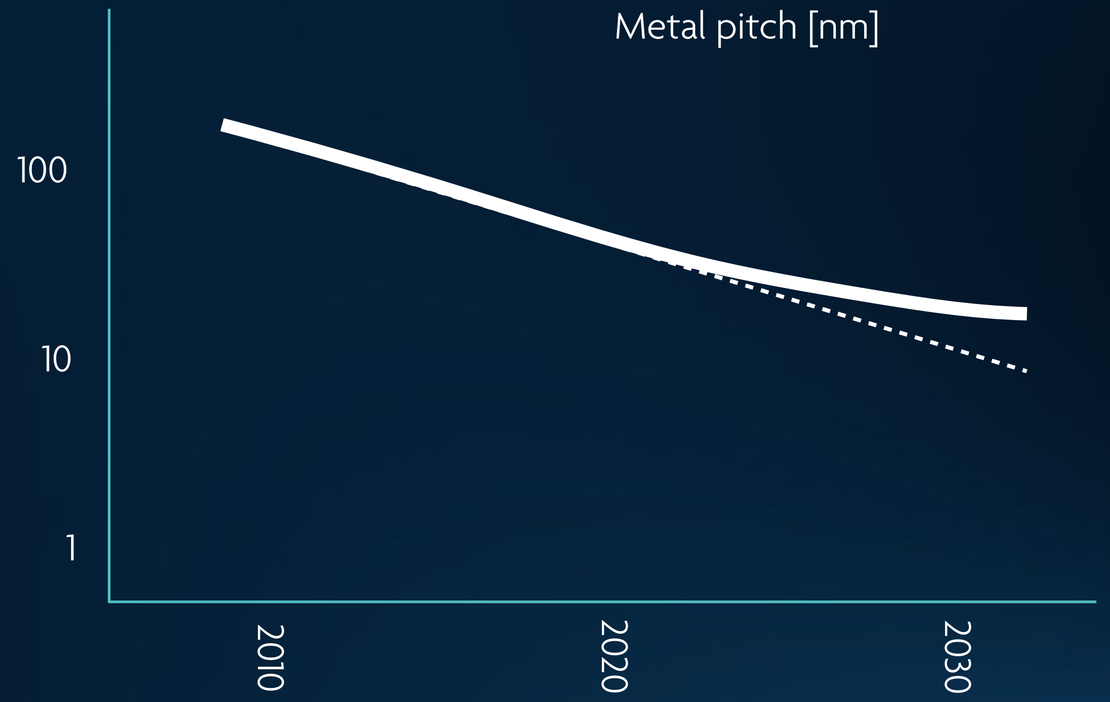


reduced cost

Scaling wall



increased density

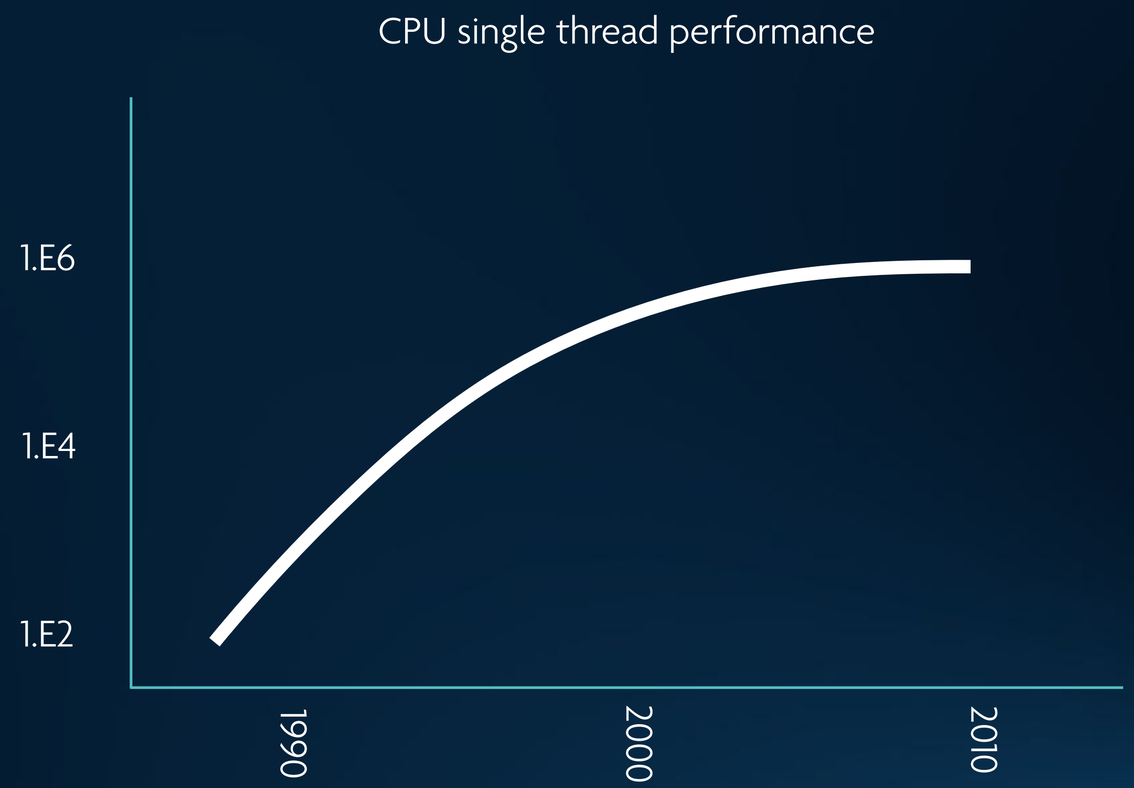


Pure lithography-enabled scaling is slowing

Performance wall



increased performance

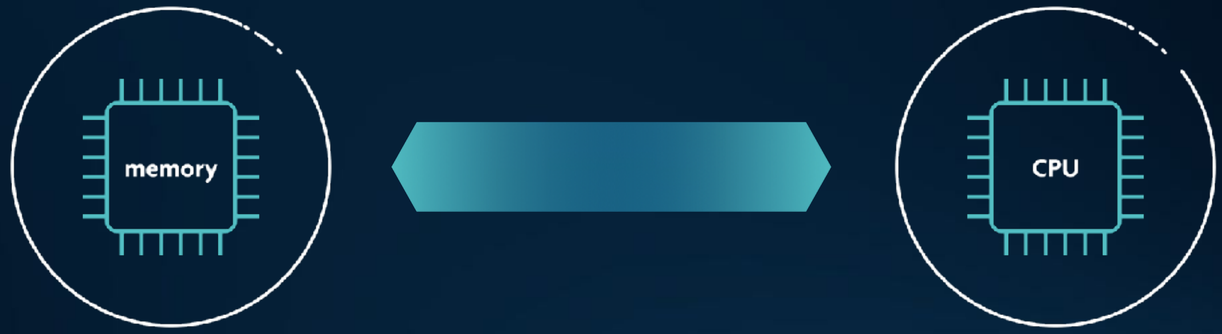


Increase of single-device performance and single-thread CPU performance diminishes

Performance wall



increased performance

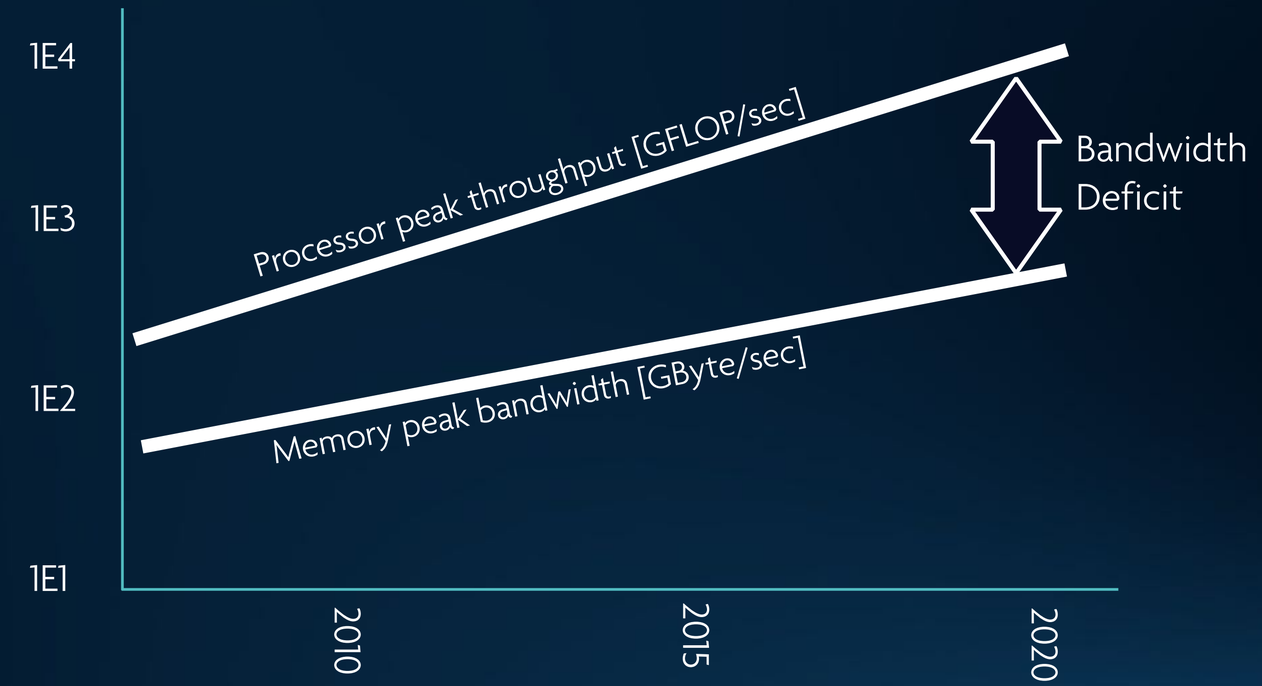


System performance becomes increasingly dominated by data path limitations between core and memory (Memory wall)

Performance wall



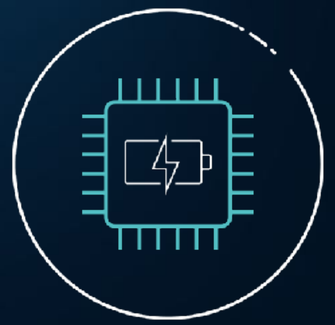
increased performance



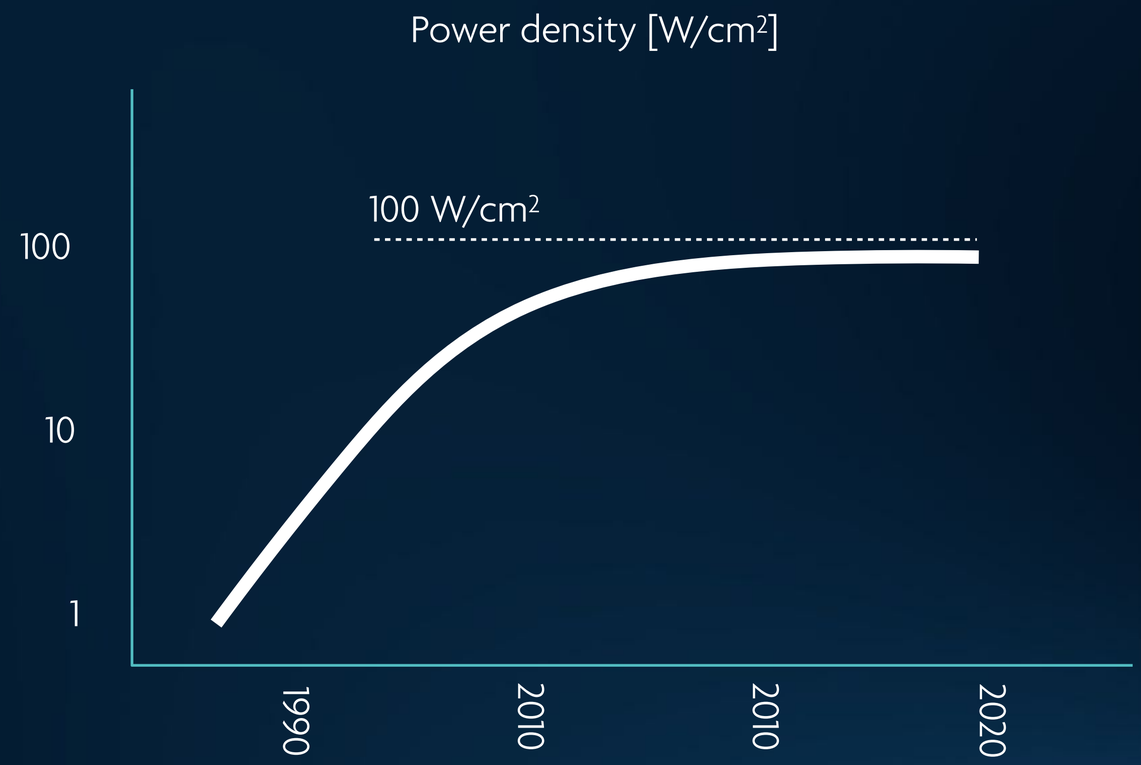
System performance becomes increasingly dominated by data path limitations between core and memory (Memory wall)

Ref: K. Akarvardar

Power wall



reduced power

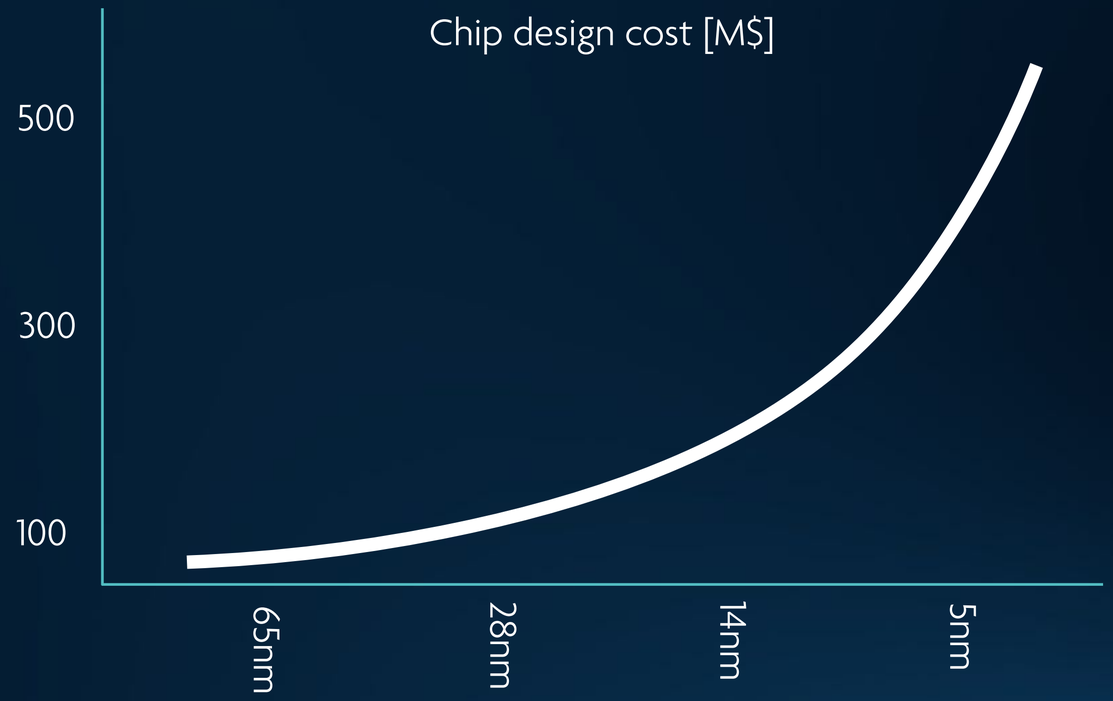


At chip level, bringing increasing power in and extracting increasing heat out of the chip/package is limited

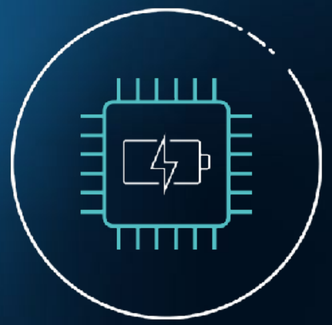
Cost wall



reduced cost



Exploding cost of manufacturing, design and process development



power wall



performance wall



scaling wall



cost wall

Breaking down **‘the Walls’**

Moore’s law **will not stop**

1



Shrink the switch

2



The next switch

3



The third dimension

4



Paradigm change

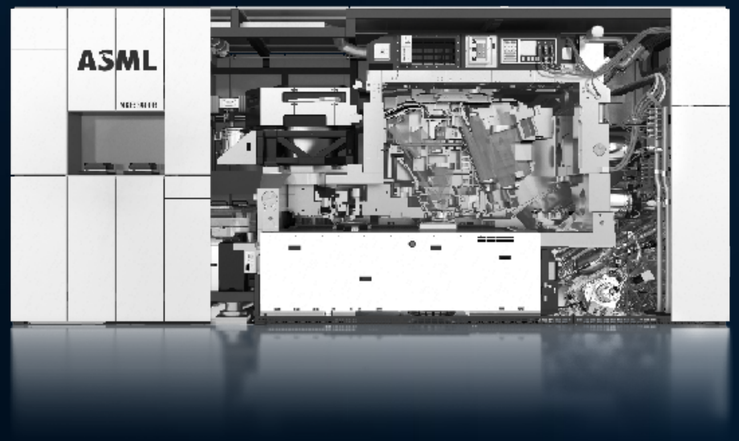
1



Shrink the switch

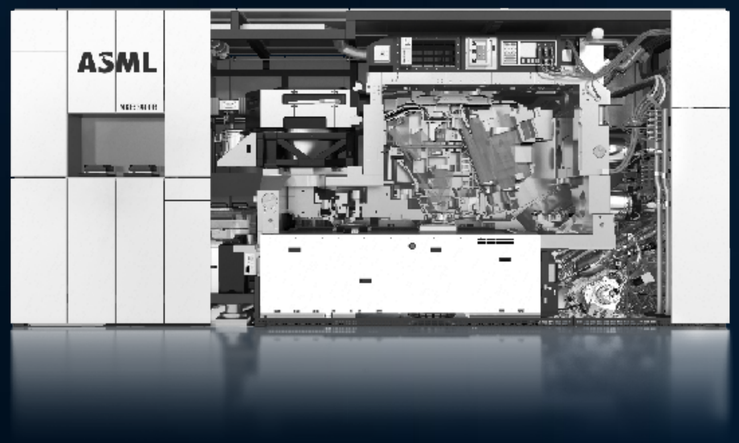
Scaling the switch enabled by the lithography roadmap

"5nm" → "3nm" → "2nm" → “1.4nm" → “1nm" → “sub-1nm”



Scaling the switch enabled by the lithography roadmap

"5nm" → "3nm" → "2nm" → “1.4nm" → “1nm" → “sub-1nm”



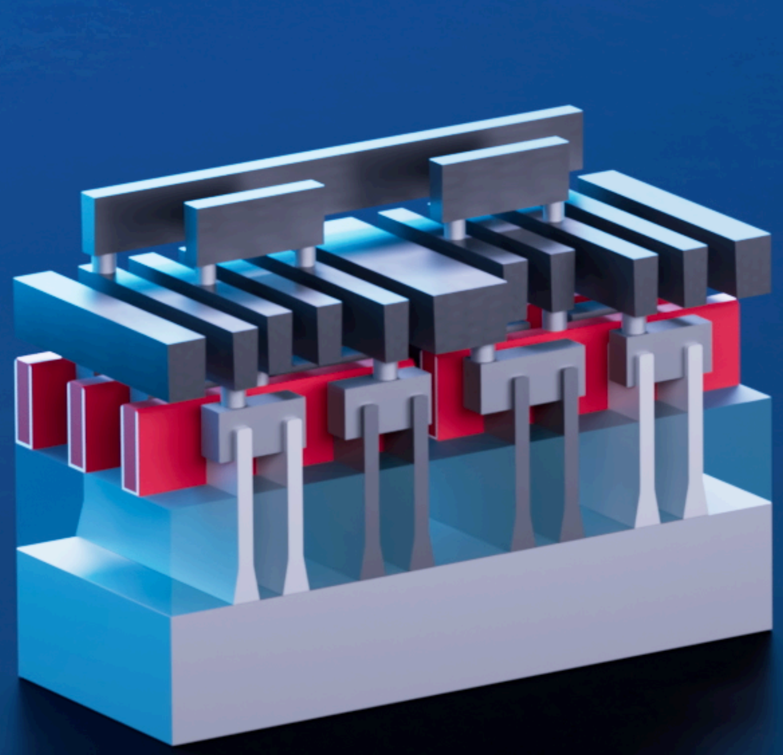


2

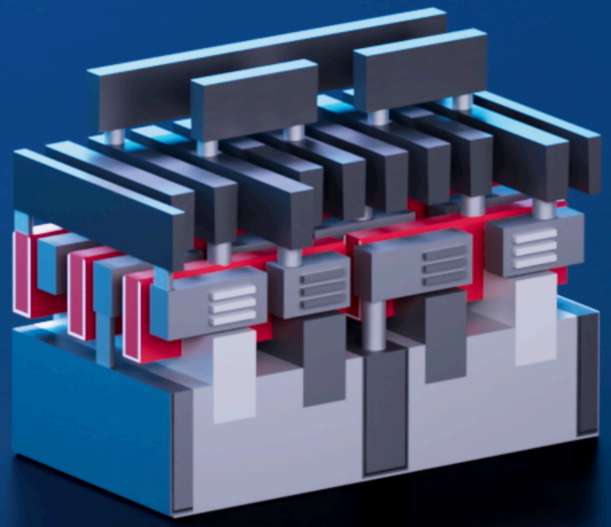


The next switch

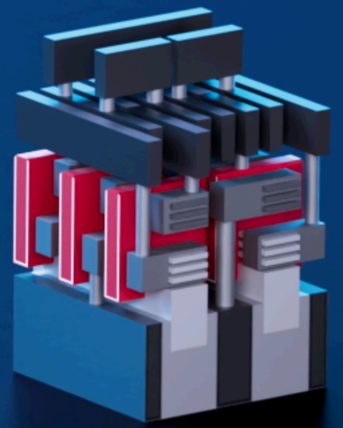
Disruptive Architectural Innovations



FinFET

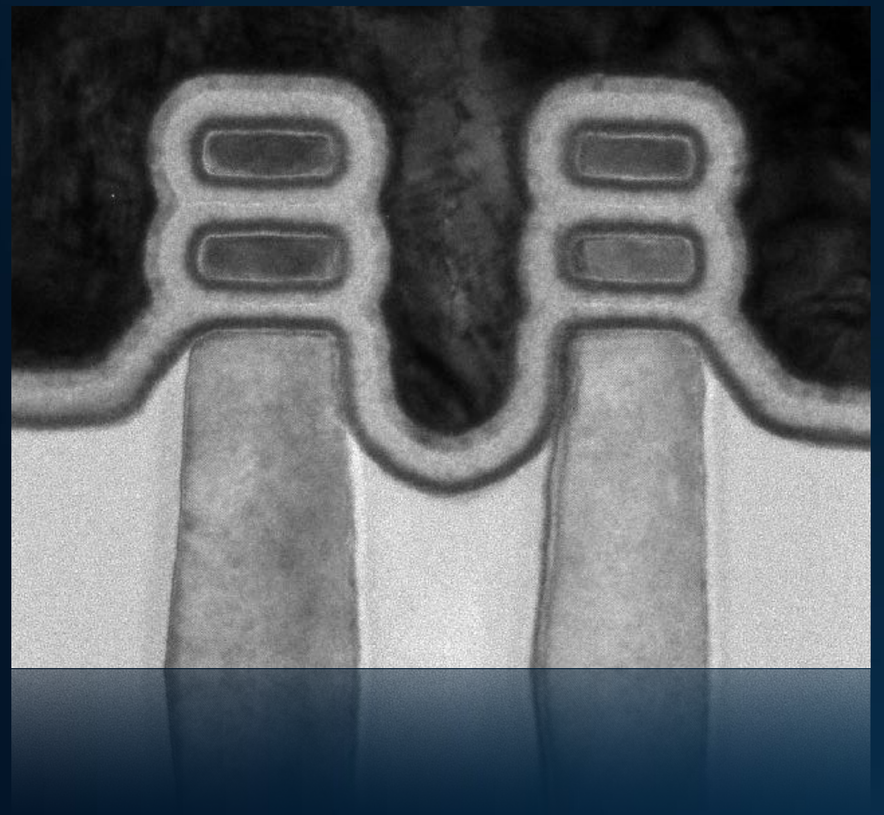


GAA Nanosheet

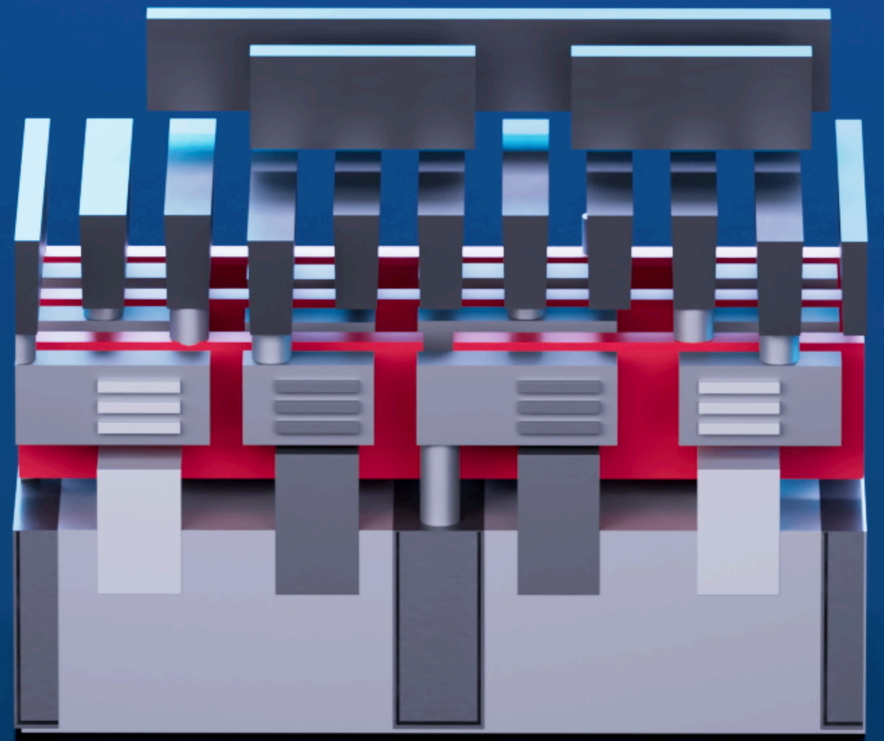


CFET

Gate-All-Around / Nanosheet transistor

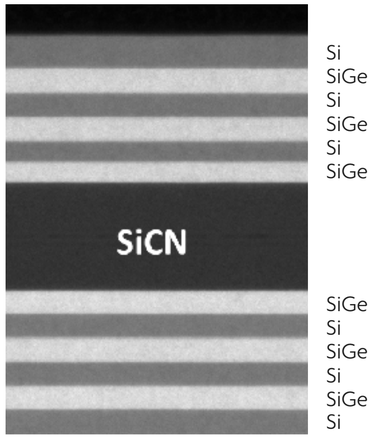


CFET



CFET

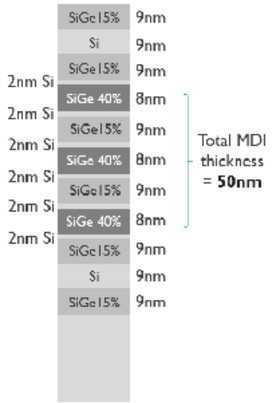
Controlled epi + embedded dielectric

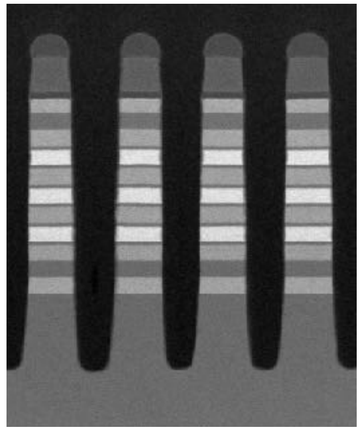


Si
SiGe
Si
SiGe
Si
SiGe

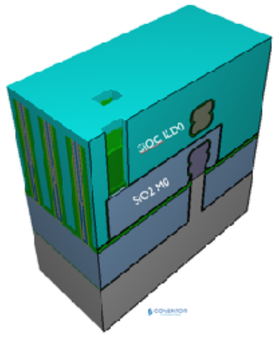
SiGe
Si
SiGe
Si
SiGe
Si

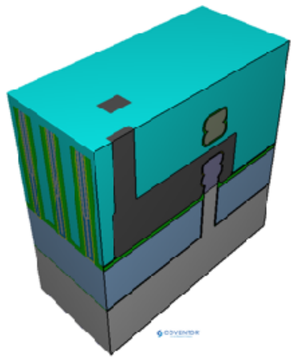
Patterning

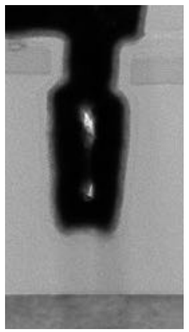


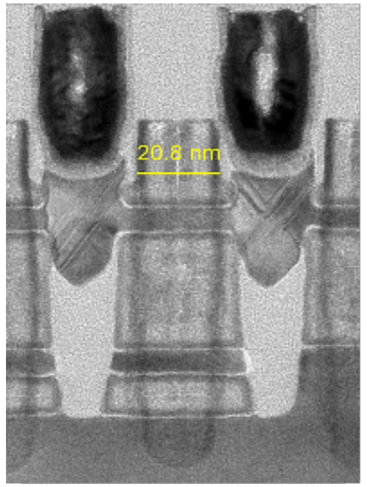


Replacement metal contacts

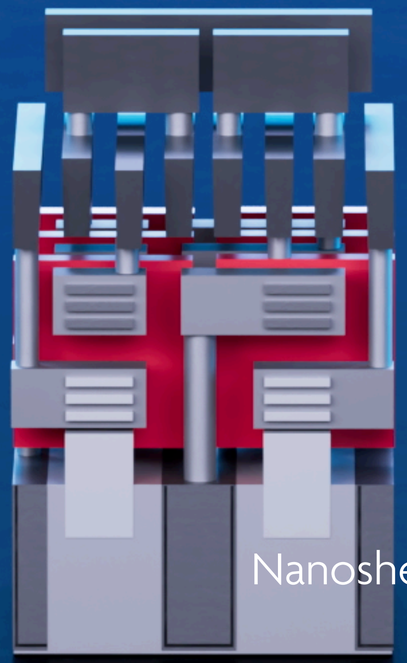








Towards sub-"1nm" nodes



FinFET

Nanosheet

CFET

Potential roadmap extension

Potential roadmap extension

2018	2020	2022	2024	2026	2028	2030	2032	2034	2036
N7	**N5**	**N3**	**N2**	**A14**	**A10**	**A7**	**A5**	**A3**	**A2**

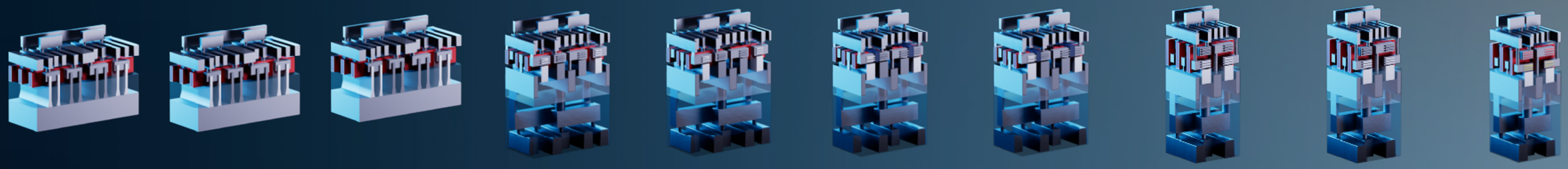
Continued dimensional scaling

Metal Pitch [nm]	40	28	23	23	21-18	21-18	18-16	18-16	16-12	16-12

Device and material innovations

Metal Tracks	7	6	6	6	5	5	5	4	<4	<4
	FinFET	**FinFET**	**FinFET**	**GAA** Nanosheet	**GAA** Nanosheet	**GAA** Forksheet	**GAA** Forksheet	**CFET**	**CFET**	**CFET** Atomic

Context-aware interconnect



3



The third dimension

Logic



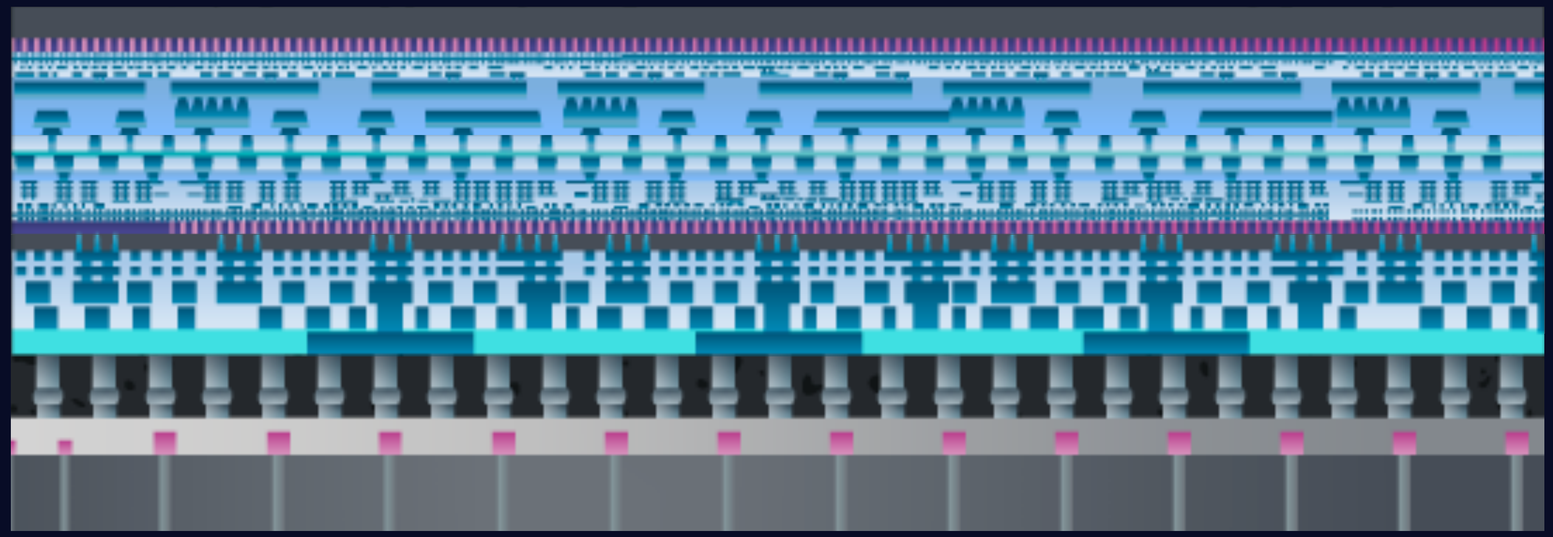
3D stacked core processor SOC

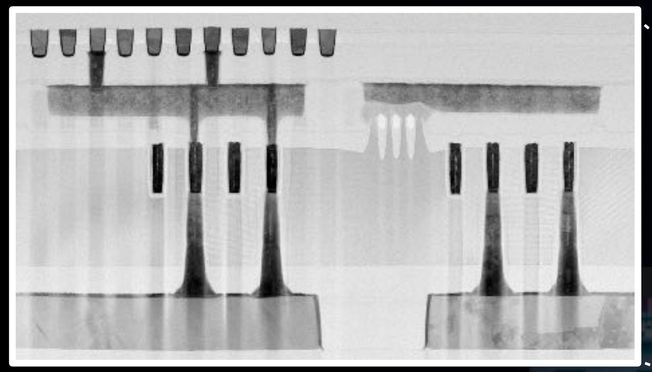
SRAM

Logic

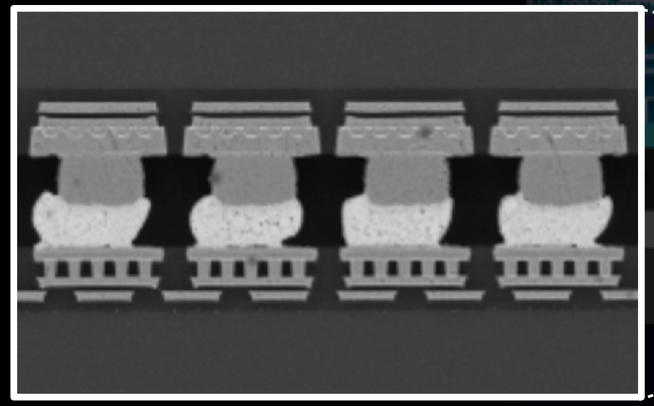
BS-PDN

I/O





Back-side Power Distribution

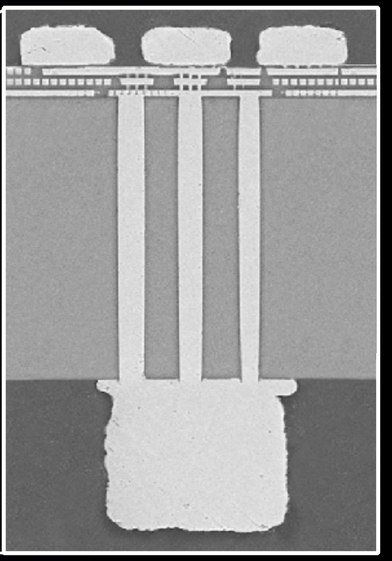


D2W using micro-bump

3D stacked core processor SOC



Cu-Cu Hybrid Bonding



Through-Si Via

Si photonics | Advanced CMOS | Memory | Mature technologies | FDSOI | GaN RF/Power

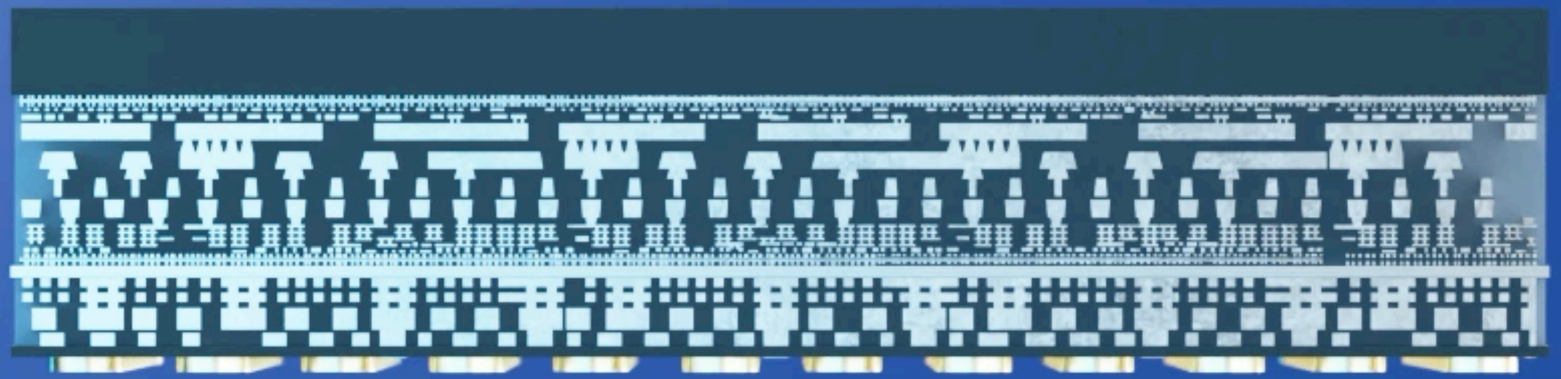
3D stacked core processor SOC

SRAM

Logic

BS-PDN

I/O



© imec 2022

Si photonics

Advanced CMOS

Memory

Mature technologies

FDSOI

GaN RF/Power

"scaled" technologies

Computation in most advanced technology nodes

+

“non-scaled" technologies

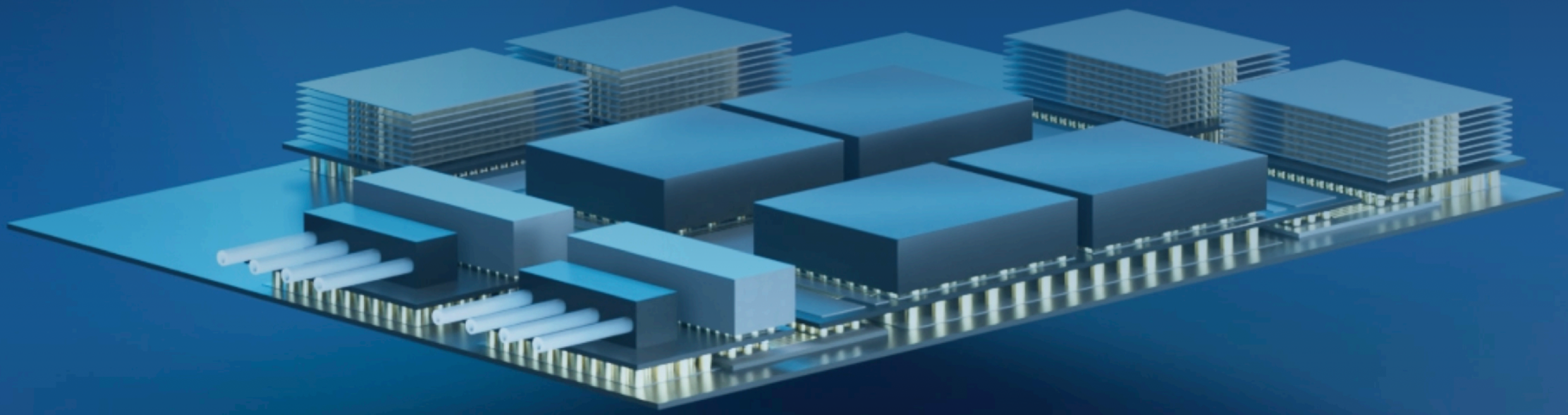
Sensors. RF, Power, Photonics...

4



Paradigm change

The future of scaling needs **system-level thinking**



SYSTEM OPTIMIZATION BASED ON OFF-THE-SHELVE TECHNOLOGY

SYSTEM OPTIMIZATION

application driven platforms / software

system modelling

architecture

component



DESIGN-TECHNOLOGY CO-OPTIMIZATION

design

device

technology

process



TECHNOLOGY OPTIMIZATION FOR GENERIC APPLICATIONS

SYSTEM-TECHNOLOGY CO-OPTIMIZATION

application driven platforms / software

system modelling

architecture

component

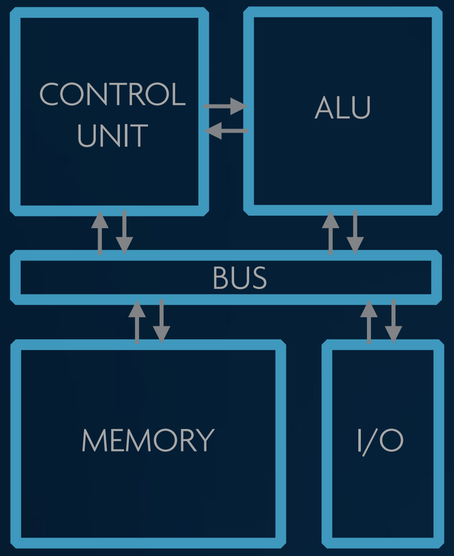
design

device

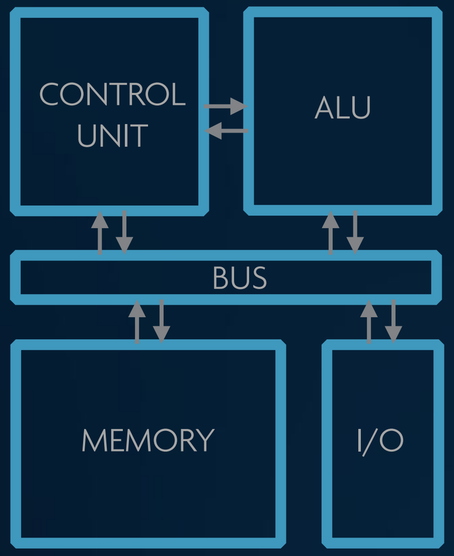
technology

process

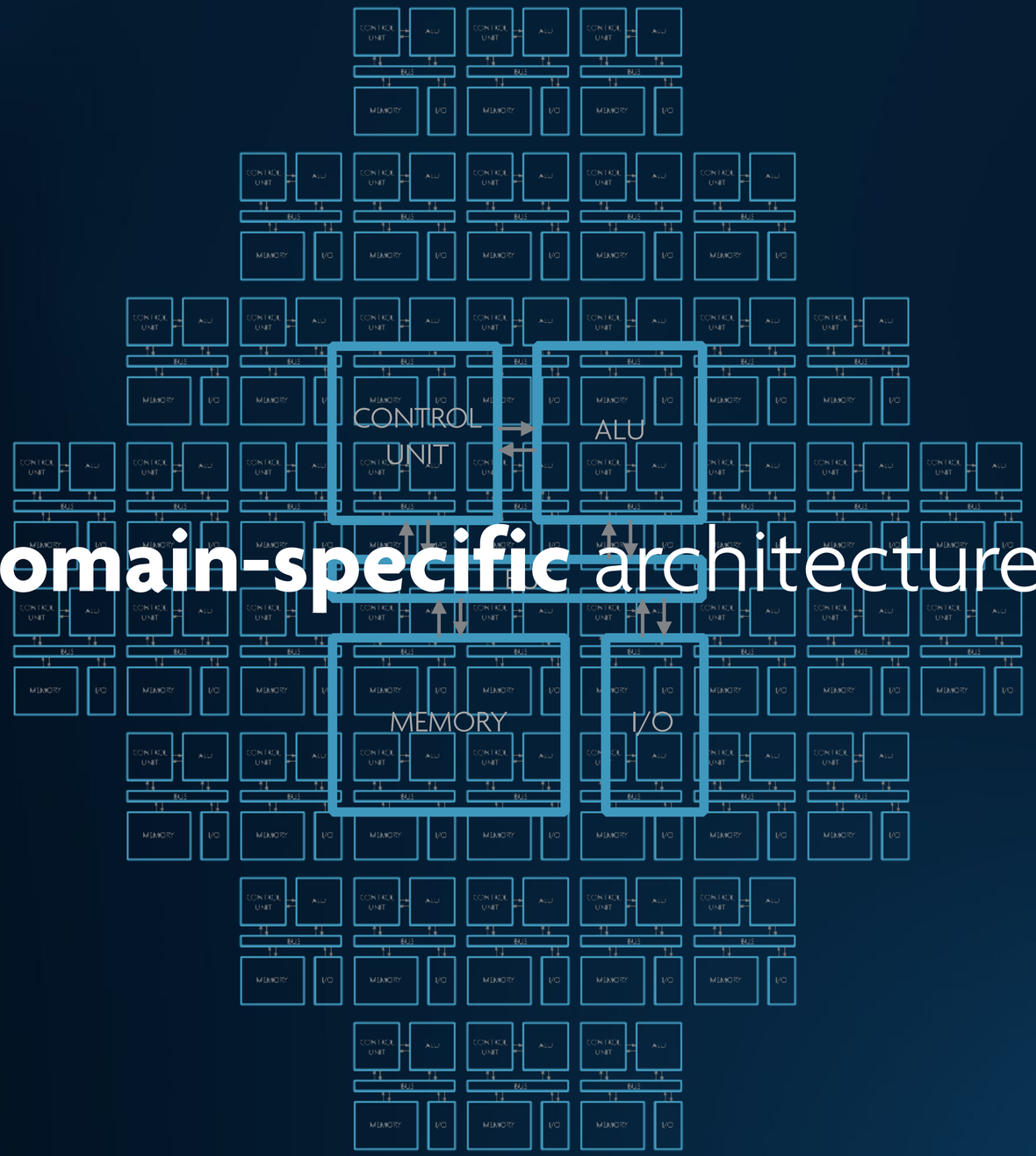




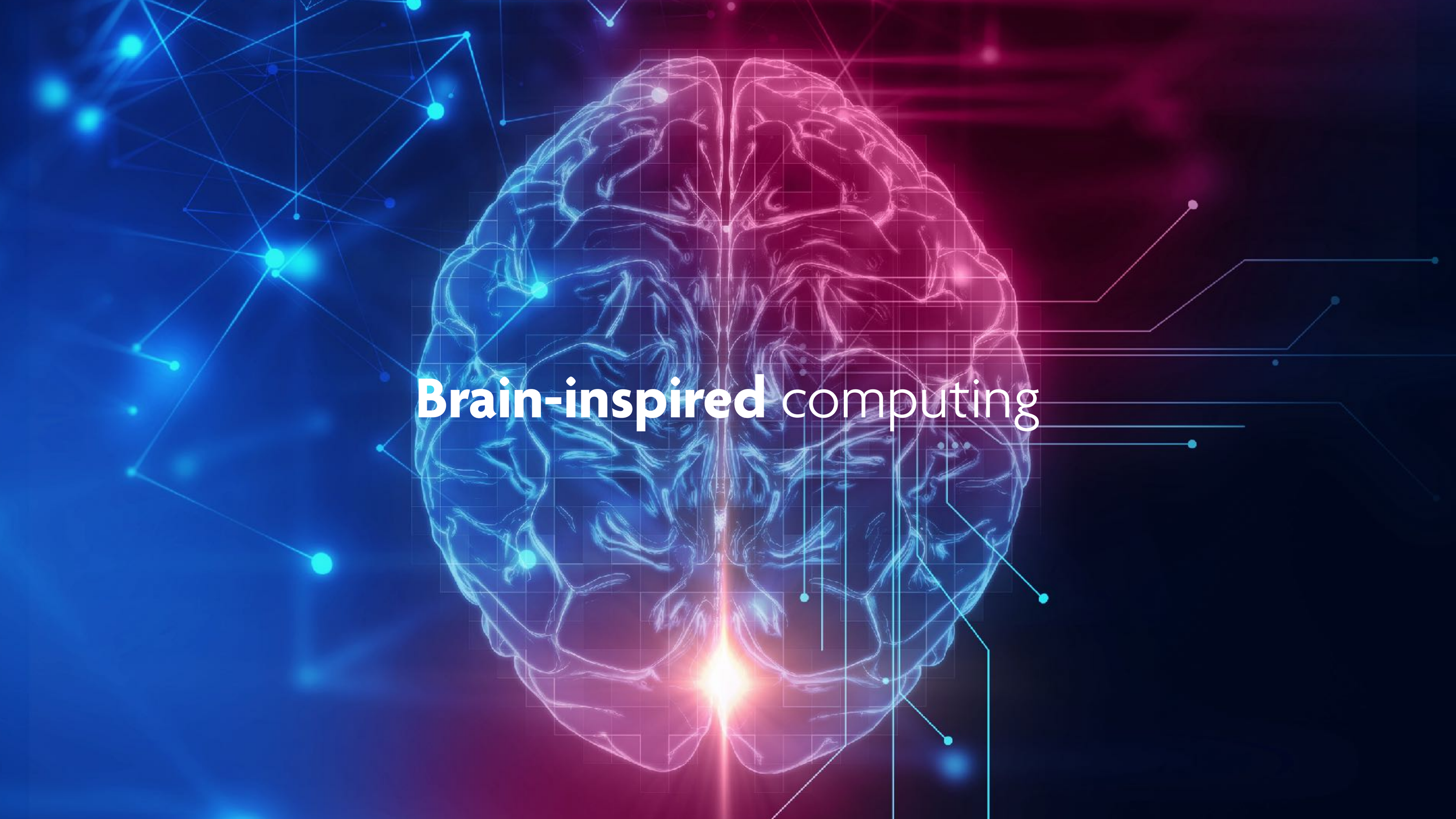
von Neumann architectures



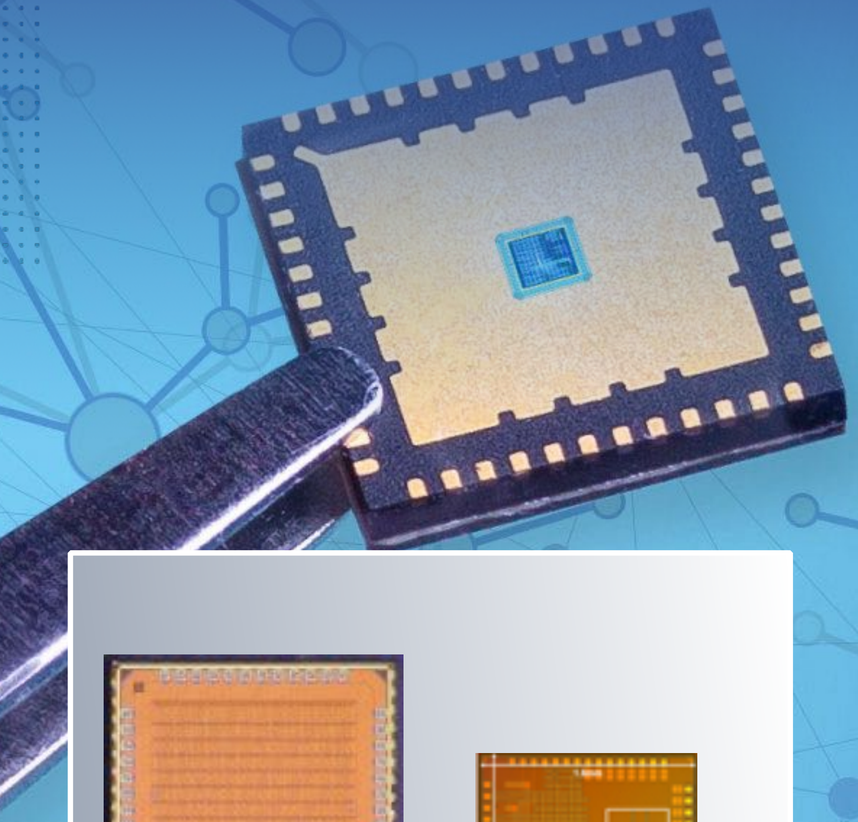
Domain-specific architectures

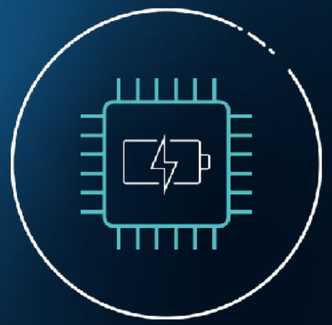


Domain-specific architectures


Brain-inspired computing

Neuromorphic computing for sensor fusion





power wall



performance wall

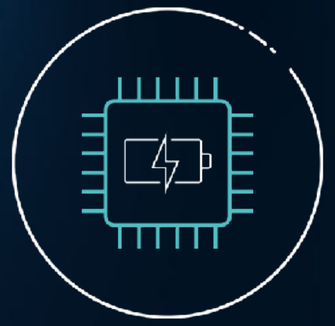


scaling wall

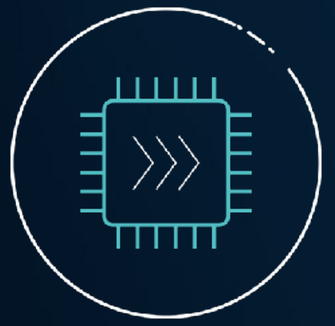


cost wall

Breaking down **‘the Walls’**



power wall



performance wall



scaling wall



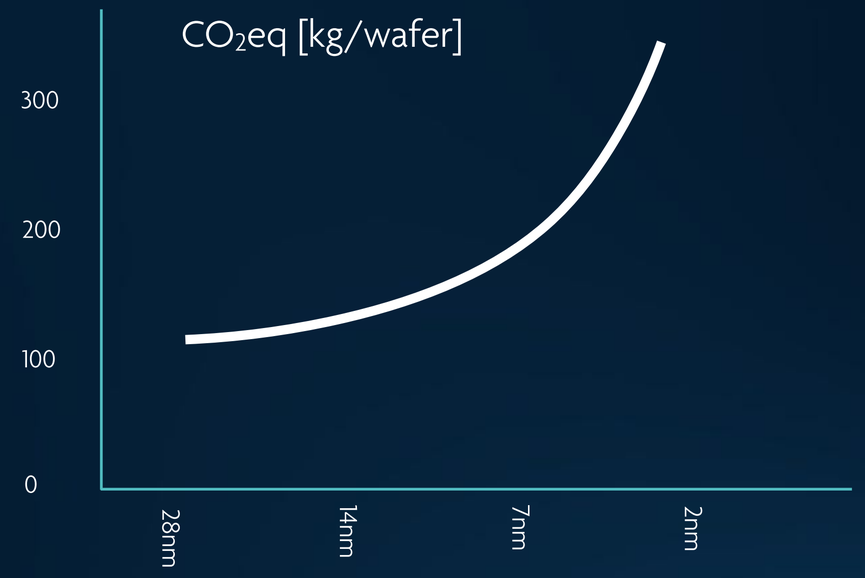
cost wall



sustainability wall

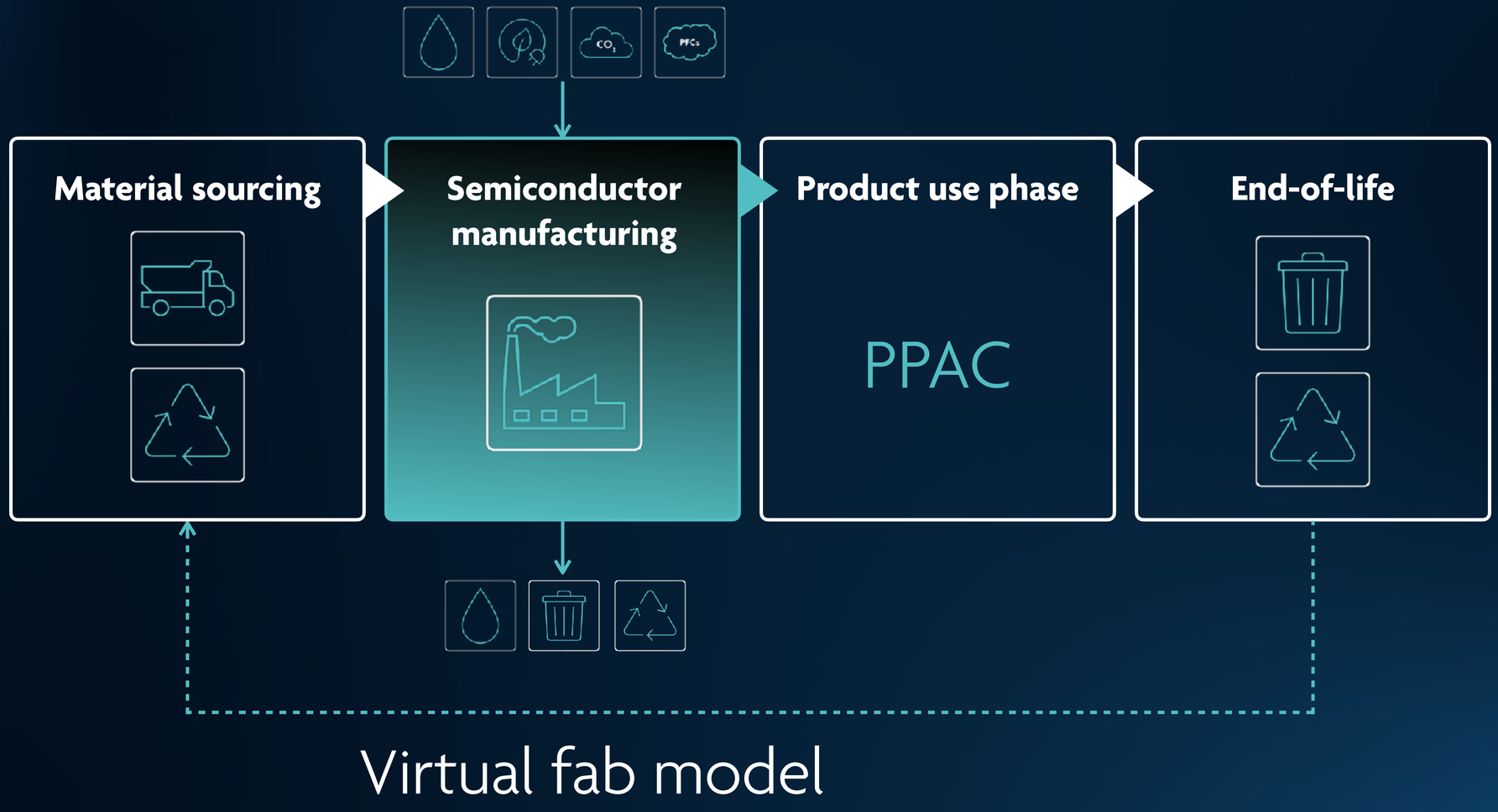
Sustainability wall

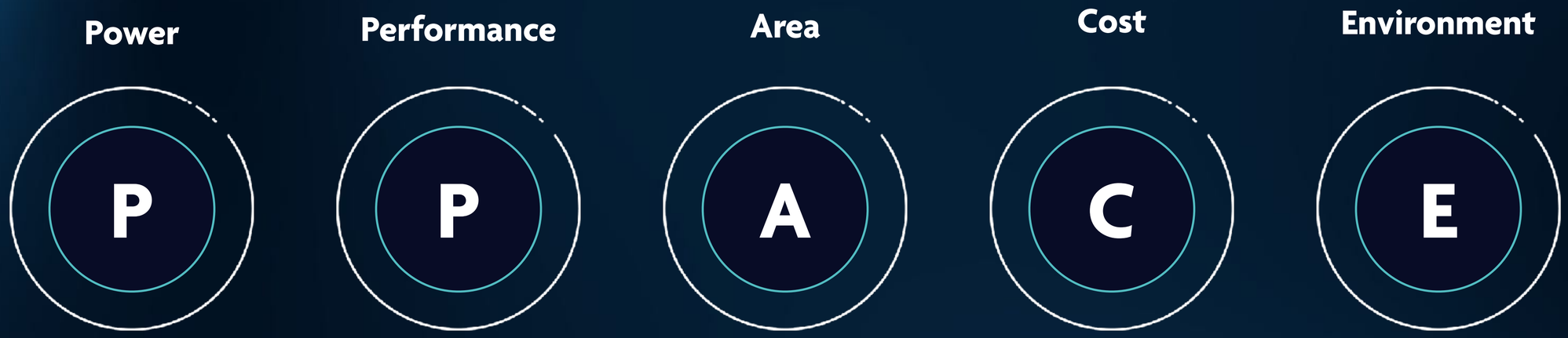
sustainability wall



CO_2 footprint of semi manufacturing is rapidly rising

Sustainable Semiconductor Technologies & Systems

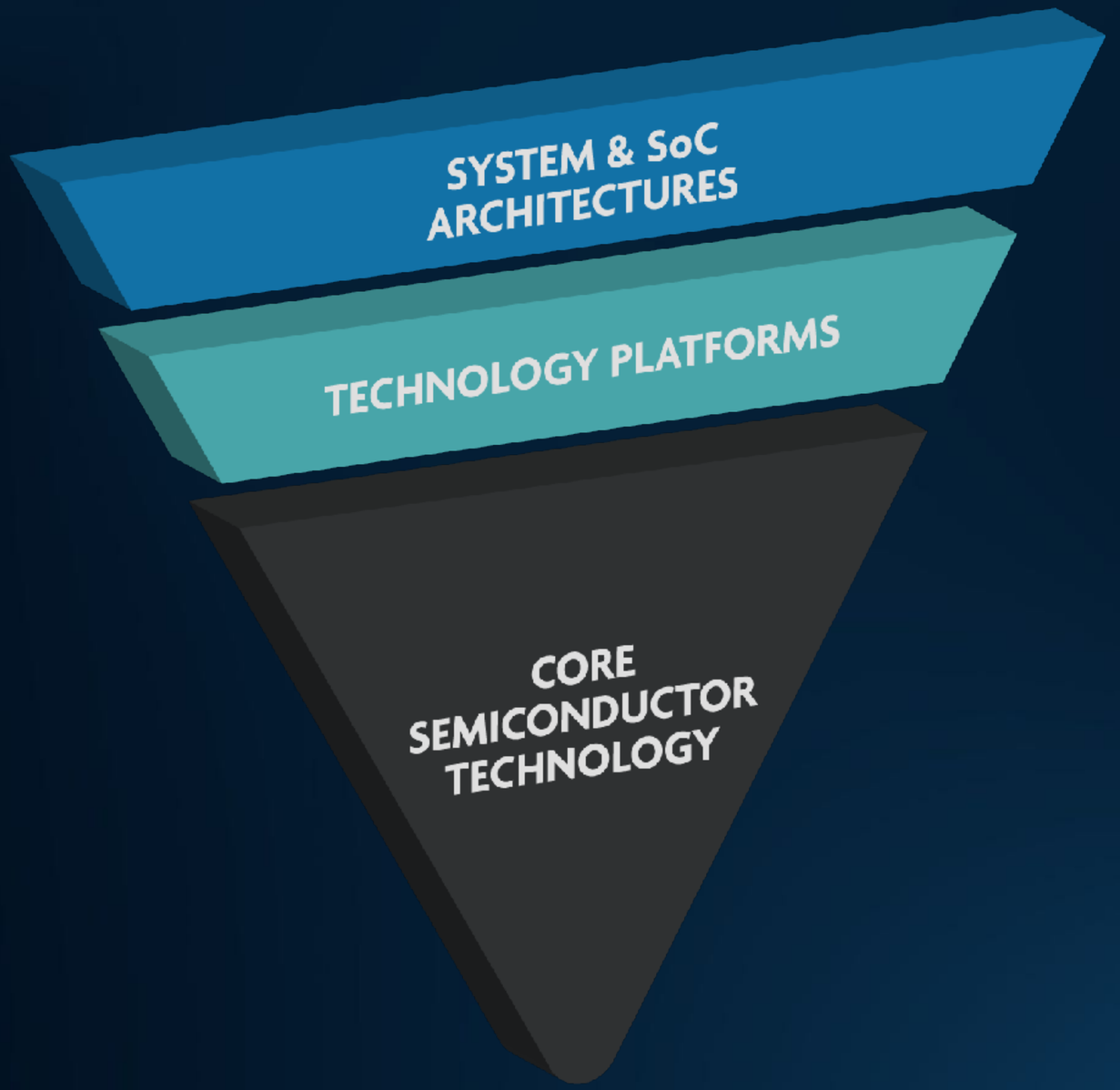



Power
Performance
Area
Cost
Environment
P
P
A
C
E
power wall
performance wall
scaling wall
cost wall
sustainability wall

Fast growth of program members






SYSTEM & SoC ARCHITECTURES
TECHNOLOGY PLATFORMS
CORE SEMICONDUCTOR TECHNOLOGY


Climate change


Sustainable Mobility

Air pollution

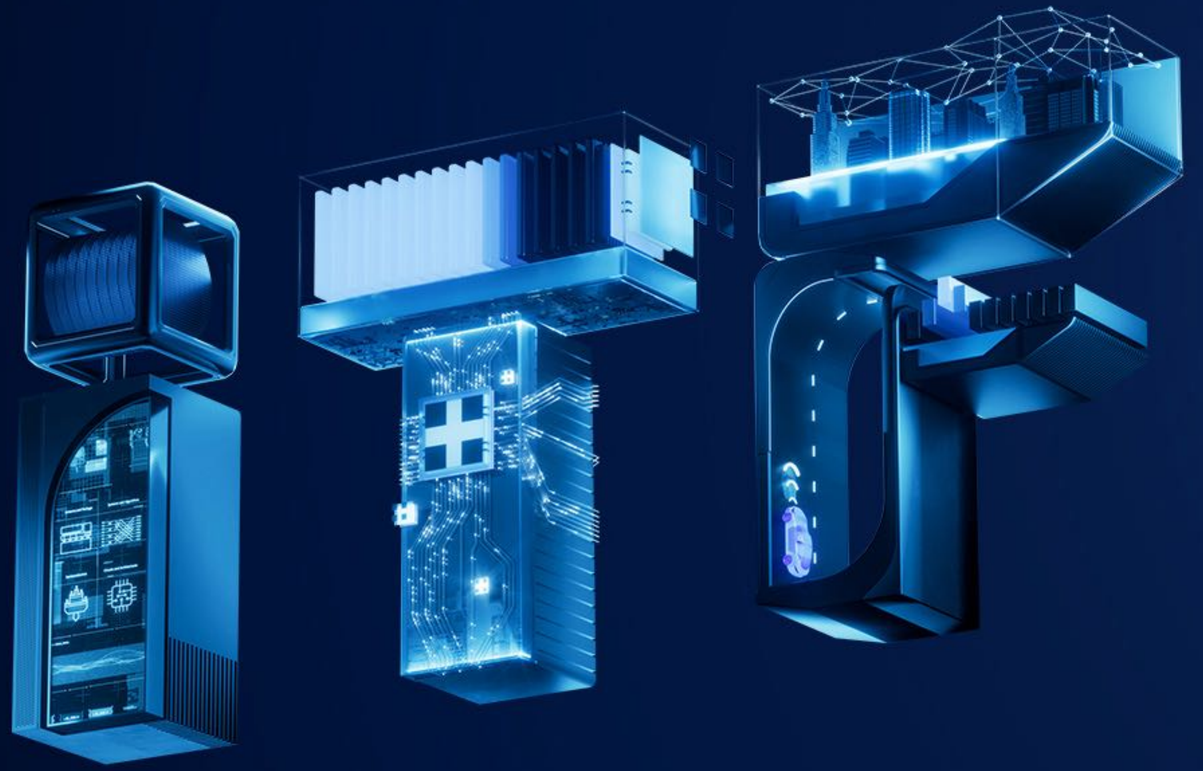



817 .92
Food shortage

We need **disruptive deep tech innovations**
We need **massive data handling**
We need **more performant technologies**

Building deep tech ecosystems is the **lodestar** to meet **the challenges** of the **21st century**

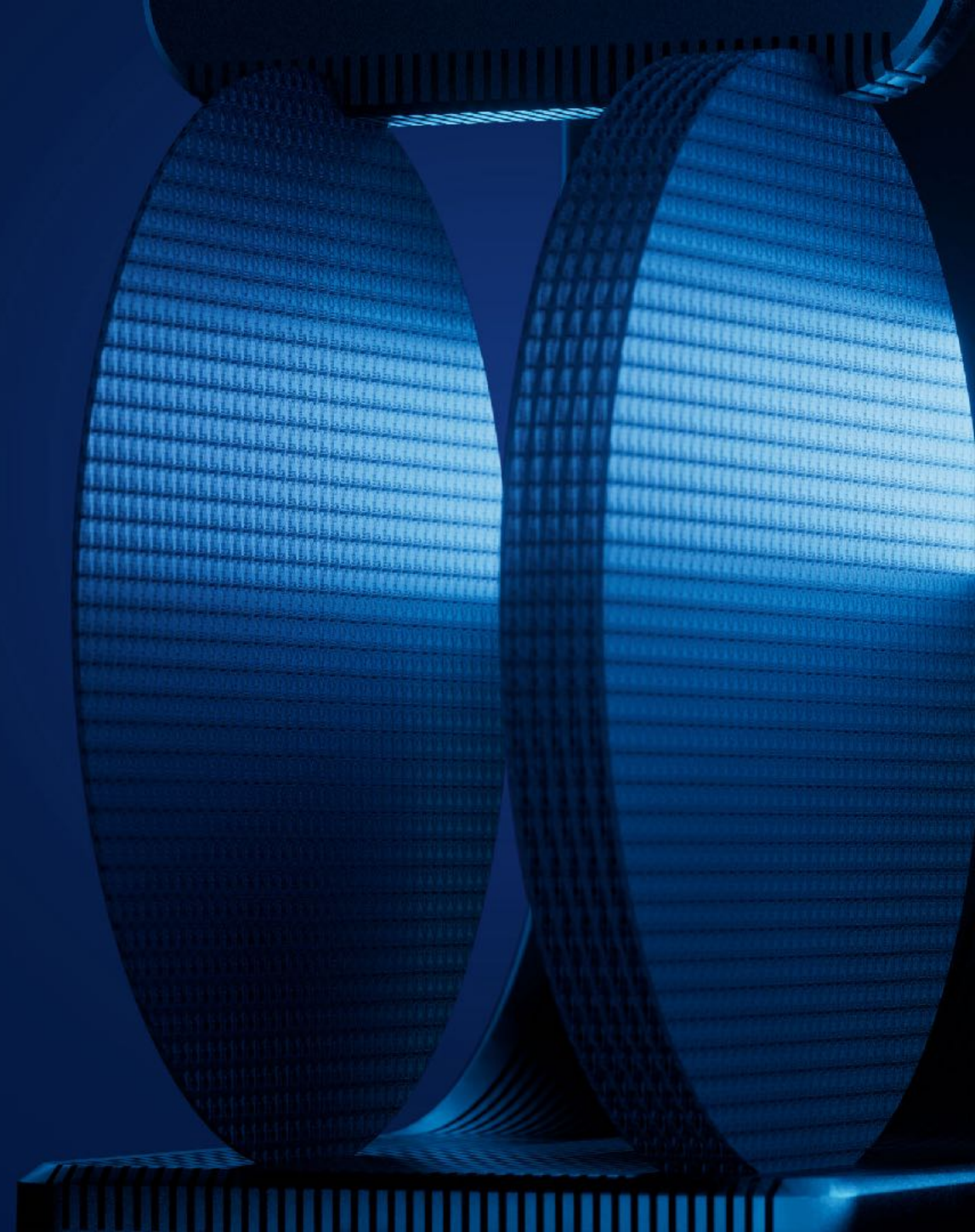
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Explore **next-gen** mobile **connectivity**

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Thank you for your attention



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embracing a better life