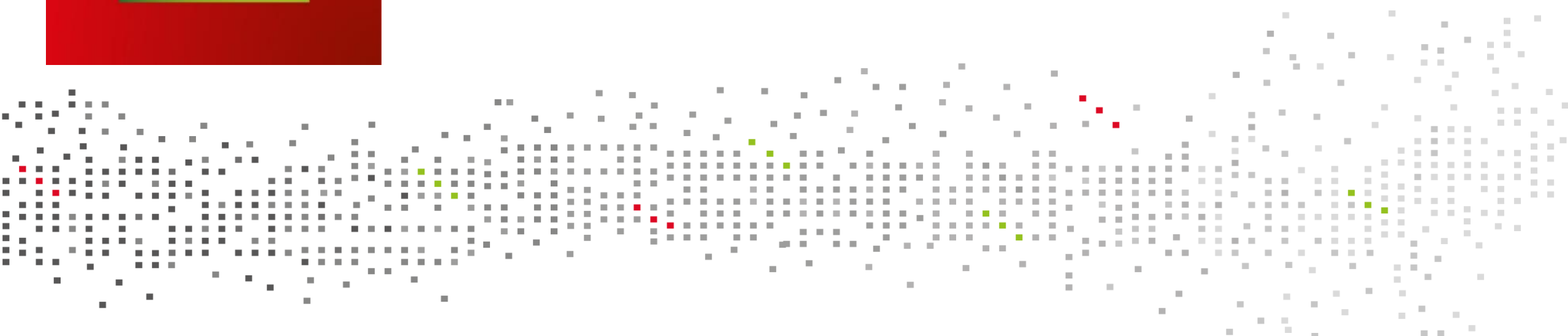




SEMICON® EUROPA

Nov 15-18, 2022 | MESSE
MÜNCHEN | Co-located with
electronica



EXOTIC APPLICATIONS OF NANOSECOND LASER ANNEALING

Sébastien KERDILES - Nov 2022

COLLABORATIONS & PARTNERS

- LETI : P. ACOSTA-ALBA, L. DAGAULT, M. OPPRECHT, C. FENOUILLET-BERANGER, L. BRUNET, L. GRENOUILLET, F. LEFLOCH

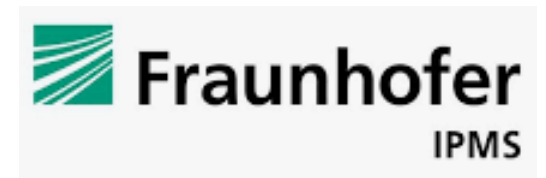
- SCREEN / LASSE : T. TABATA, F. ROZE, K. HUET, F. MAZZAMUTO



- CNRS (LAAS) : F. CRISTIANO, R. DAUBRIAC



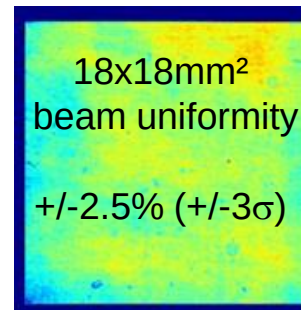
- FRAUNHOFER (IPMS) : T. ALI, T. KAMPFE, K. SEIDEL



INTRODUCTION : EQUIPMENT

At LETI, Nanosecond laser annealing (NLA) is performed using SCREEN LT-3100 platform

- ❖ XeCl excimer laser :
 - ❖ **UV laser : 308 nm wavelength**
 - ❖ **160 ns pulse duration (FWHM)**
- ❖ Fully automated system for 200 & 300 mm wafers
- ❖ Scan & repeat mode with masks : beam = 15x15, 26x33 mm², ...
- ❖ In-situ metrology : Time Resolved Reflectometry (melt detection)
- ❖ Heating chuck : 20-400°C
- ❖ Ambient : N₂, Ar, O₂



ULTRA-SHORT & SELECTIVE ANNEAL

NLA : Surface exposed to a pulsed laser beam

➤ High T° anneal with extremely fast heating & cooling

→ Enables high active dopant concentrations

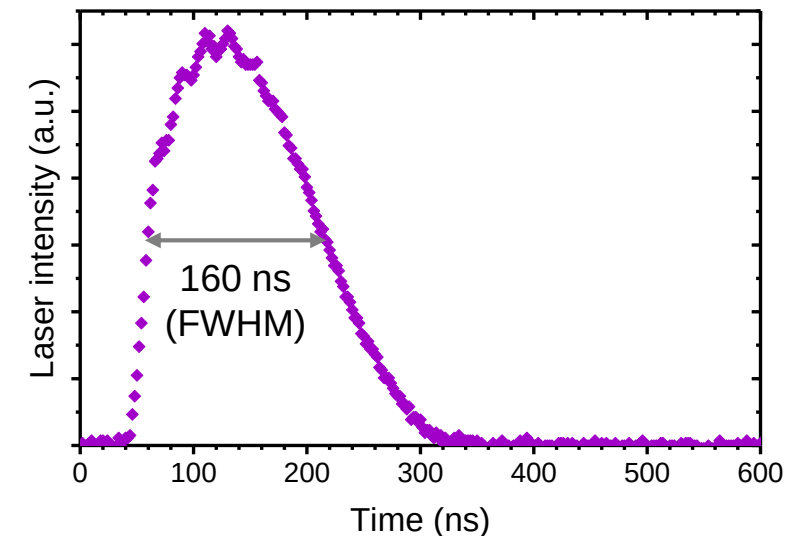
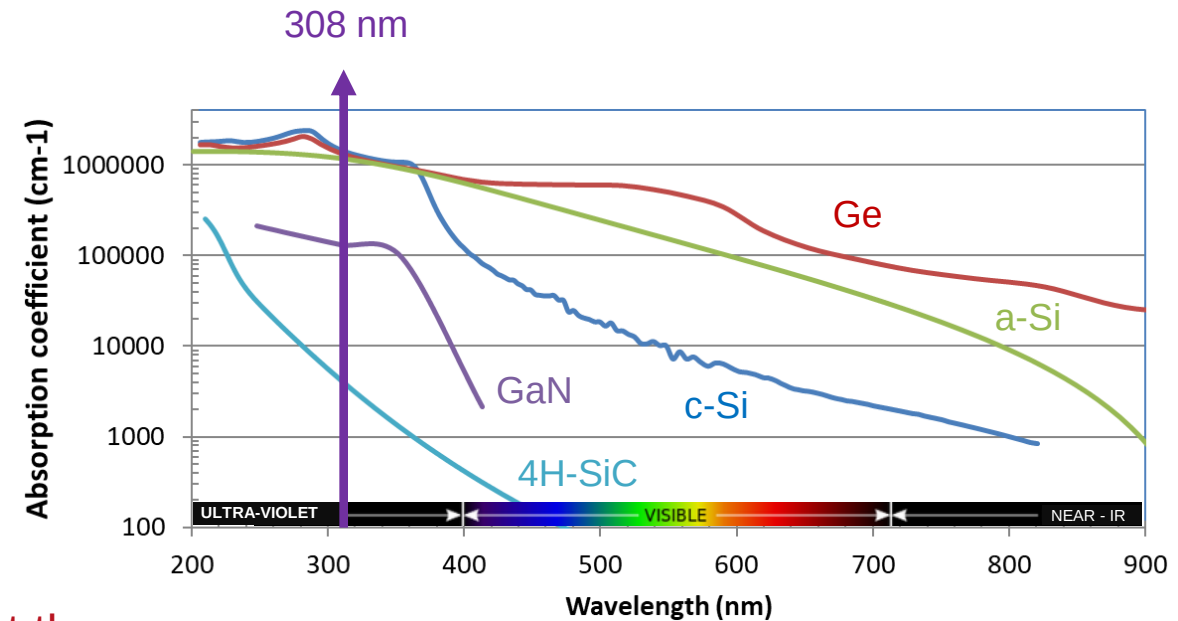
➤ Selective anneal : only the extreme surface is heated, not the volume

❖ Short wavelength : absorption limited to the surface

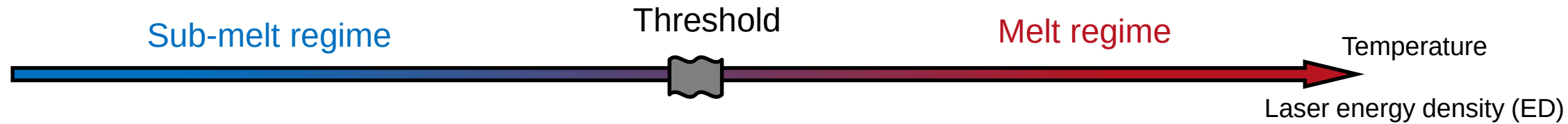
Penetration depth : ~ 7 nm in Si or Ge,
~ 100 nm in GaN, ~ 2 μm in 4H-SiC

❖ Short pulse : very limited heat diffusion

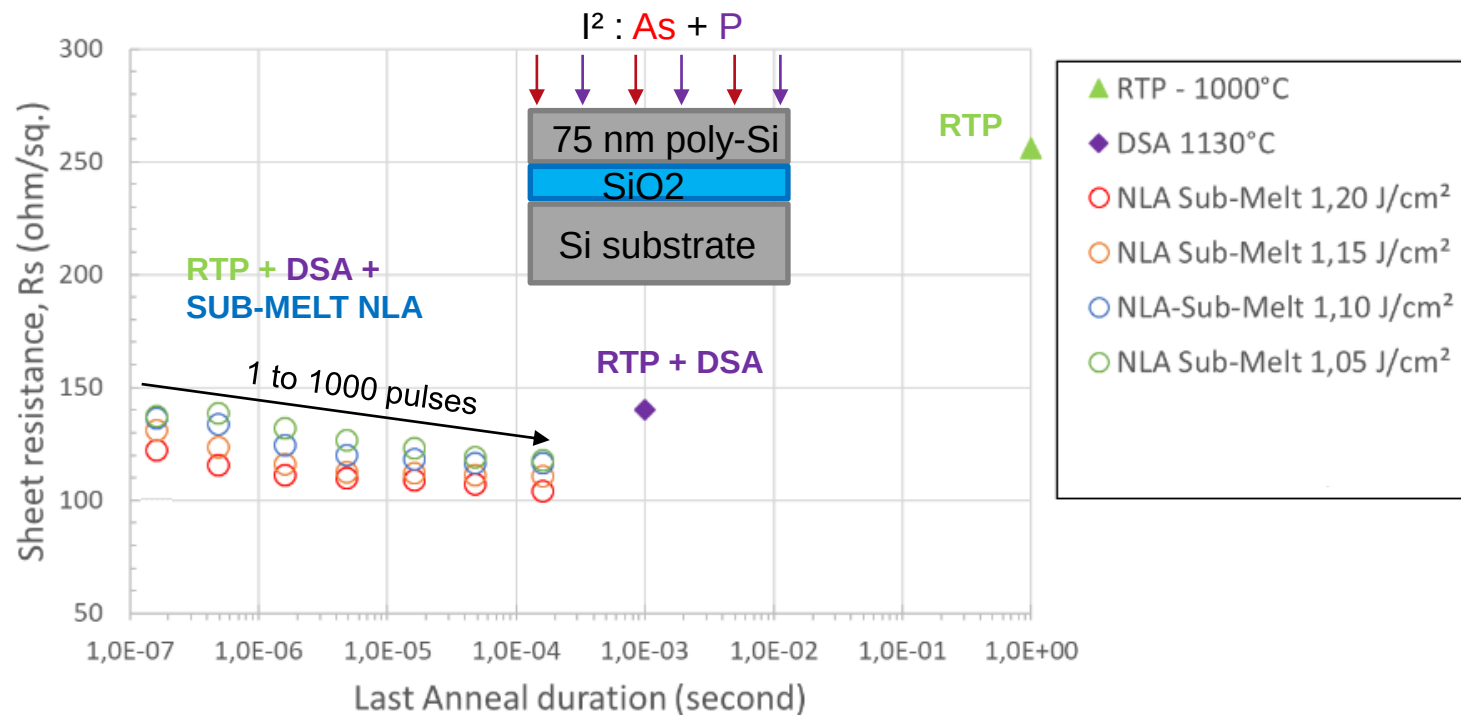
→ Enables anneals of the top layers with moderate temperatures in the underlying structures. Perfect for 3D integration !



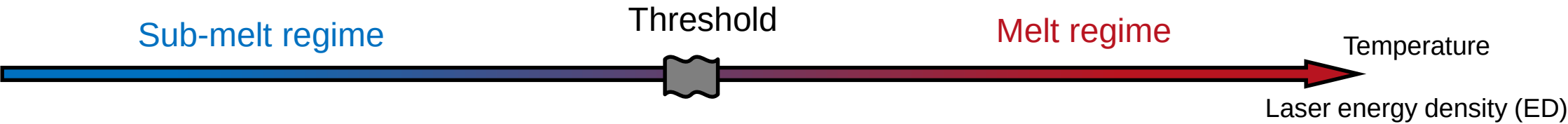
INTRODUCTION : 3 INTERESTING REGIMES



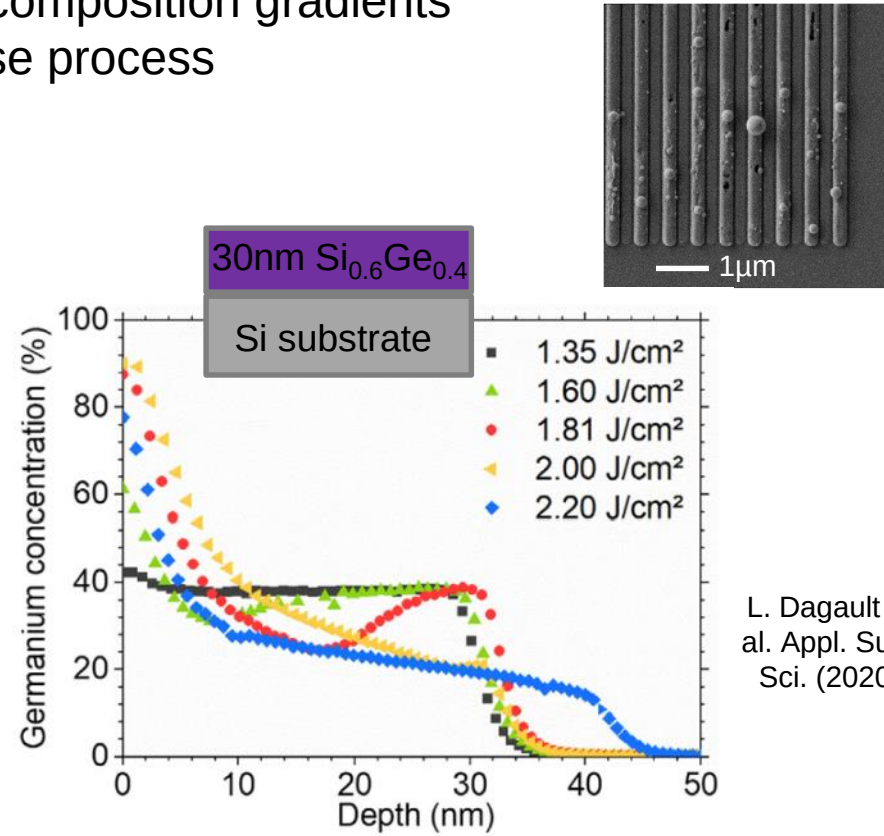
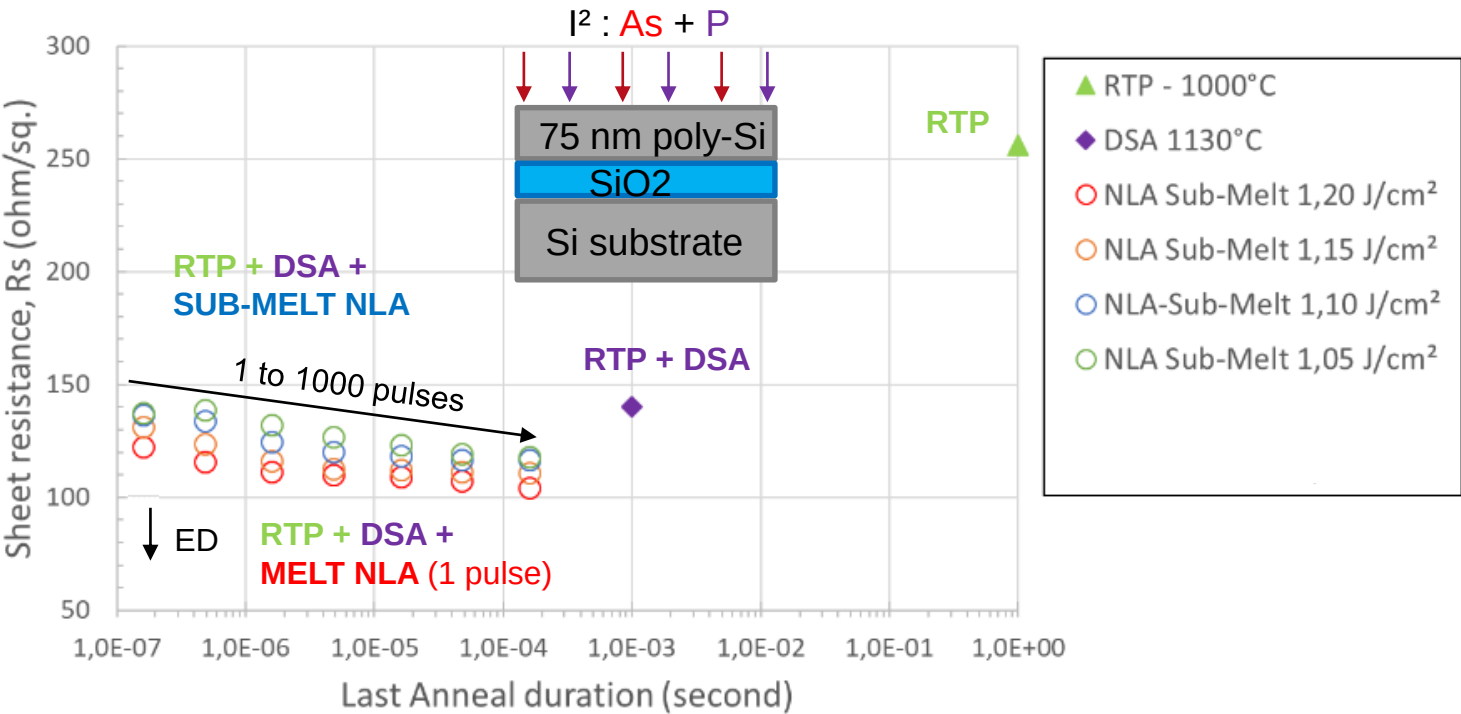
- ❖ Solid-phase : no morphology change / roughening
- ❖ Almost no diffusion
- Often multi-pulse process (cumulative effects)



INTRODUCTION : 3 INTERESTING REGIMES

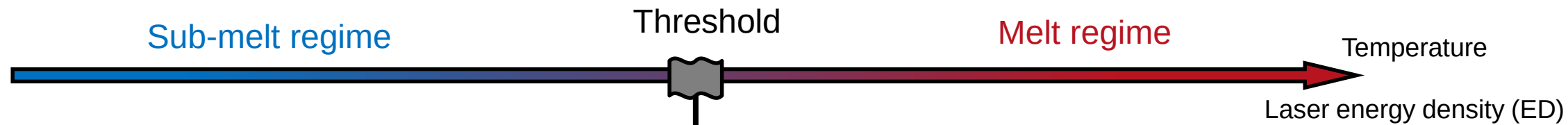


- ❖ Solid-phase : no morphology change / roughening
- ❖ Almost no diffusion
- Often multi-pulse process (cumulative effects)
- ❖ Liquid-phase : morphology & roughness changes
- ❖ Diffusion, composition gradients
- Single pulse process



L. Dagault et al. Appl. Surf. Sci. (2020)

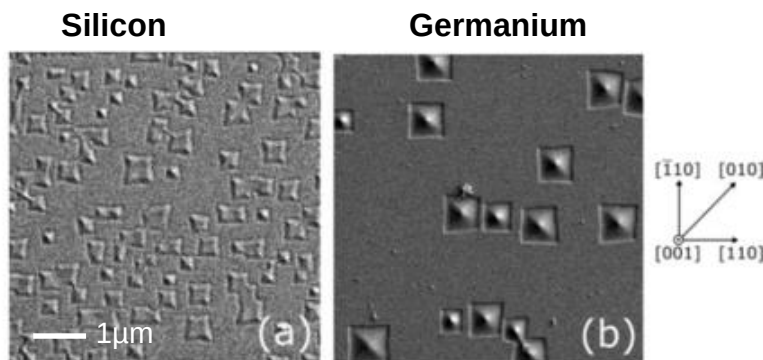
INTRODUCTION : 3 INTERESTING REGIMES



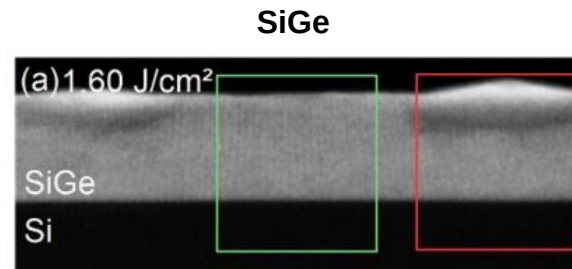
- ❖ Solid-phase : no morphology change / roughening
- ❖ Almost no diffusion
- Often multi-pulse process (cumulative effects)

- ❖ Liquid-phase : morphology & roughness changes
- ❖ Diffusion, composition gradients
- Single pulse process

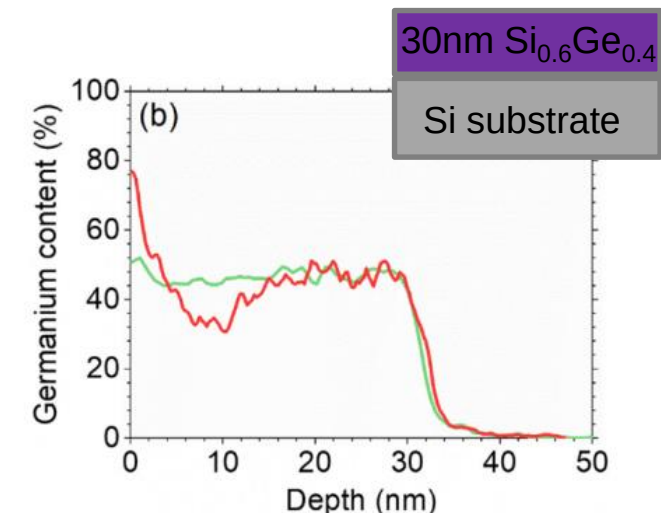
❖ At the melt onset : isolated molten islands appear



SEM top view of Si & Ge epilayer after UV-NLA close to the melt threshold



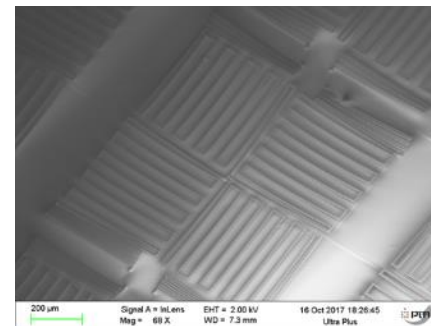
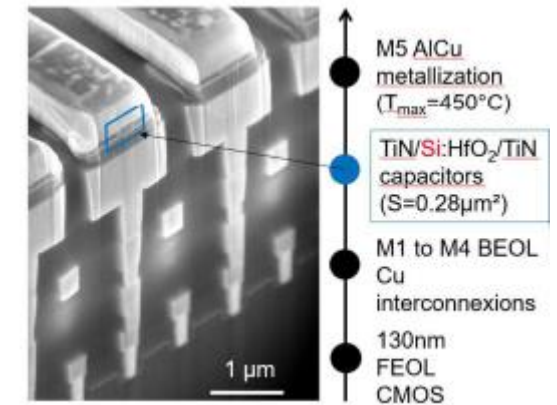
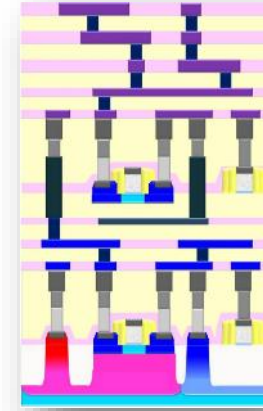
STEM HAADF & corresponding EDX Ge depth profiles after UV-NLA @ 1.6 J/cm²



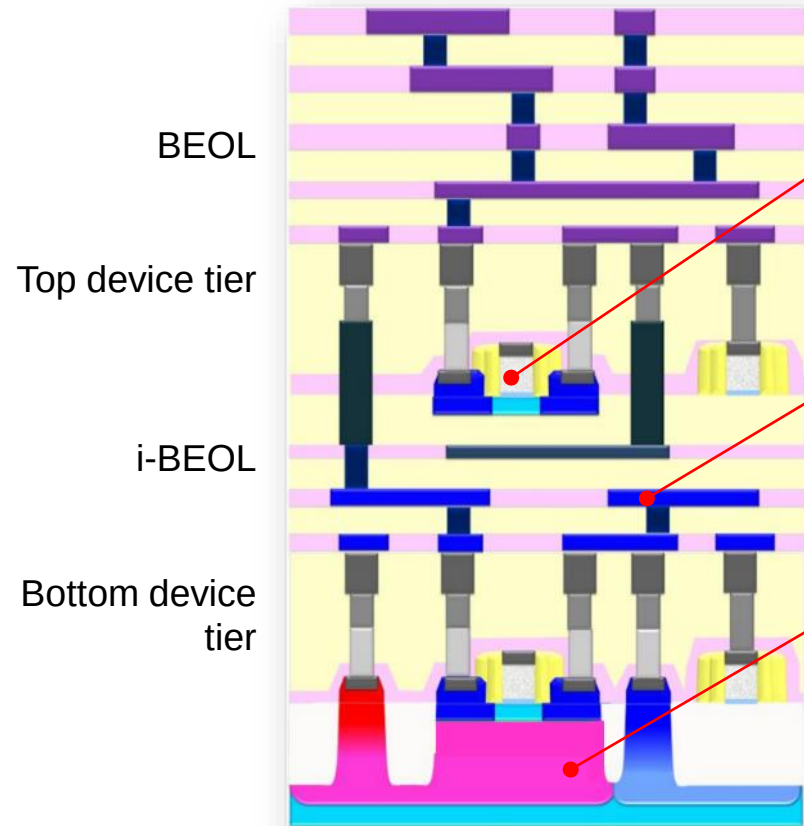
L. Dagault et al. Appl. Surf. Sci. (2020)

OUTLINE

- ❖ Introduction
- ❖ 3 More than Moore applications :
 - 3D sequential integration, CoolCube™
 - Ferroelectric memories
 - Highly doped Si:B for bolometers & quantum applications
- ❖ Conclusion



3D SEQUENTIAL INTEGRATION : THERMAL LIMITATIONS



'Cold' processing for the top level

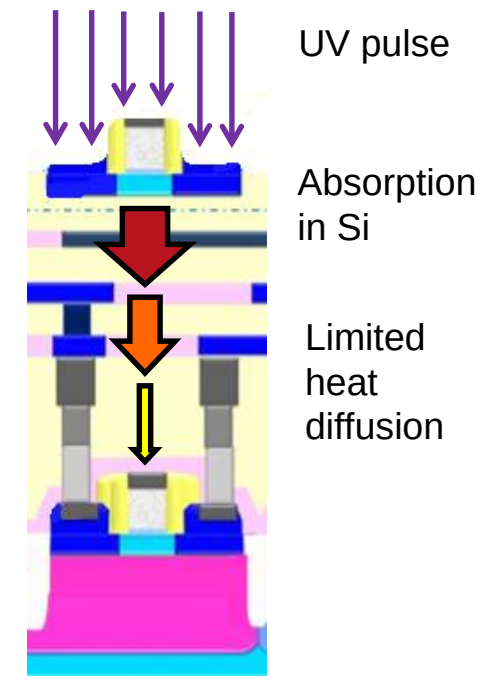
Local interconnect level thermal stability and low resistivity

Bottom MOSFET thermal stability

Thermal budget limitations

→ How to realize a high performance transistor at the upper level without impacting the bottom one ?

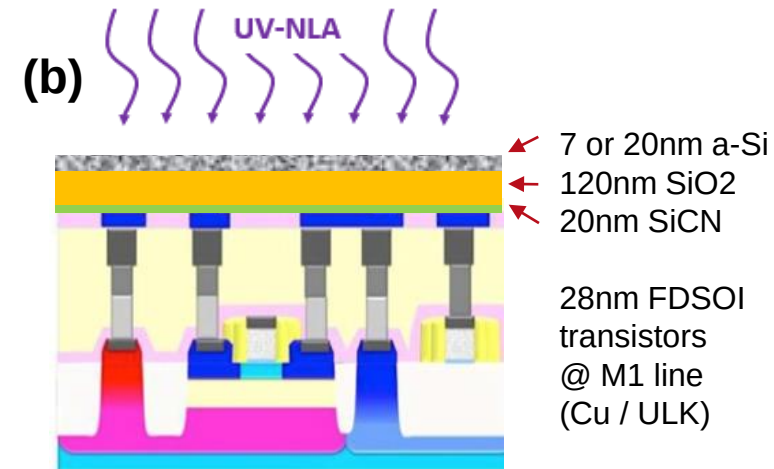
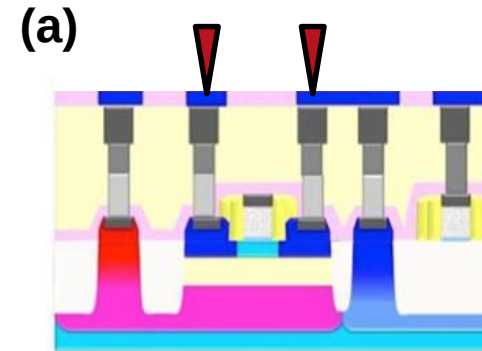
- ❖ Classical annealing techniques heating the whole wafer $> 500^{\circ}\text{C}$ not compatible
- Alternative = selective nanosecond laser annealing, heating only the top transistor



3D SEQUENTIAL INTEGRATION : TRANSISTOR & CU LOW-K STABILITY (1)

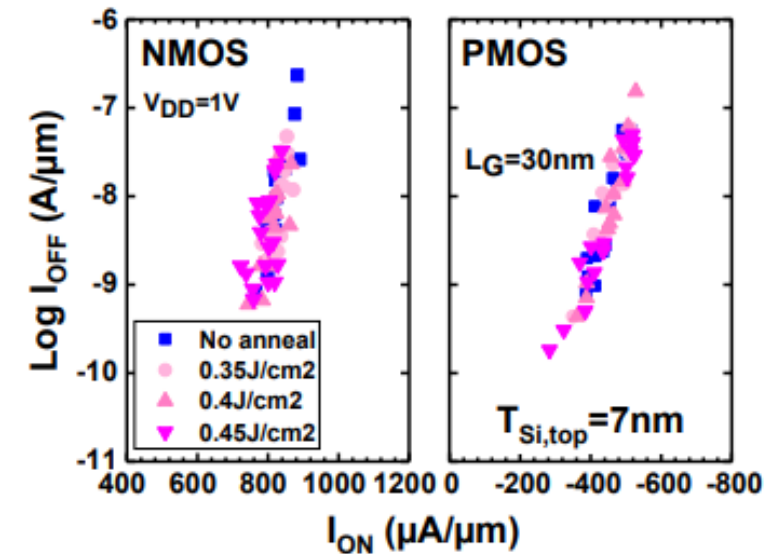
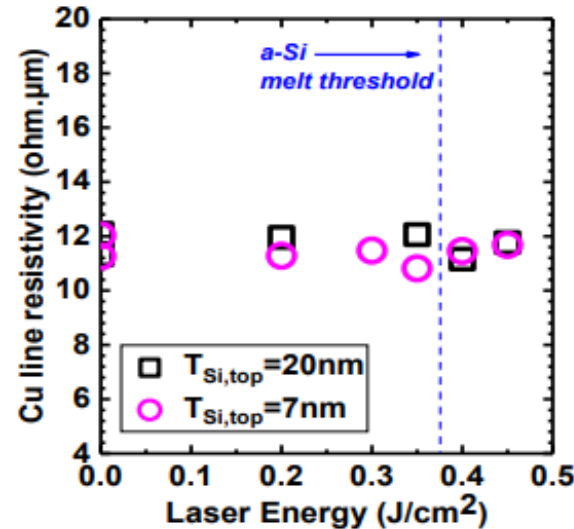
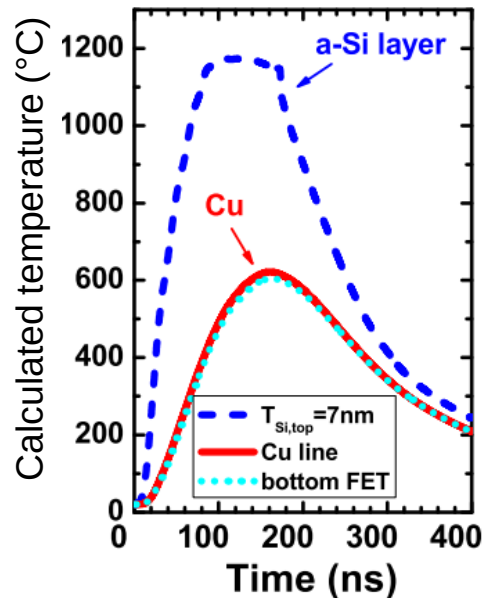
- ❖ Bottom device thermal stability upon UV-NLA evaluated on 28 nm FD-SOI technology with Cu/ULK @ M1 level.
- UV-NLA on a-Si layer simulating top device

- 28nm FD-SOI transistors @ M1 level (TaN/Ta barrier, Cu line, SiOCH ULK) → Structure (a)
- Electrical test before UV-NLA @ M1 level
- 20nm Low-K SiCN deposition
- 120nm SiO₂ (TEOS, 350°C) deposition
- 7 or 20 nm a-Si deposition (LPCVD @ 425°C, Si₂H₆)
- UV-NLA (up to a-Si melt, ~1150°C) → structure (b)
- BS clean + Silicon layer wet etch (TMAH)
- SiO₂ and SiCN dry etch
- Touch CMP → structure (a)
- Electrical test after UV-NLA @ M1 level



3D SEQUENTIAL INTEGRATION : TRANSISTOR & CU LOW-K STABILITY (2)

- ❖ Bottom device thermal stability upon UV-NLA evaluated on 28 nm FD-SOI technology with Cu/ULK @ M1 level.

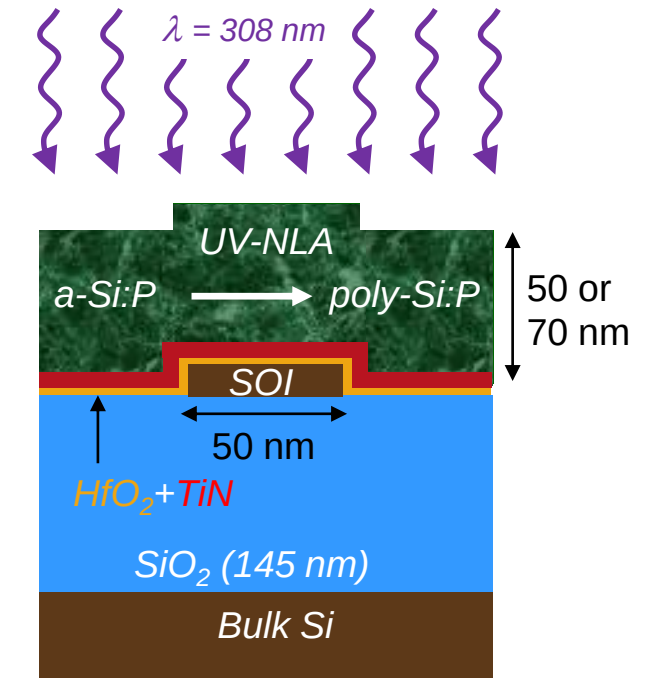


- Cu line resistivity unchanged
- No transistor performance degradation, even beyond the a-Si layer melt threshold (~1150°C)
- UV-NLA fully compatible with 3D integration for the top level processing without degradation of the bottom level.

3D SEQUENTIAL INTEGRATION : GATE ANNEALING (1)

- ❖ High T° ($> 800^\circ\text{C}$) anneals for gate stack densification, Dit curing & mobility enhancement : not possible in 3D integration.
- ❖ Challenges : Low resistance gate & reliability

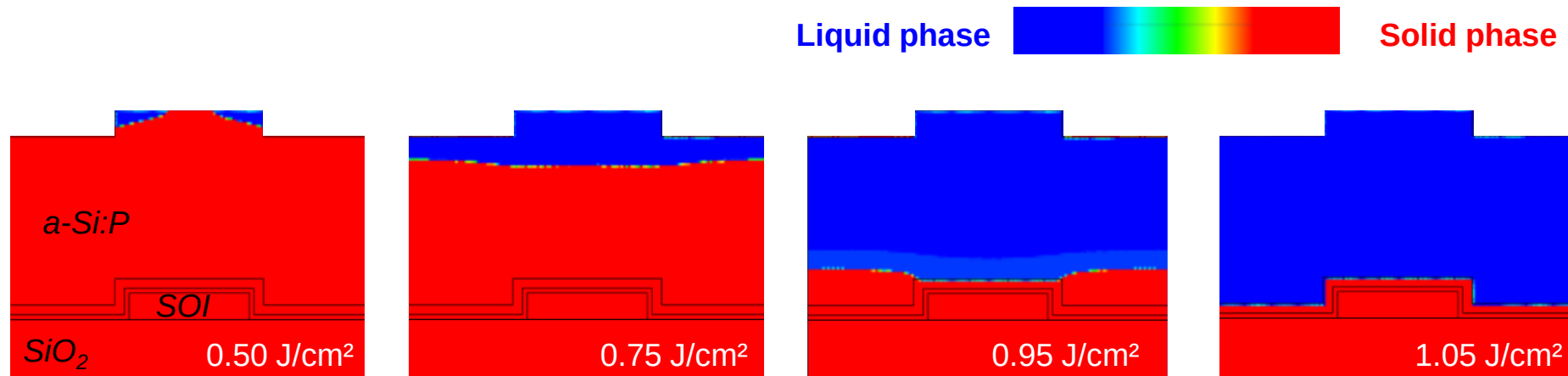
- Active regions patterning, 12 nm thick SOI
- Interlayer + 2 nm HfO_2 + 6 nm TiN deposition
- 50 or 70 nm a-Si:P deposition by LPCVD @ 475°C ($\text{Si}_2\text{H}_6 + \text{PH}_3$)
- **UV Nanosecond Laser Annealing**
- Touch CMP
- Characterization



→ In a gate first approach : UV-NLA developed to crystallize a-Si & activate the dopants

3D SEQUENTIAL INTEGRATION : GATE ANNEALING (2)

- ❖ 2D numerical simulations (LIAB software) :
 - Guidelines for the process conditions (laser energy density range)
 - Temperature as a function of depth and time



S. Kerdilès, ECS Trans. (2019)

- Onset of a-Si:P melt ($\sim 1150^\circ\text{C}$) : $\sim 0.50 \text{ J/cm}^2$
- Full a-Si:P melt : $\sim 1.05 \text{ J/cm}^2$ = **Target**
- SOI channel melt : $\sim 1.20 \text{ J/cm}^2$ → **Detrimental**

3D SEQUENTIAL INTEGRATION : GATE ANNEALING (3)

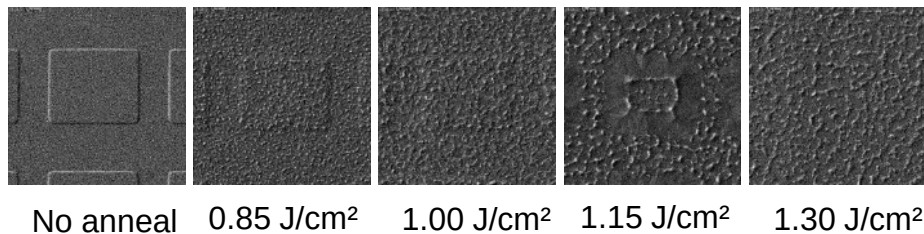
❖ Sheet resistance (70nm Si:P + TiN)

→ Rs optimum @ 'near-complete' Si:P layer melt
 $\rho(\text{Si:P}) = 1.9 \text{ m}\Omega\cdot\text{cm}$ after 1 laser pulse @ 1.15 J/cm^2

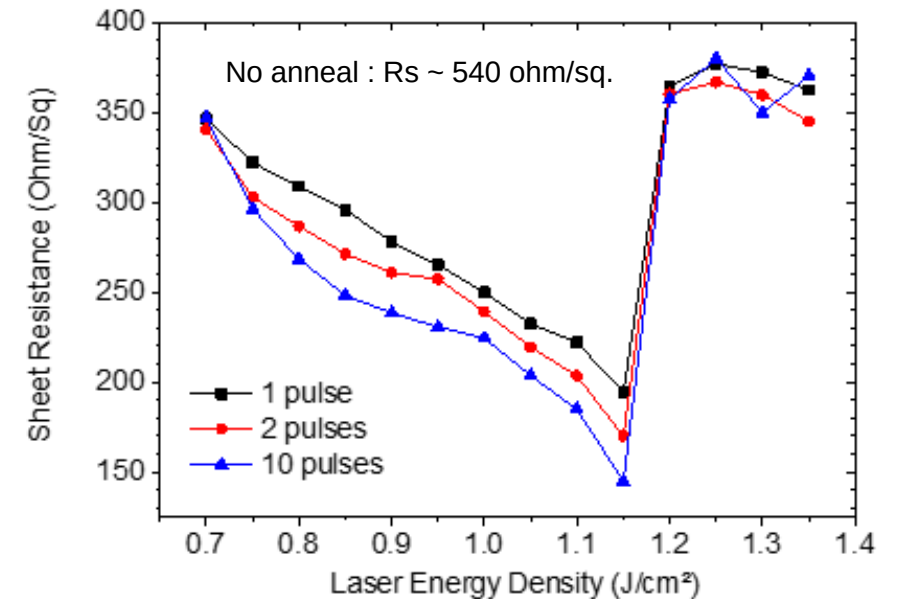
→ Abrupt increase at 1.15 J/cm^2 : full a-Si:P melt (smaller grains)
 → Further improvement in multipulse mode

❖ SEM top view ($5 \times 5 \mu\text{m}^2$) :

→ Maximum surface roughness at the near-complete melt



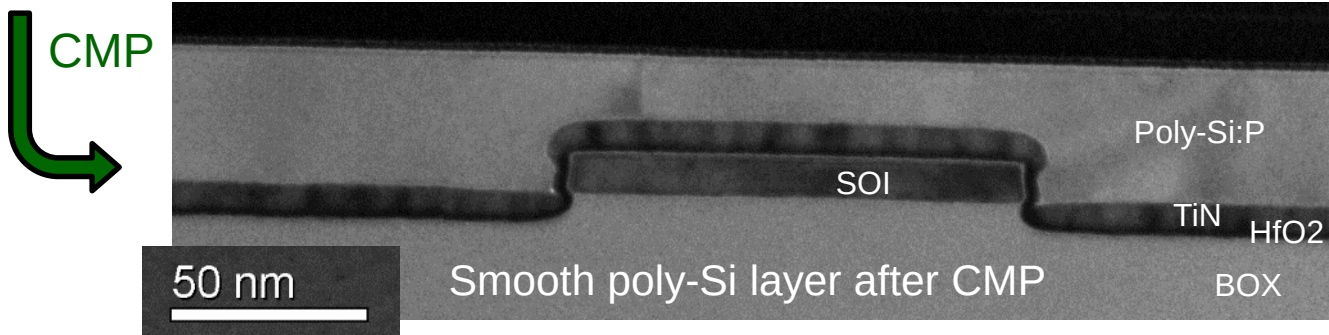
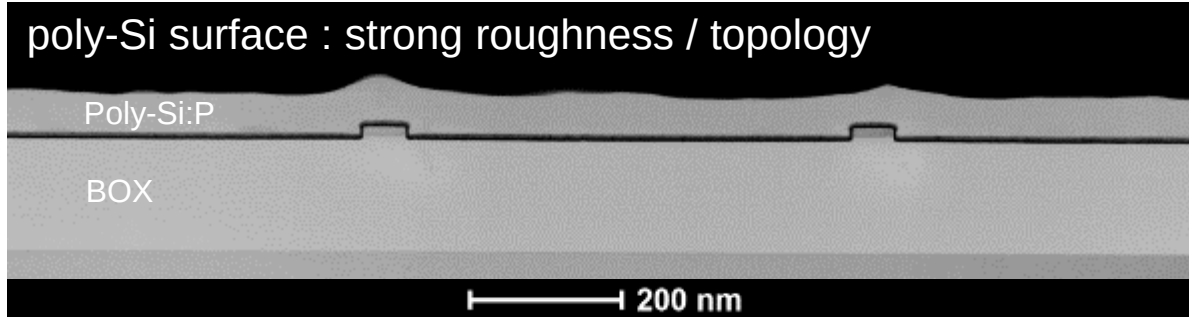
L. Brunet et al., IEDM (2018)



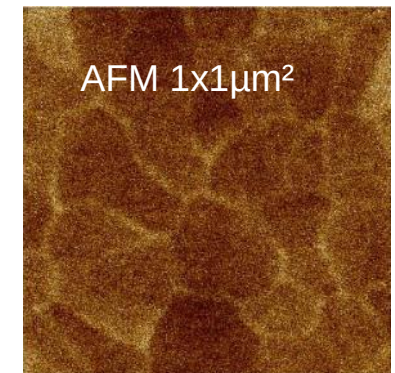
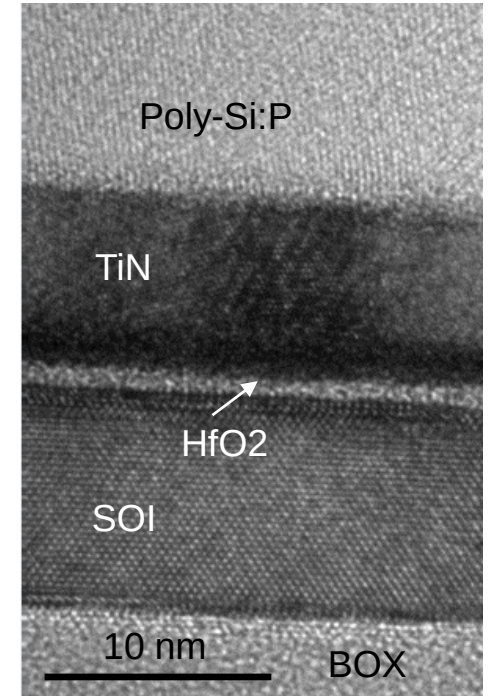
Trade-off to be found between Rs & roughness

3D SEQUENTIAL INTEGRATION : LOW T° GATE STACK

- ❖ Gate stack laser annealing integrated in the 3D-sequential flow (28nm FD-SOI)

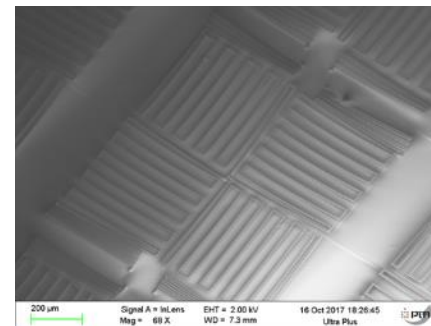
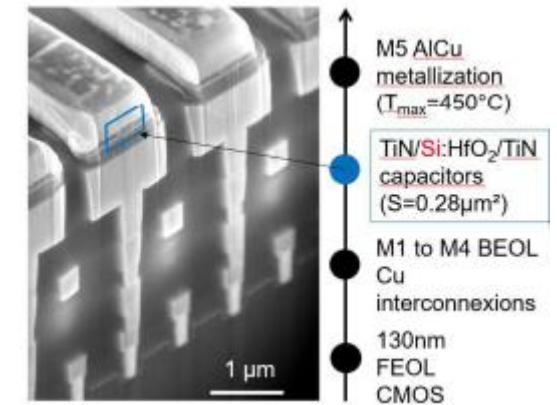
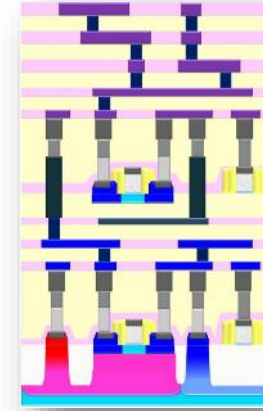


- Efficient smoothing by CMP (20 nm removal)
- Poly-Si grains : 100-300nm
- SOI channel kept monocrystalline



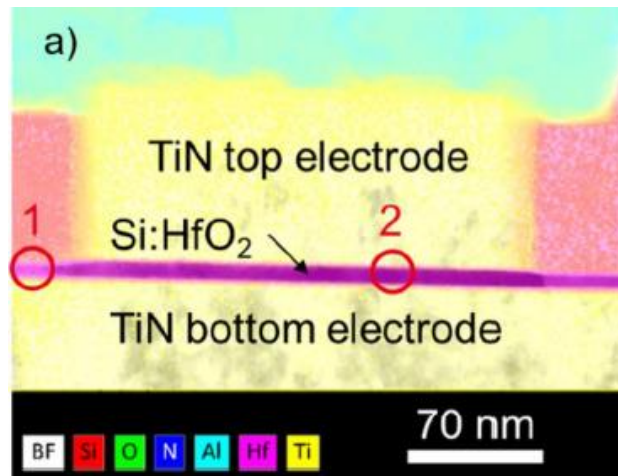
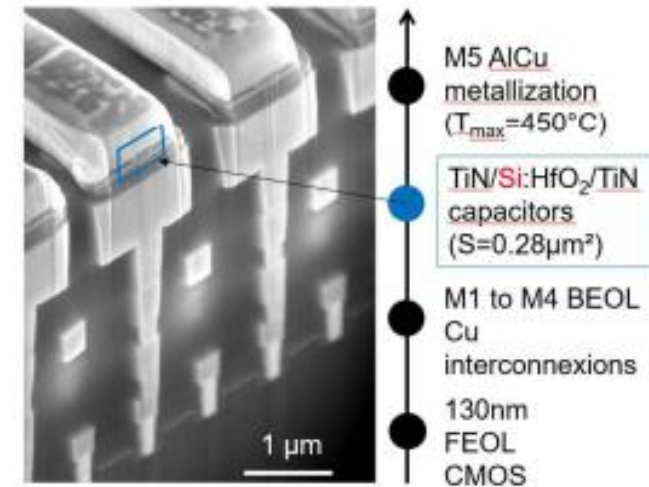
OUTLINE

- ❖ Introduction
- ❖ 3 More than Moore applications :
 - 3D sequential integration, CoolCube™
 - Ferroelectric memories
 - Highly doped Si:B for bolometers & quantum applications
- ❖ Conclusion

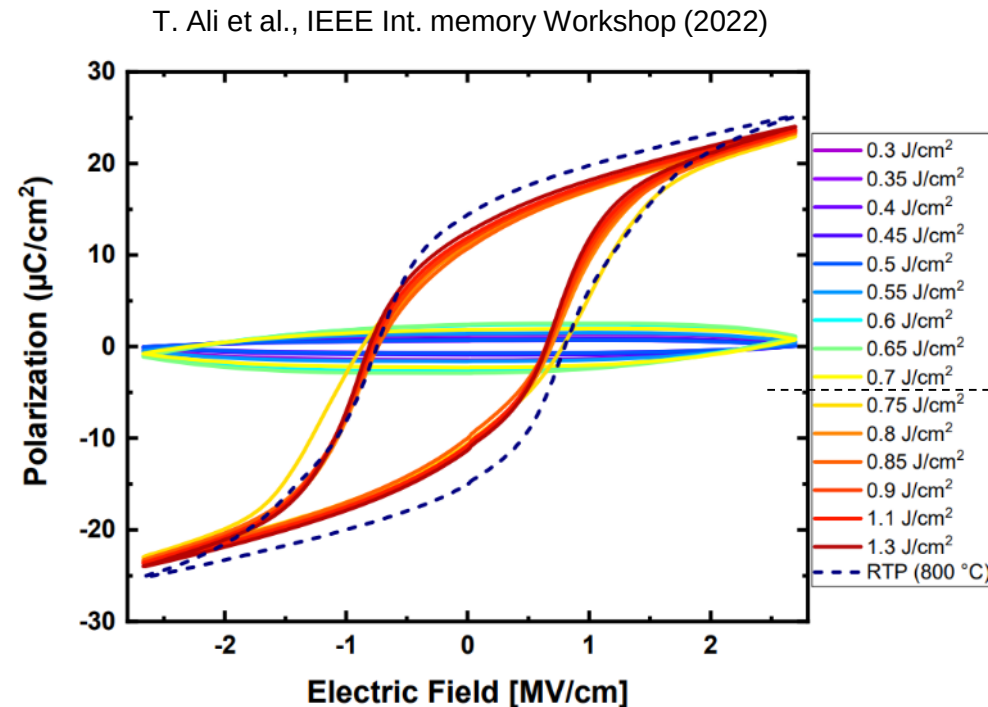


FERROELECTRIC MEMORIES : OPPORTUNITY FOR NLA

- ❖ Hafnium-based oxides actively investigated for CMOS compatible FERAM
 - ❖ Si implantation used to stabilize the ferroelectric phase (orthorhombic phase)
 - ❖ Typical structure : MIM capacitors with TiN top & bottom electrodes
 - ❖ HfO₂: Si crystallization into the appropriate phase : typically RTP > 700°C
- Not compatible with BEOL integration



L. Grenouillet et al., VLSI (2020)



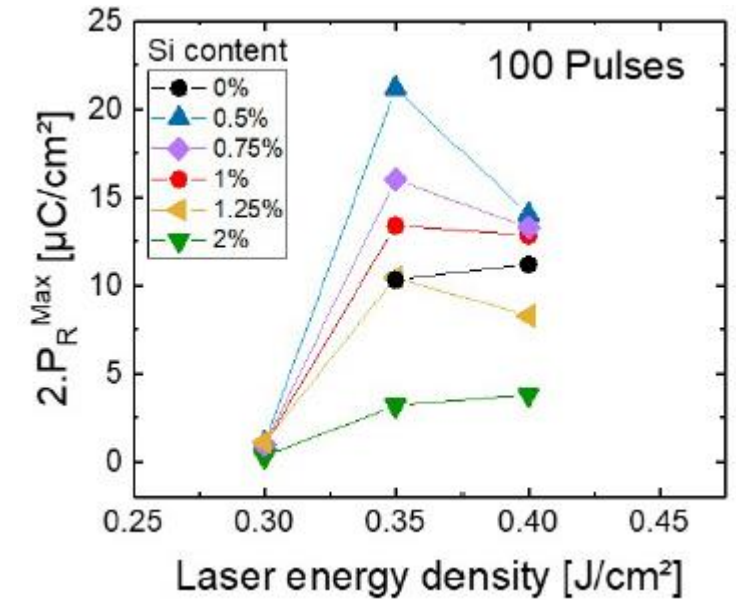
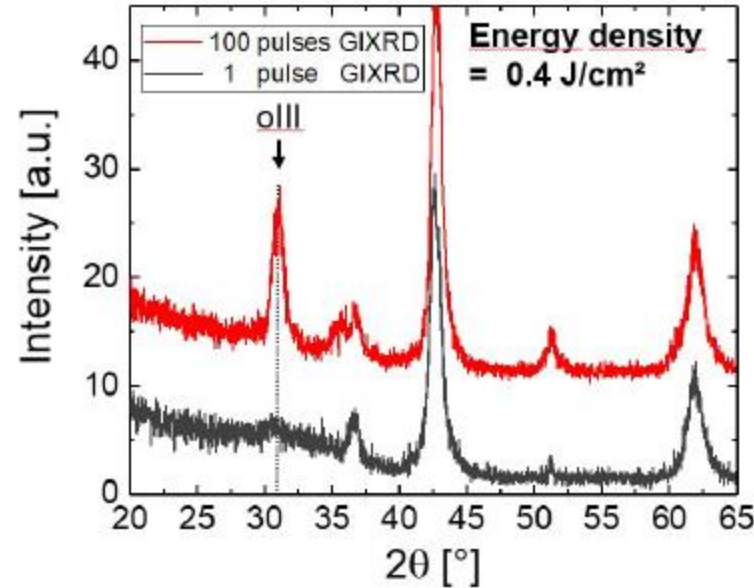
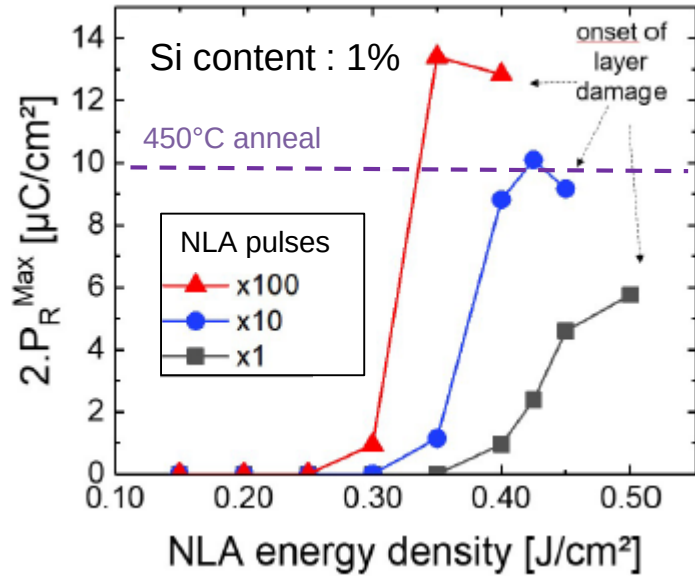
- ❖ But Nanosecond pulsed laser annealing can do it !

- Sub-melt process
- Multipulse mode

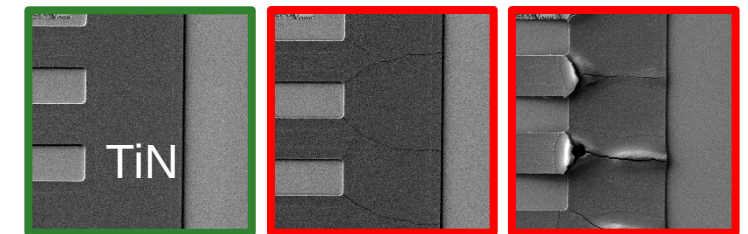
FERROELECTRIC MEMORIES : FIRST TRIALS

TiN / HfO₂:Si / TiN capacitors area : 0.28μm²

L. Grenouillet et al., VLSI (2020)



- HfO₂ with 1% Si : Ferroelectricity demonstrated, with polarization up to 40% higher than with a 450°C anneal. Orthorhombic phase obtained. Cumulative effect with the number of pulses = lateral grains growth
- Laser energy density (ED) limitation : TiN top electrode damage
- Si content : 0.5% = optimum

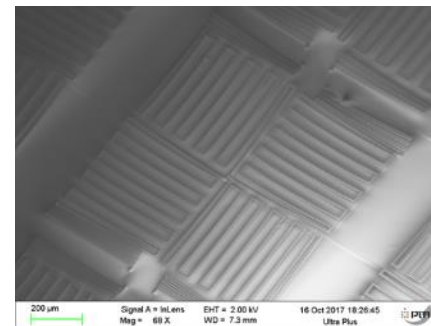
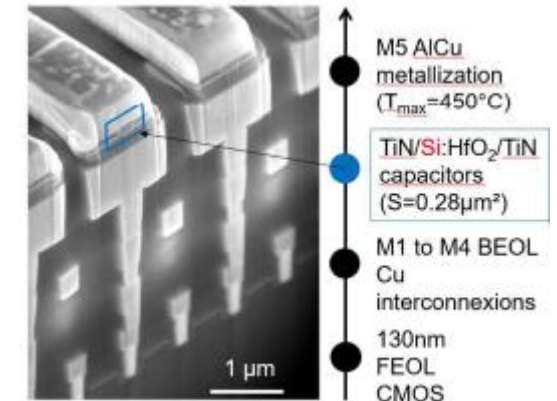
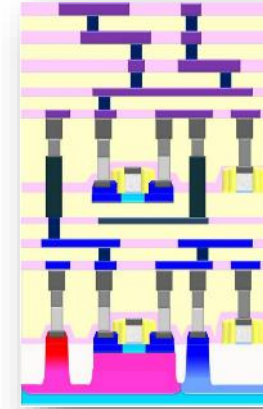


ED

$2P_R$ values beyond 20 $\mu C/cm^2$ can be obtained using UV-NLA in a BEOL-compatible integration

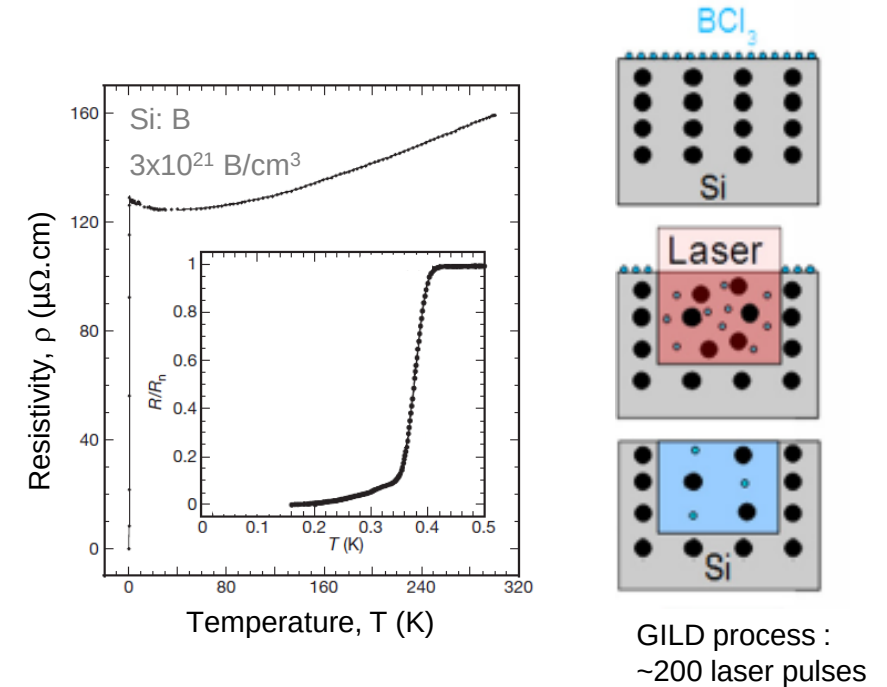
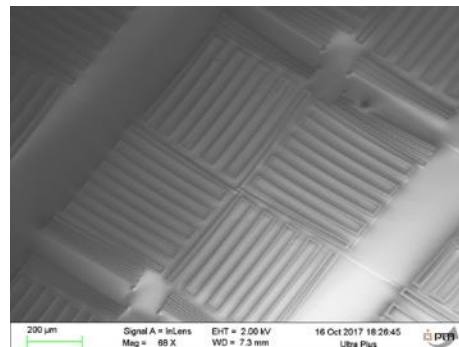
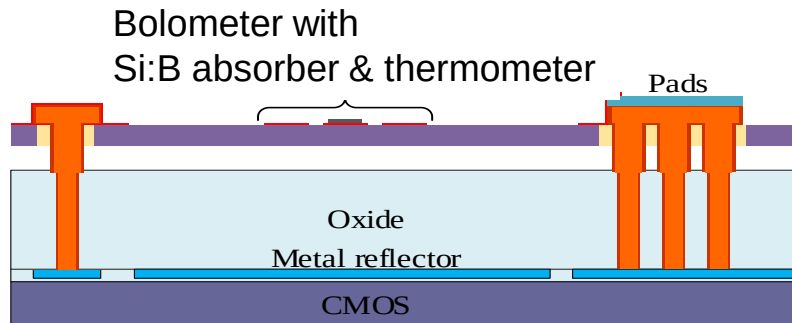
OUTLINE

- ❖ Introduction
- ❖ 3 More than Moore applications :
 - 3D sequential integration, CoolCube™
 - Ferroelectric memories
 - Highly doped Si:B for bolometers & quantum applications
- ❖ Conclusion



SUPERCONDUCTING SILICON

- ❖ 2006 : Discovery of superconductivity in highly boron doped Si by Gas Immersion Laser Doping (GILD), i.e BCl_3 adsorption on Si in UHV + multi-pulse laser anneal
 - ❖ Critical temperature never exceeding 0.7 K, so far.
 - ❖ Si:B : candidate for superconducting Qbits & bolometers for astrophysics operating at 50-100mK (absorber) thanks to its compatibility with large scale integration.
- Transfer of a blanket Si:B layer onto CMOS devices.



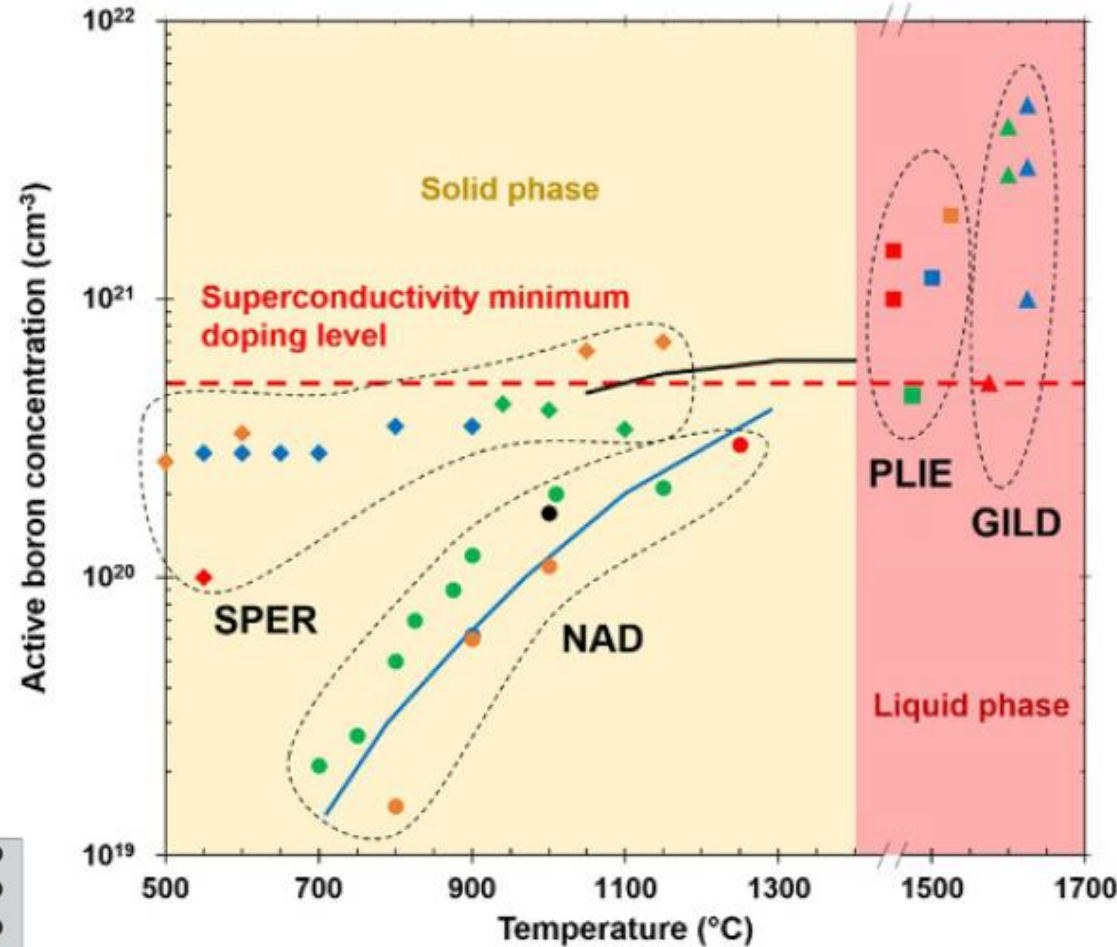
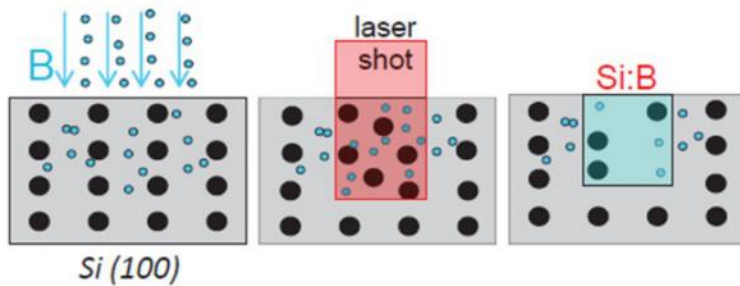
E. Bustarret et al., Nature (2006)

PATH TO HIGH ACTIVE BORON CONCENTRATION

❖ High $[B]_{\text{active}}$: liquid phase

❖ GILD not industrial

→ LETI investigating Pulsed Laser Induced Epitaxy (PLIE), combining ion implantation & UV-NLA at atmospheric pressure with a large beam.



F. Chiodi et al., Chapter 9 in 'Laser annealing processes in semiconductor technology', Elsevier (2021)

Solid phase

Solid solubility references

— [Trumbore1960]

— [Borisenko1987]

Non-Amorphizing Doping (NAD)

● BCl_3 + furnace [Fuller1954]

● B_2O_3 + furnace [Vick1969]

● Implantation + furnace [Schwettmann1974]

● Implantation + furnace [Ryssel1980]

● Implantation + furnace [Tsien1981]

Solid Phase Epitaxy Regrowth (SPER)

◆ PAI^1 + implantation + furnace [Tsai1979]

◆ PAI + implantation + furnace [Landi1988]

◆ PAI + implantation + RTA² [Solmi1990]

◆ PAI + implantation + FLA³ [Jain2004]

Liquid phase

Pulsed Laser Induced Epitaxy (PLIE)

■ B_2O_3 + NLA⁴ [Young1978]

■ Implantation + NLA [Tsien1981]

■ Implantation + NLA [Masetti1983]

■ Implantation + NLA [Solmi1990]

Gas Immersion Laser Doping (GILD)

▲ BCl_3 + NLA [Kerrien2002]

▲ BCl_3 + NLA [Bustarret2006]

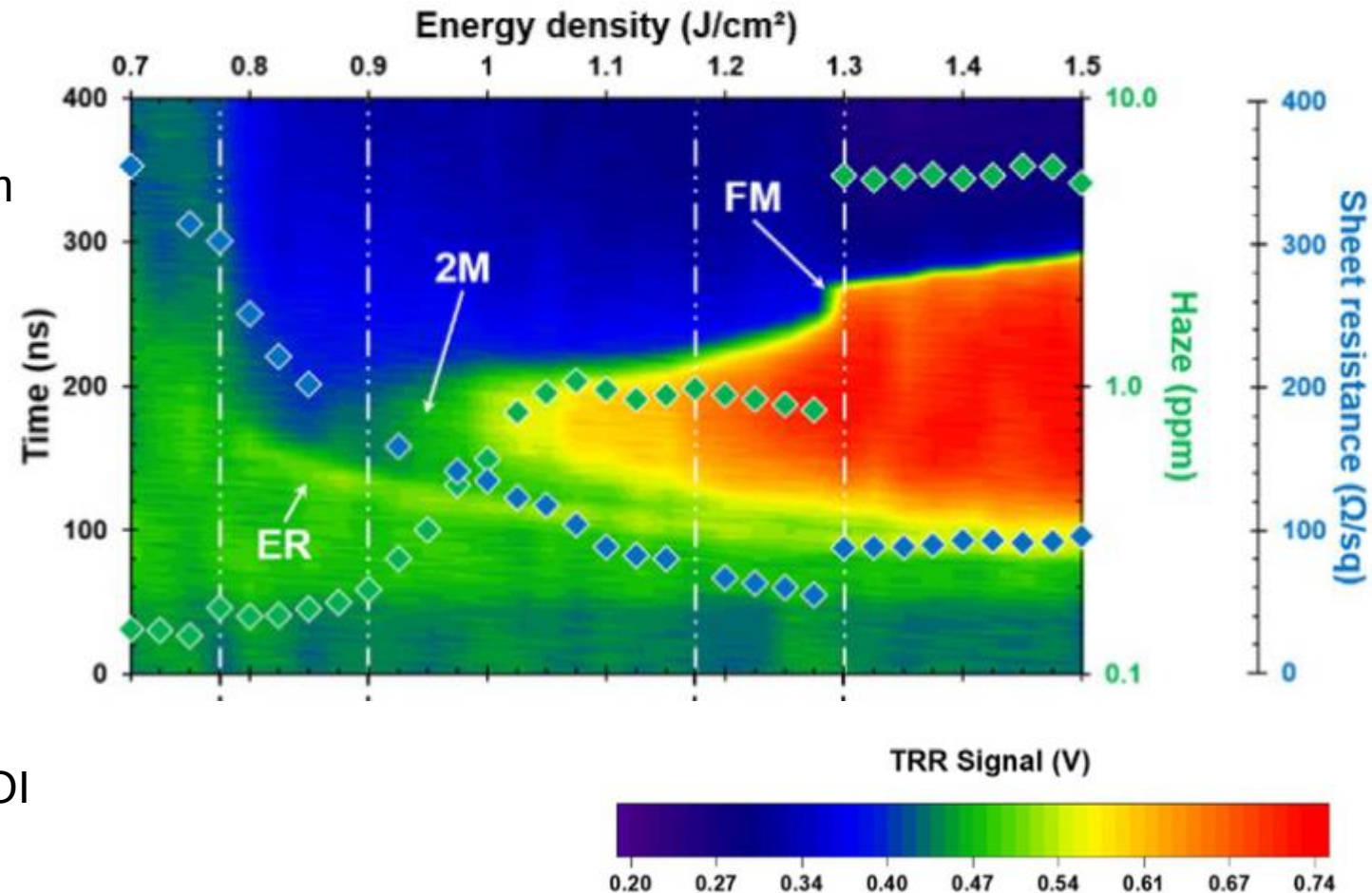
▲ BCl_3 + NLA [Marcenat2010]

Si:B SAMPLES PREPARATION

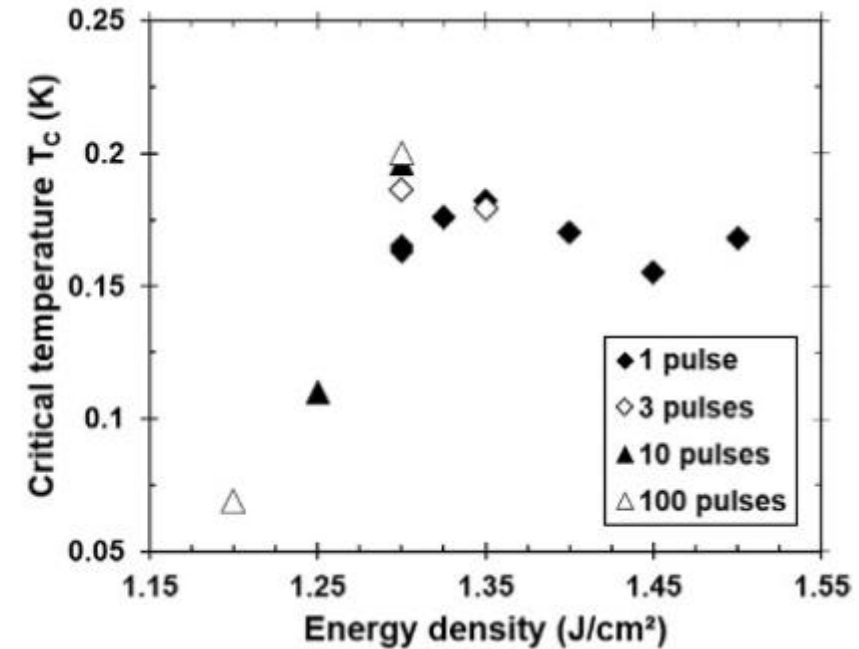
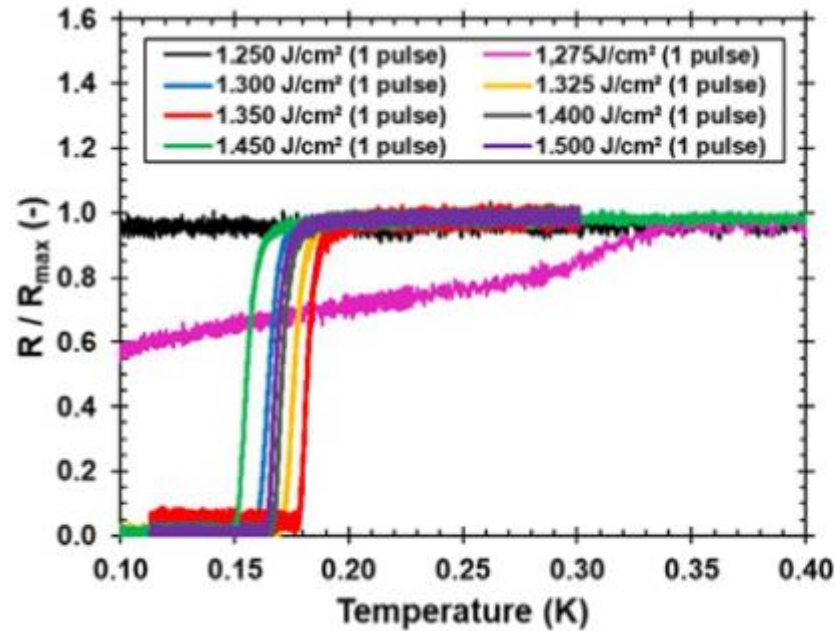
PLIE sequence :

- ❖ Starting material : SOI 34 nm / BOX 20nm
- ❖ 2.5×10^{16} B/cm² implantation
→ Amorphized depth : 15 nm
- ❖ Laser annealing
→ Full SOI melt detected @ 1.3 J/cm²

Superconductivity expected below this full SOI melt threshold ...



SUPERCONDUCTIVITY IN Si:B SAMPLES OBTAINED BY PLIE



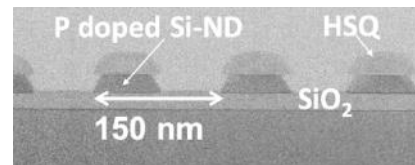
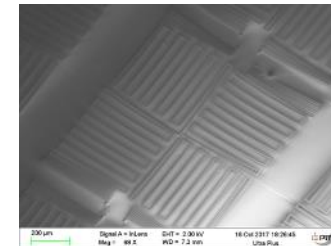
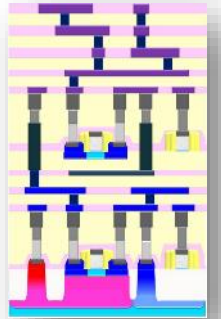
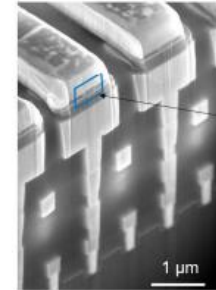
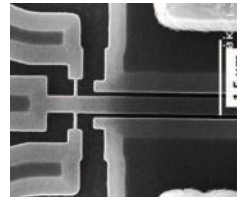
- ❖ Superconductivity obtained in Si:B samples
- ❖ Surprisingly for polycrystalline SOI layers (i.e. $ED \geq 1.3 \text{ J/cm}^2$ for 1 pulse)
- ❖ Critical temperature still to be improved (ideally 0.5 K)
- ❖ Superconductivity remains after anneal @ 500°C → compatible with our bolometers flow

F. Chiodi et al., Chapter 9 in 'Laser annealing processes in semiconductor technology', Elsevier (2021)

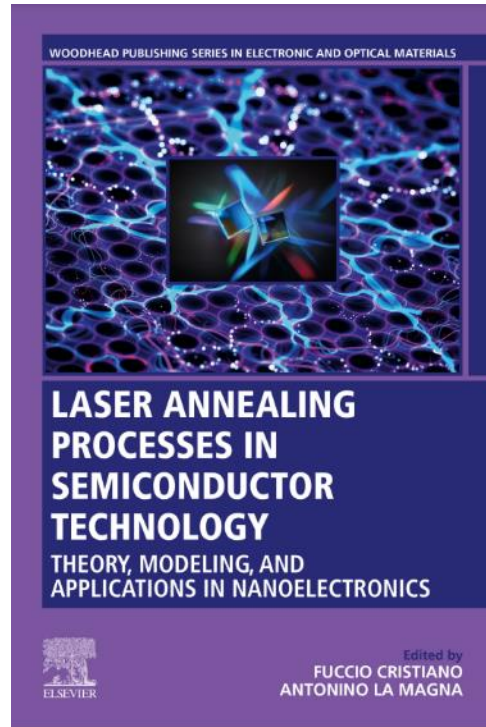
R. Daubriac et al., ECS-J. Sol. State Sci. Technol. **10** 014004 (2021)

CONCLUSION

- ❖ **Nanosecond laser annealing (NLA)**, especially with a UV radiation, enables surface annealing with an **excellent in-depth selectivity**
- ❖ NLA : technique of choice to **overcome thermal budget limitations** in various **3D** architectures
 - ❖ 3D sequential integration : gate stack annealing & possibly S/D dopant activation
 - ❖ Ferroelectric memories integrated in the BEOL
 - ❖ MEMS above IC
 - ❖ ...
- ❖ NLA also enables very **high active dopant concentrations**
 - ❖ Superconducting Si for bolometers in astrophysics
 - ❖ Plasmonics



TO LEARN MORE ABOUT
NANOSECOND LASER
APPLICATIONS :



THANK YOU FOR YOUR ATTENTION

CEA-Leti, technology research institute
Commissariat à l'énergie atomique et aux énergies alternatives
Minatec Campus | 17 avenue des Martyrs | 38054 Grenoble Cedex | France
www.leti-cea.com

