



DE LA RECHERCHE À L'INDUSTRIE

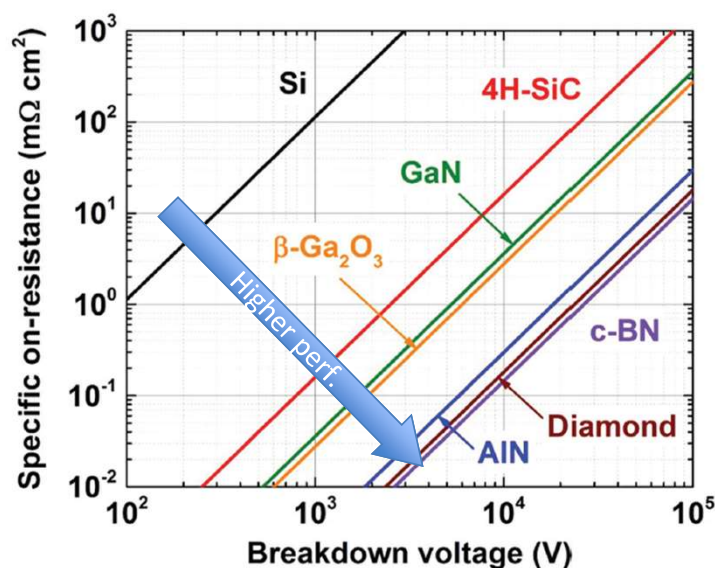
Overview of the normally-OFF GaN-on-Si MOSc HEMT transistor in the fully recessed gate architecture

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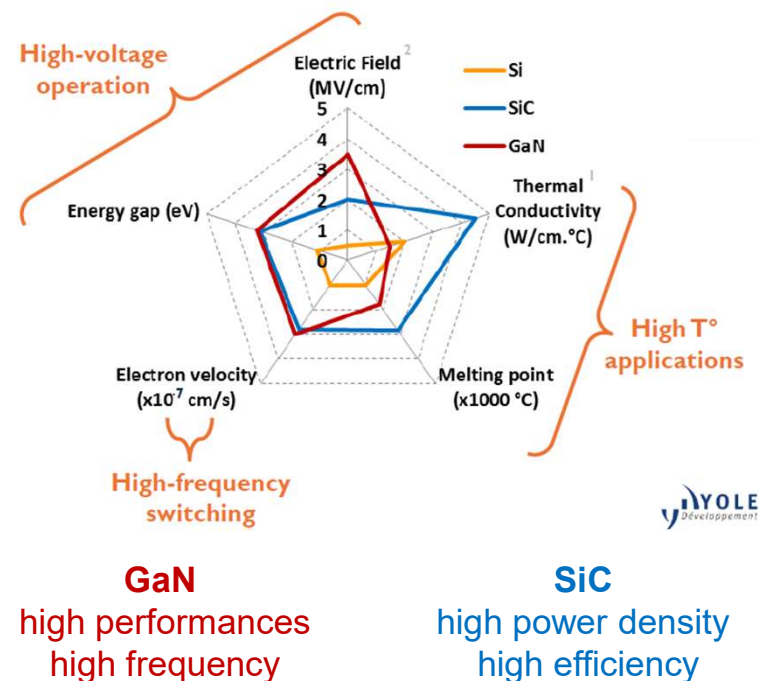
- **Why GaN MOSc HEMT power devices ?**
- **Advantages & Challenges of recessed-gate architecture**
- **Takeaway messages**

Figure-of-merit of WBG semiconductors for unipolar vertical switches at low frequency



J.Y. Tsao et al. *Advanced Electronic Materials* (2018)

Properties of Si, SiC and GaN materials

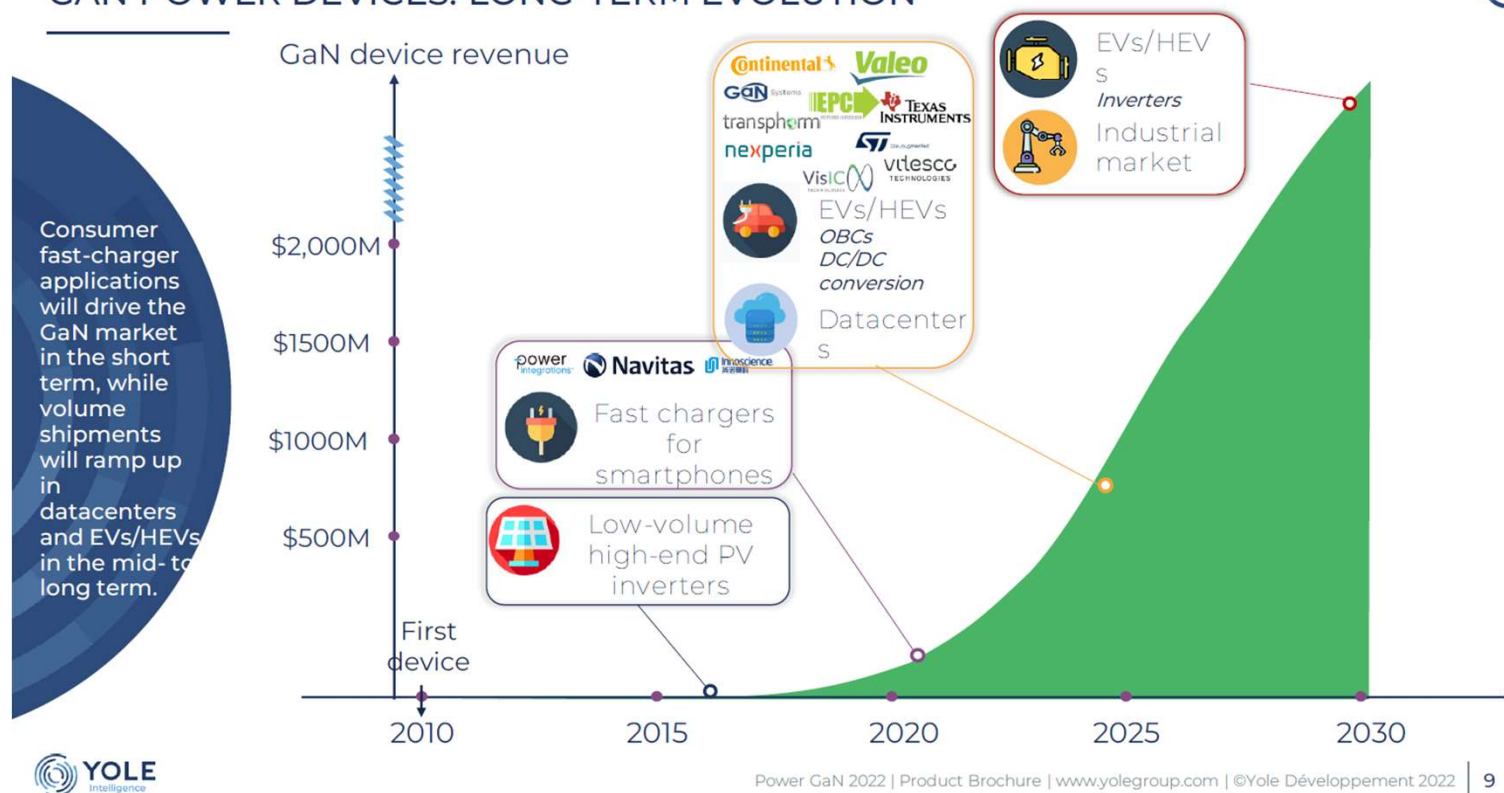


Ana Villamor / Yole Développement, présenté à APEC (2019)

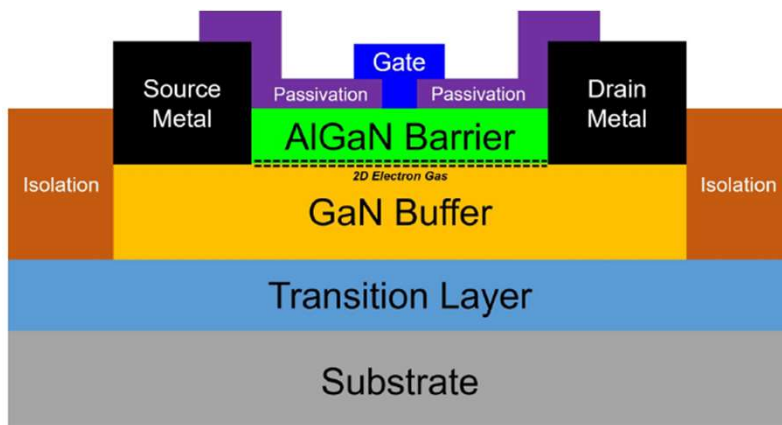
→ **GaN devices target high performances and high frequency applications.**

GaN POWER DEVICES: LONG-TERM EVOLUTION

« GaN is **for high performance and high frequency solutions**, as well as size reduction at a reasonable cost in long term »
A. Villamor, Yole Devt at APEC'2019



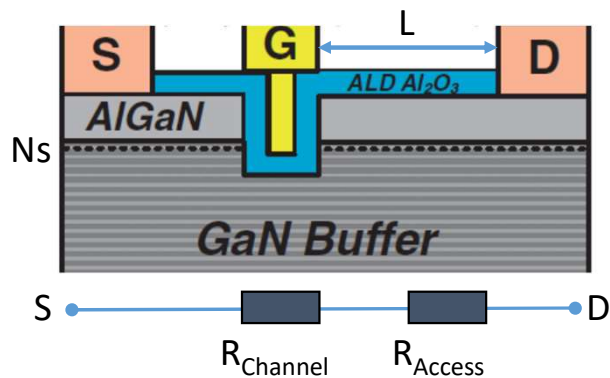
<https://www.yolegroup.com/product/report/power-gan-2022/>
Extract from the product brochure



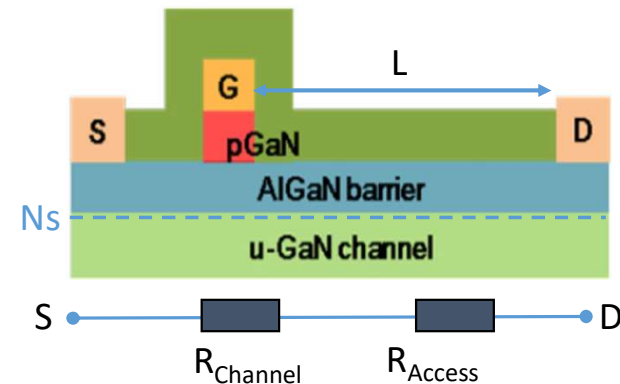
AlGaN / GaN HEMT schematic cross section

→ Normally-ON device

B.N. Pushpakaran et al. Journal of electronic materials (2020)

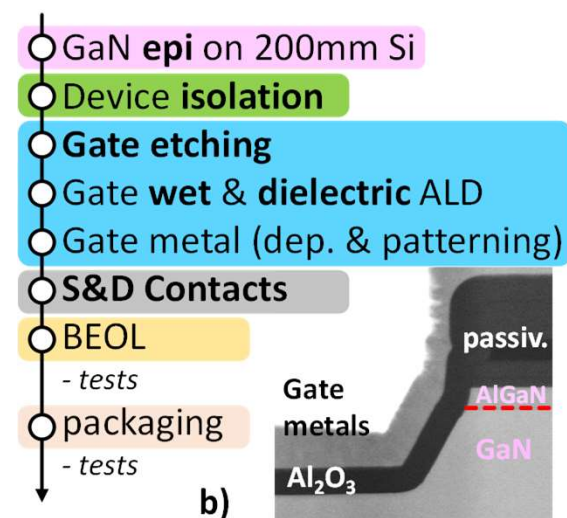
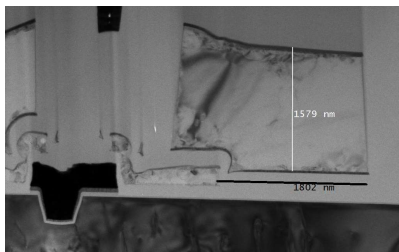
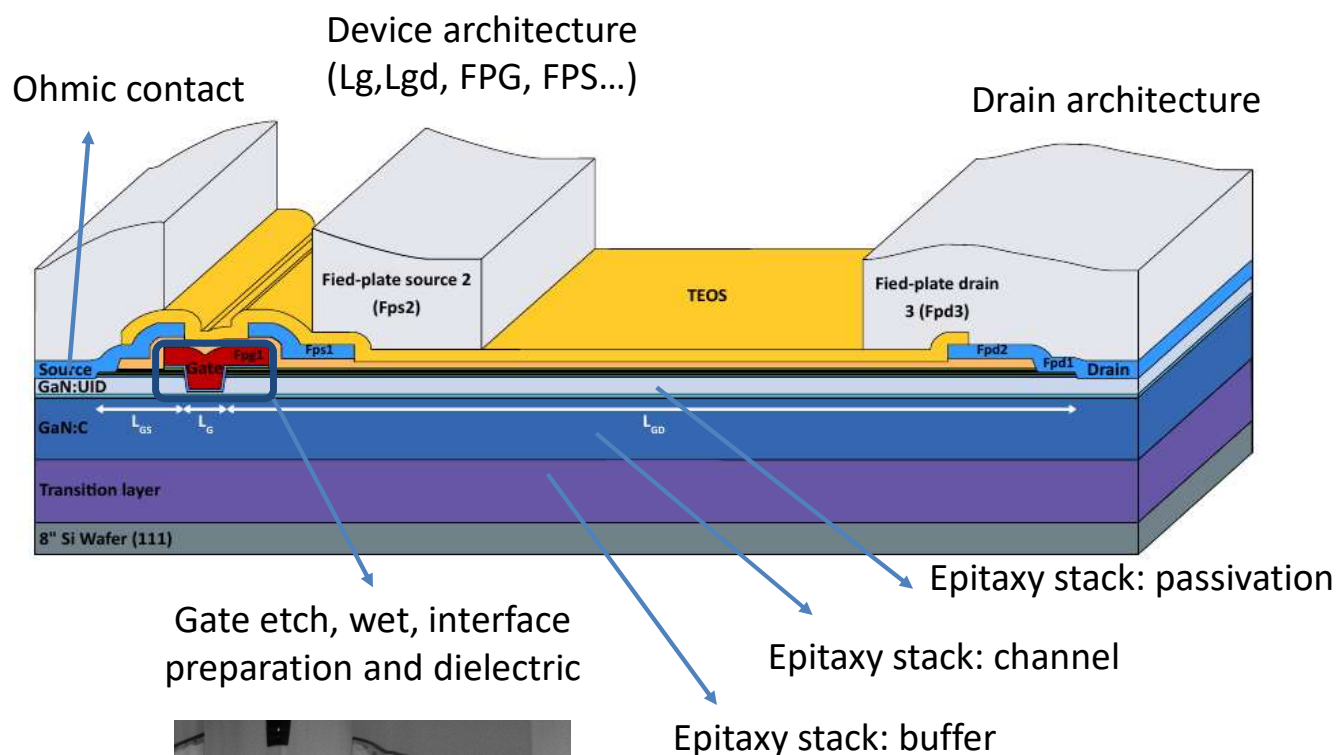


MOSc HEMT: V_t depends upon
channel engineering
(GaN doping, back barrier)



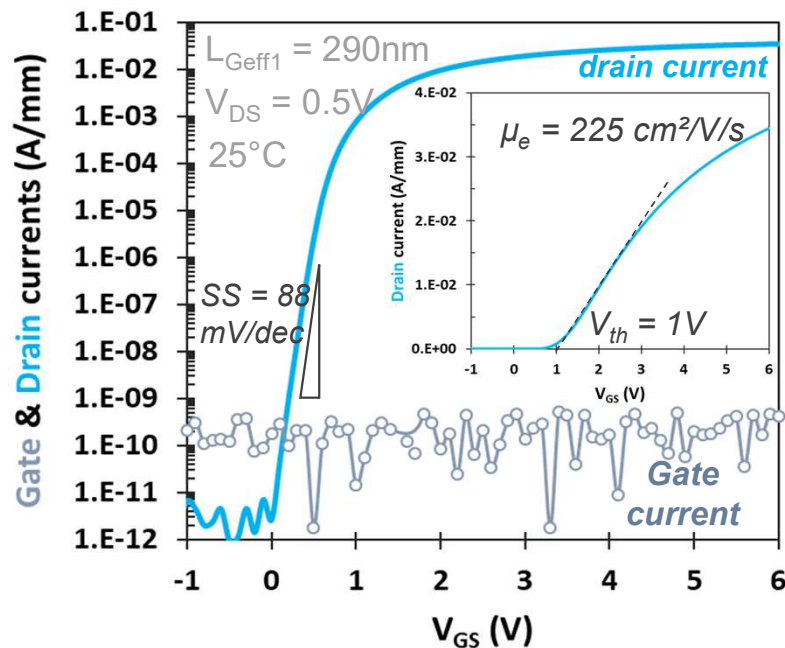
pGaN Gate: V_t depends upon
N_s determined by AlGaN barrier
(among others)

	MOS HEMT	pGaN GATE
PROS	Lower R _{access} Smaller R(T) degradation Higher V _g allowed	Low R _{channel} (2DEG) Better stability (no GaN // dielectric interface)
CONS	High R _{channel} Higher V _{th} instability (trapping in dielectric)	Higher R _{access} Larger R(T) degradation Lower allowed V _g max



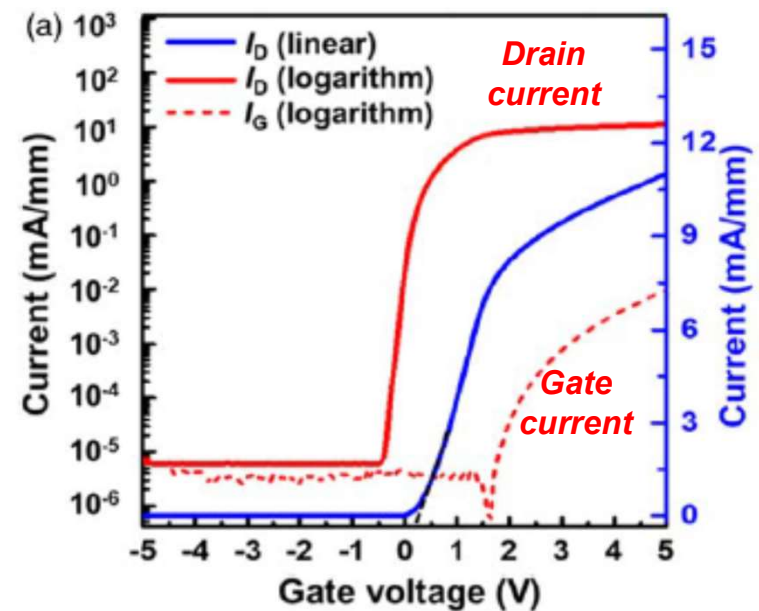
Our recess-gate MOS-HEMT

C. Le Royer et al., ISPSD (2022)



State-of-the-art pGaN device

C. Zeng et al., Appl. Phys. Express 12, 121005 (2019)



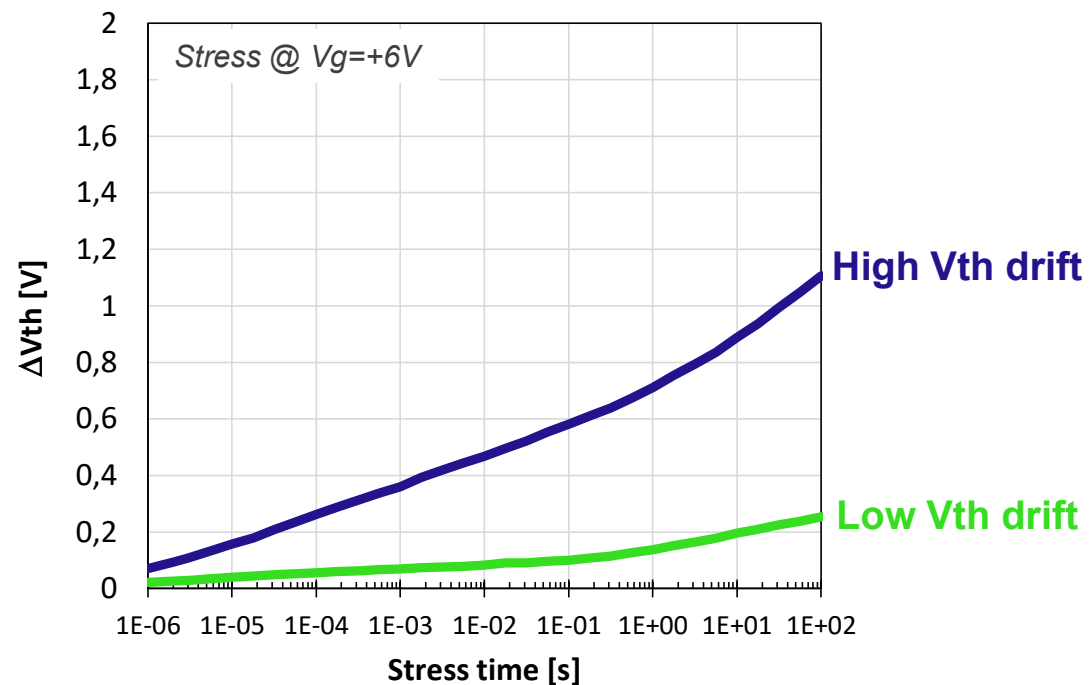
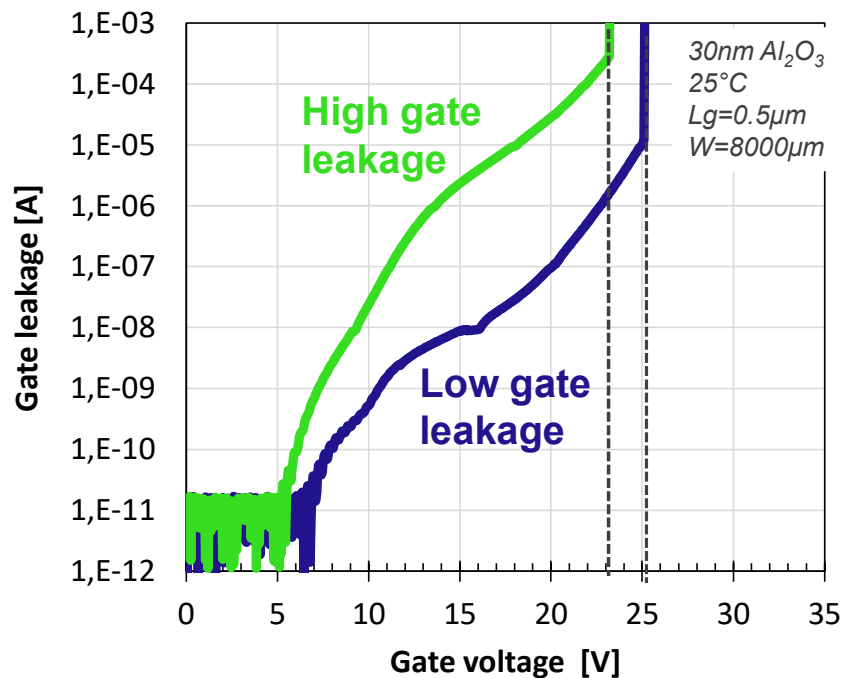
Several orders of magnitude lower gate leakage current with MIS-gate
 → Higher gate voltage overdrive (theoretically) allowed

Internal data with 2 different Al_2O_3 processes

Al_2O_3 process 1

Al_2O_3 process 2

R. Gwoziecki et al., GaN Marathon (2022)

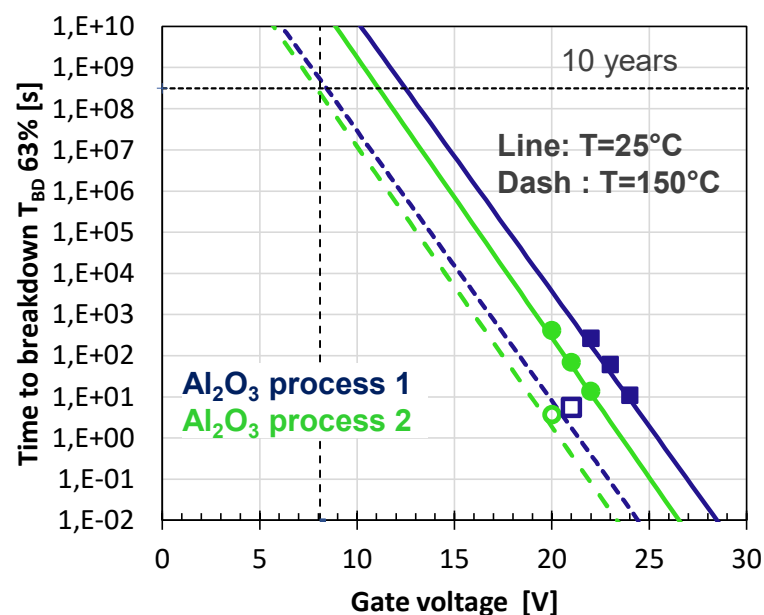
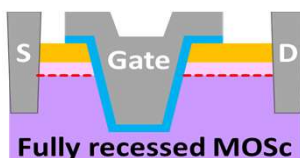


- High gate breakdown voltage whatever the diel process (larger than 20V for 30nm $\text{Al}_2\text{O}_3 > 7\text{MV/cm}$)
- Competition / tradeoff between leakage level & trapping (BTI)

Our recess-gate MOS-HEMT

Vg > 8V @ 10 years

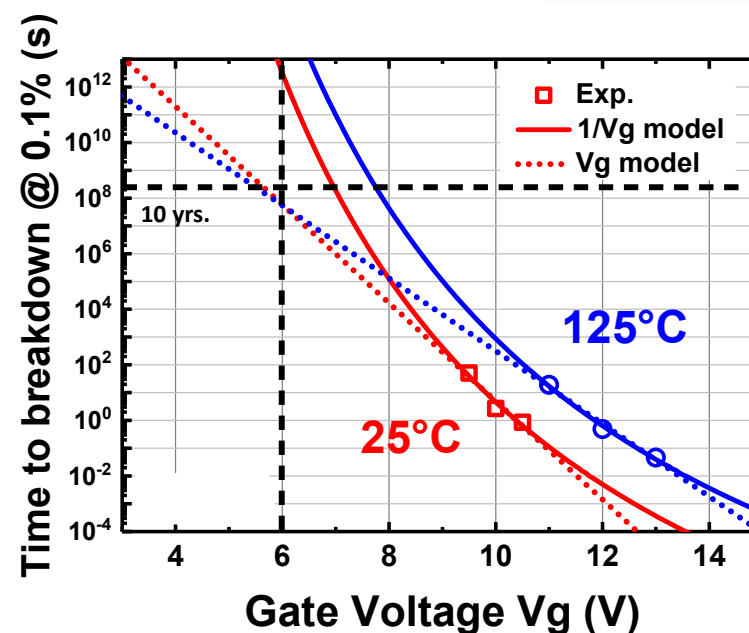
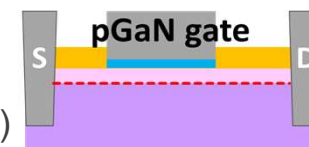
R. Gwoziecki et al., GaN Marathon (2022)



pGaN device

Vg 5 - 8V @ 10 years

(depends on extrapolation model)

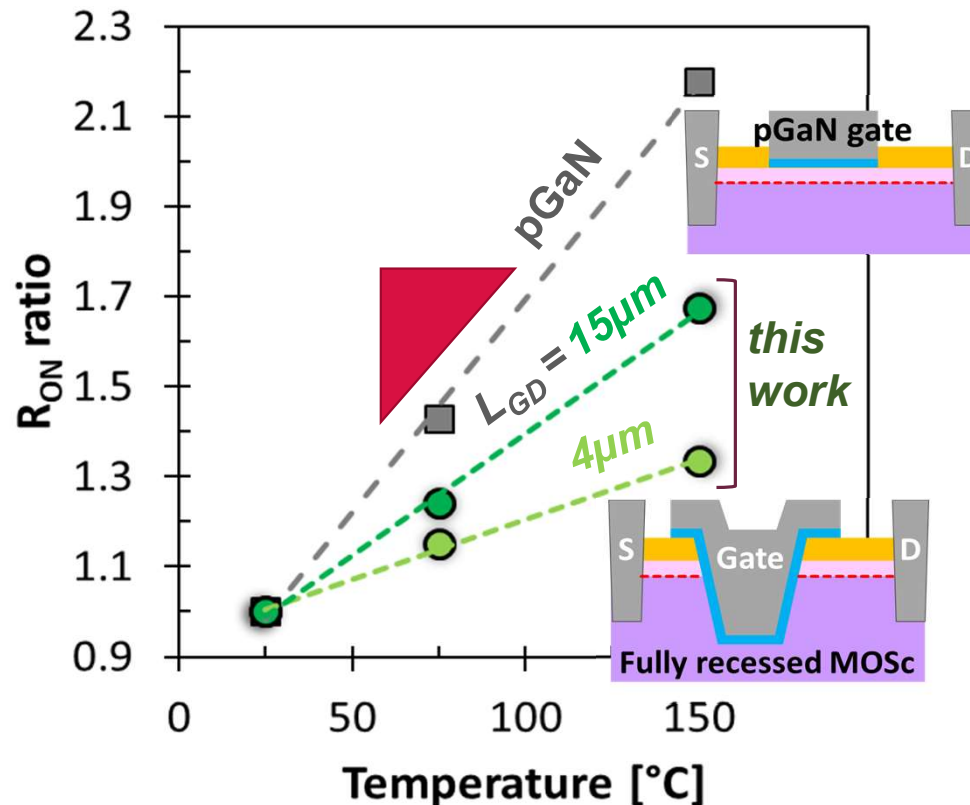


Higher Tddb for dielectric showing lower gate leakage

Max $V_g > 8\text{V}$ for 10 years lifetime @ 150°C for a 30nm Al_2O_3

Similar to pGaN but increasing the dielectric thickness is allowed !

ADVANTAGE OF RECESSED MOS-HEMT: LOWER INCREASE OF R_{ON} WITH TEMPERATURE

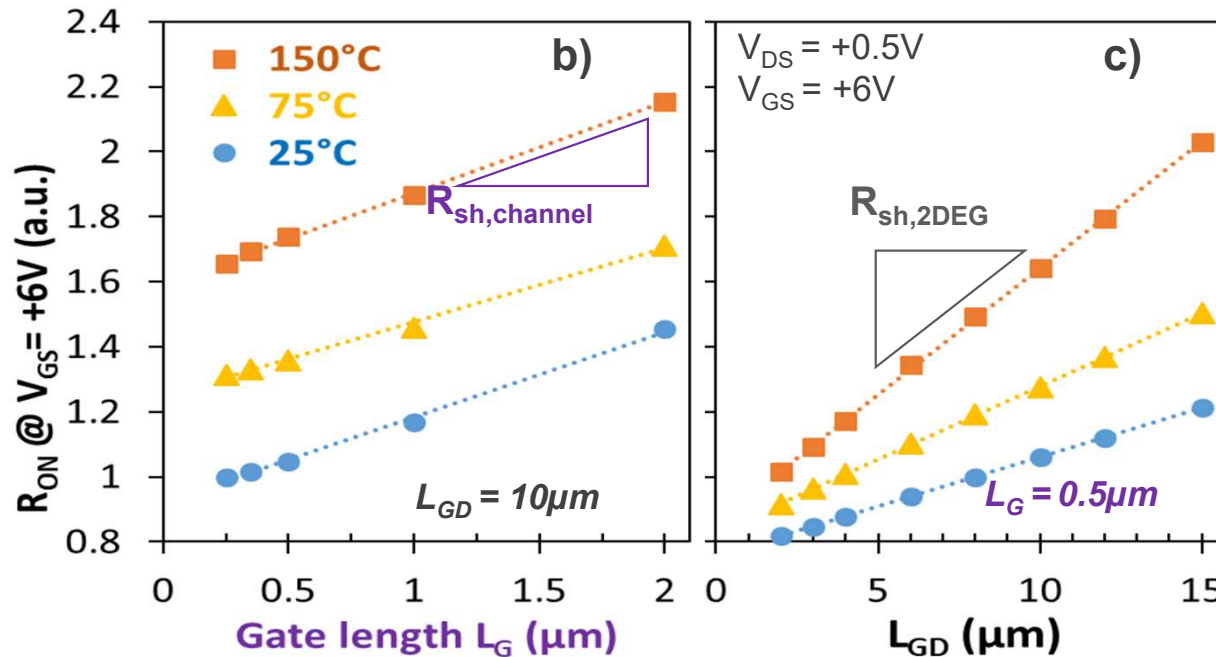


pGaN: IGT60R070D1 data sheet:
600V CoolGaN™ E-mode Power
Transistor, 2020-05-29

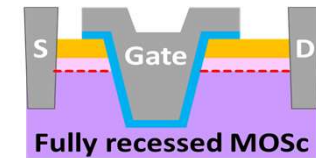
MOSc HEMT : our work
C. Le Royer, ISPSD 2022

- Benefits of lower mobility degradation for channel inversion layer than for the 2DEG layer
- ➔ Better performance for recess MS-gate at high temperature

ADVANTAGE OF RECESSED MOS-HEMT: TEMPERATURE DEPENDANCE OF CHANNEL AND ACCESS RESISTANCE



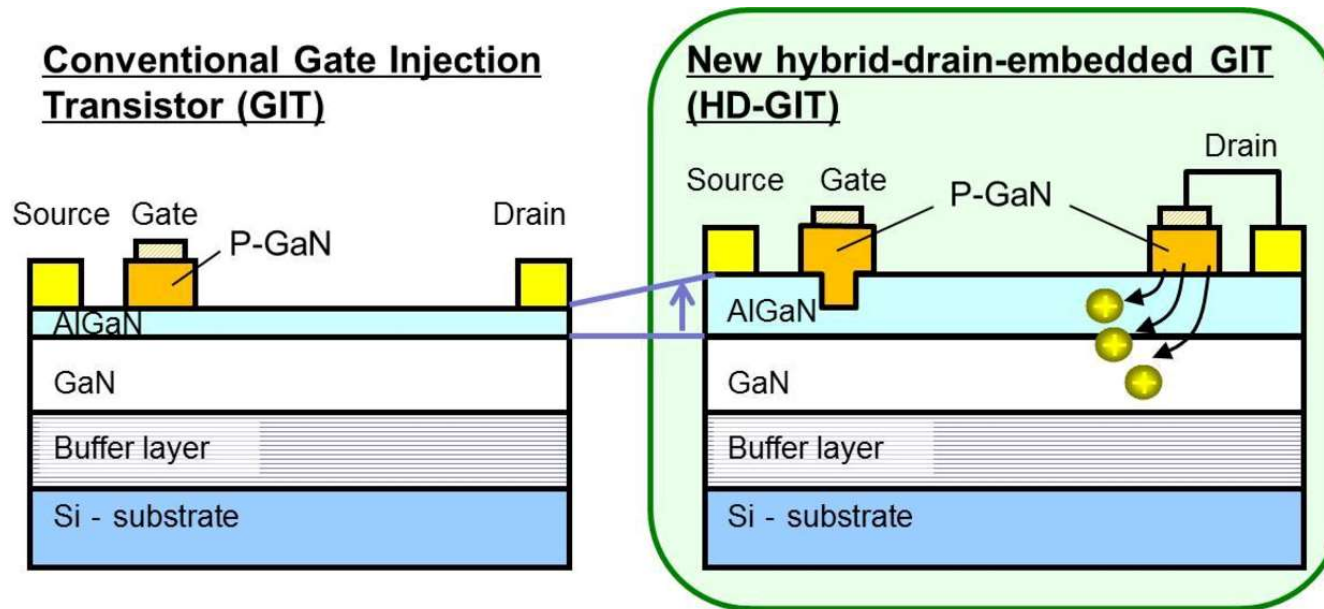
C. Le Royer, ISPSD 2022



➤ Benefits of lower mobility degradation for channel inversion than 2DEG

- $R_{channel}$ increase by only ~20% from 25°C to 150°C
- R_{2DEG} increase by a factor 2,2 to 2,5 (higher mobility at low temp but higher degradation)

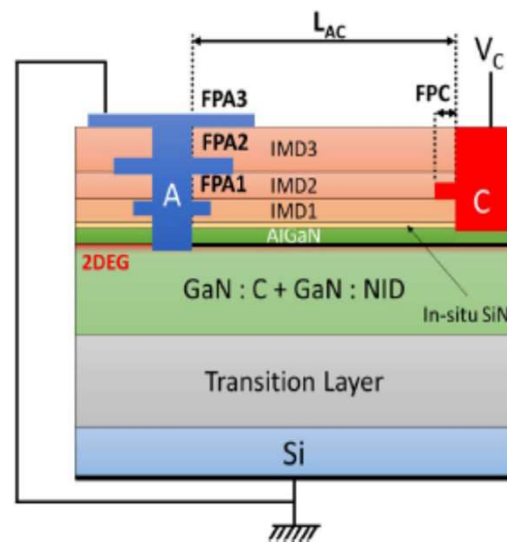
DYNAMIC PERFORMANCES : HOW TO REDUCE CURRENT COLLAPSE WITH pGAN- GATE



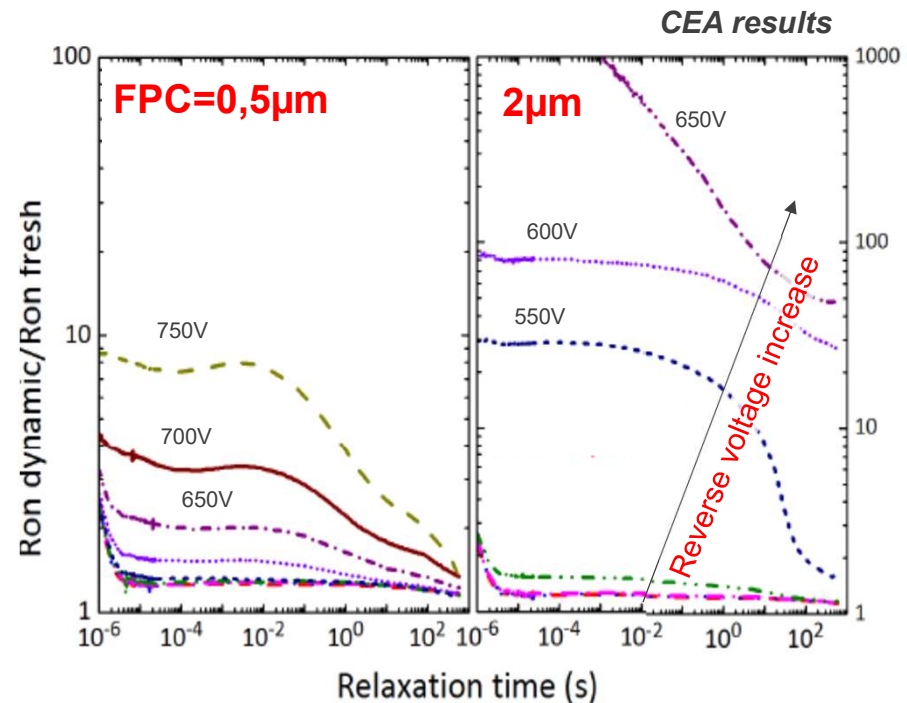
- Use the pGaN layer for Gate but also to inject hole to compensate electron trapping

http://www.how2power.com/newsletters/1509/articles/H2PToday1509_design_Panasonic.pdf?NOREDİR=1

DYNAMIC PERFORMANCES: CURRENT COLLAPSE REDUCTION FOR RECESSED MOS-HEMT



GaN-on-Si SBD structure
FPC = Cathode Field Plate length

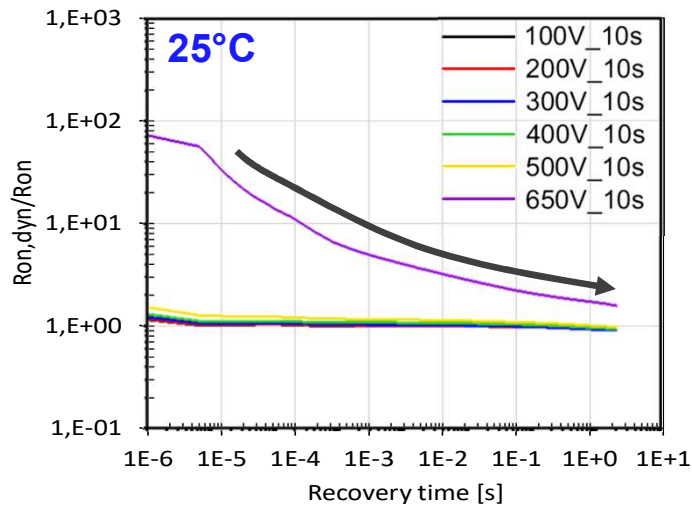


Lorin et al.: On the Understanding of Cathode Related Trapping Effects in GaN-on-Si Schottky Diodes DOI: 10.1109/JEDS.2018.2842100

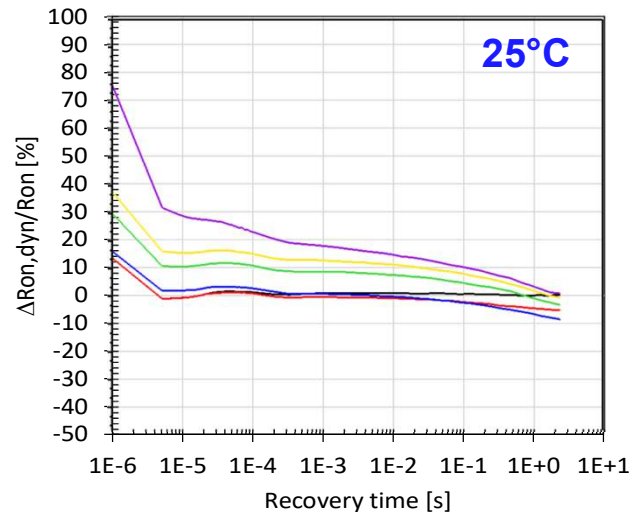
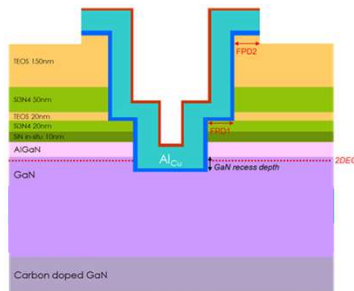
- Cathode (aka Drain) architecture optimization (field plate, passivation) is effective to reduce the current collapse (limitation of electron trapping in passivation)

DYNAMIC PERFORMANCES: CURRENT COLLAPSE REDUCTION FOR RECESS MOS-HEMT

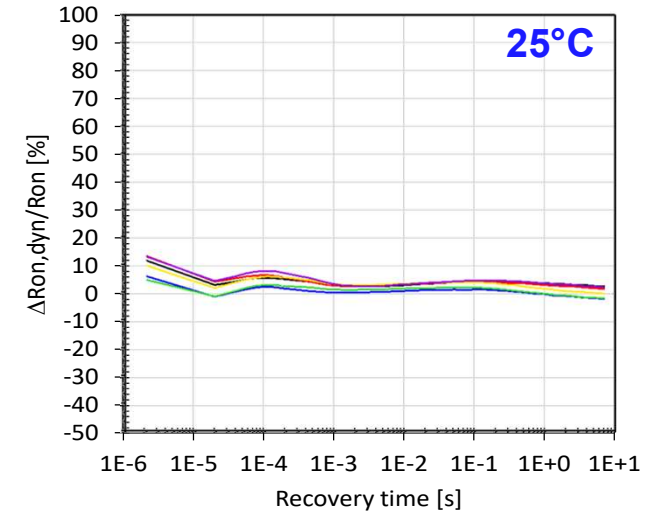
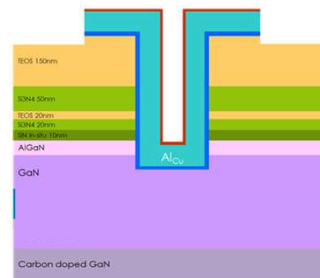
R. Gwoziecki et al.,
GaN Marathon (2022)



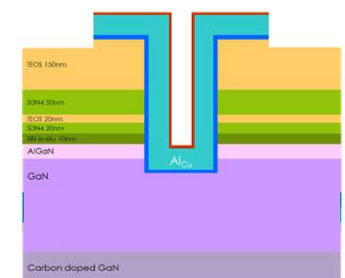
Previous process



Thick passiv. under FP

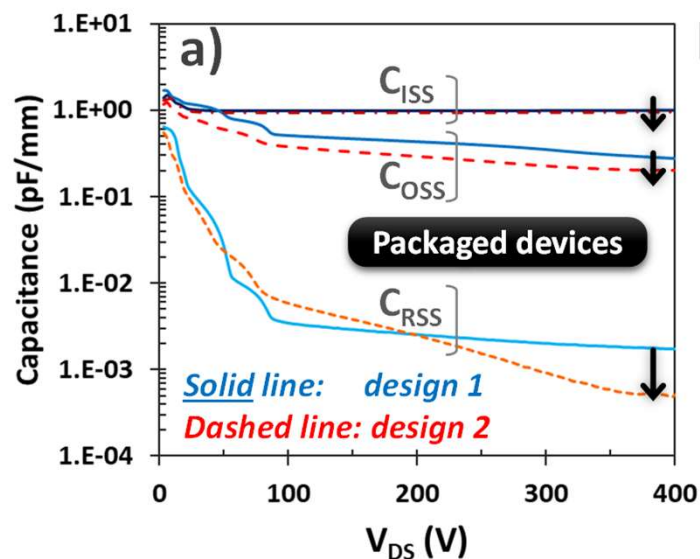


[C] reduction in epi layers



➤ Drain architecture optimization (field plate, passivation) is effective to reduce the current collapse (limitation of electron trapping in passivation); further benefits with epi optimization

C. Le Royer, ISPSD 2022



b) $V_{DS} = 200V$

	C_{ISS} (pF/mm)	C_{OSS} (pF/mm)	C_{RSS} (pF/mm)
MIS HEMT [1]	1	0.06	0.0060
This work:			
Design 1	0.99	0.43	0.0026
Design 2	0.87	0.27	0.0025

$V_{DS} = 400V$	C_{ISS} (pF)	C_{OSS} (pF)	C_{RSS} (pF)
pGaN [3]	380	72	0.3
pGaN [4]	242	65	1.5
This work:			
Design 1	476	131	0.831
Design 2	418	87	0.225

[1] P. Moens et al. ISPSD 2014

[3] IGT60R070D1 data sheet « 600V CoolGaN™ E-mode Power Transistor » (www.infineon.com)
 [4] GS66508T data sheet « Top-side 650VE-mode GaN transistor » (www.gansystems.com)

Learning :

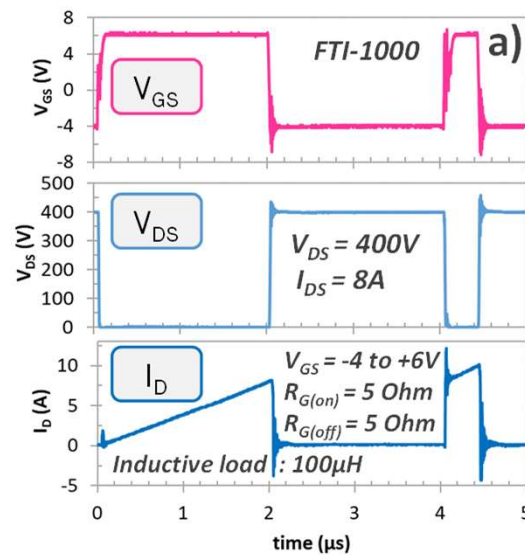
-The C_{ISS}/C_{RSS} ratio at 400V can thus be **maximized** for canceling parasitic switch ON of low side transistor in half bridge circuits.

This ratio is found to be much **higher** than for pGaN [3-4]: **1800** vs. **130-160**

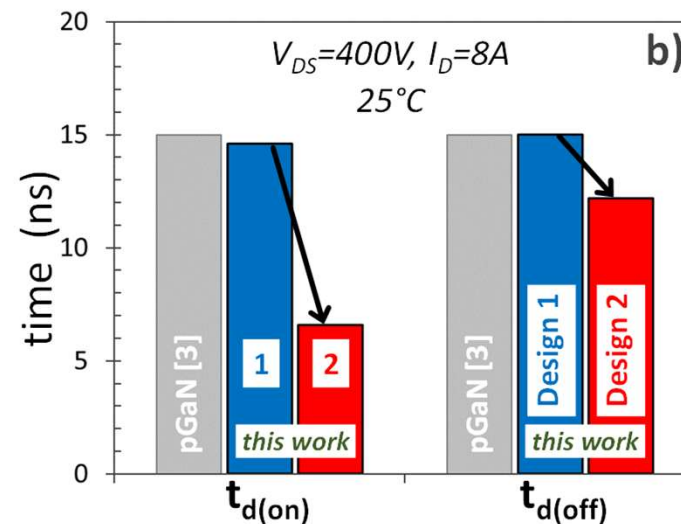
Switching tests performed for analysing losses in half bridge configuration

C. Le Royer, ISPSD 2022

Typical example (design 1, $I_D=8A$)



Switching times for 2 designs and pGaN comparison



Learning :

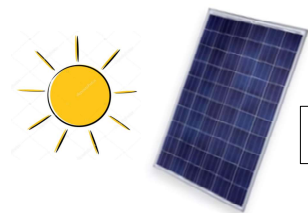
- Turn-on switching loss energy (E_{ON}) is dramatically improved ($>63\%$) with our recent integration scheme
- Switching times $t_{d(on)}$ and $t_{d(off)}$: fully recessed gate outperforms the commercial devices (pGaN)

Implementation of recessed-gate GaN-on-Si MOSc HEMTs in a 400W PV micro-inverter

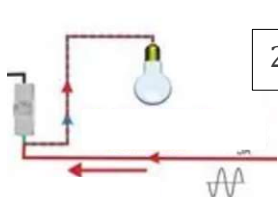
Live demonstration presented at the Leti Innovation Days (June 2022)

leti
cea tech

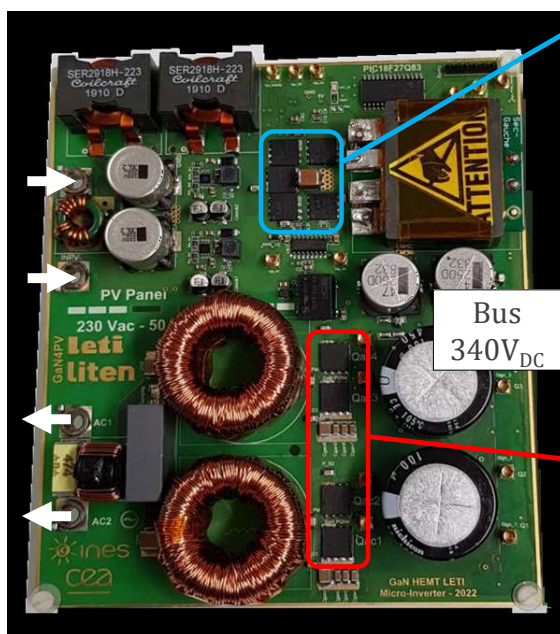
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20-50V_{DC}

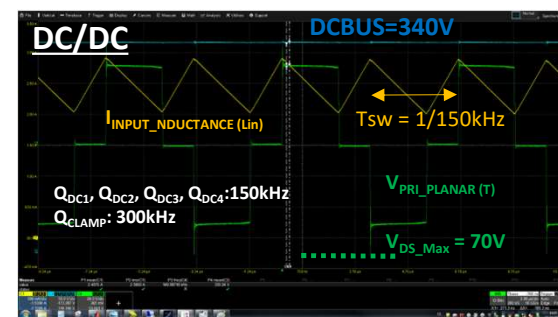
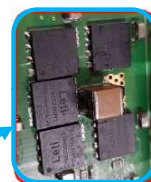


230V_{AC}-50Hz

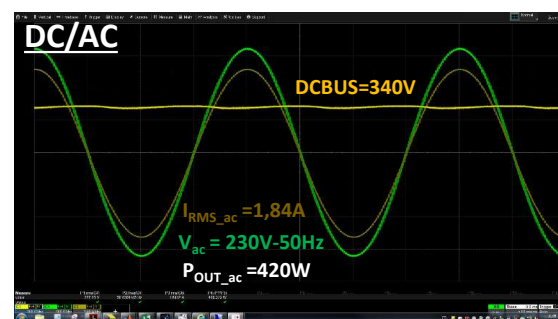
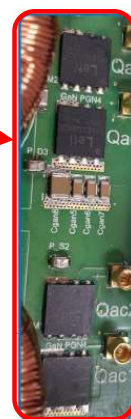


400W volume ~14x16x2.5cm³

DC/DC stage : 20-50V_{DC} → 340V_{DC}
5x GaN HEMTs (100V, 50A)



DC/AC stage : 340V_{DC} → 230V_{AC}-50Hz
4x GaN HEMTs (650V, 30A)



- **N-off GaN device based on recessed-gate MOS HEMT has been demonstrated, with several improvements with respect to pGaN-gate**
 - Lower gate leakage current
 - Higher gate voltage allowed for a typical 10 years lifetime
 - Better temperature-dependent behavior (Ron increase is lower)
 - Other parameters are well controlled (max leakage < 10^{-7} A/mm @ $V_{ds}=650$ V, limited Ron collapse)
 - Vth stability can be further improved

Many thanks to all contributors:

*C. Gillot, R. Gwoziecki, C. Le Royer,
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- R. Gwoziecki et al, "Recent advances in GaN power devices development at CEA-LETI", GaN Marathon (2022)
- W. Vandendaele et al, "Role of free holes in nBTI degradation », ISPSD 2022
- C. Le Royer et al, "Normally-OFF 650V GaN-on-Si MOSc-HEMT Transistor: Benefits of the Fully Recessed Gate Architecture", ISPSD 2022
- C. Leurquin et al, Novel High Voltage Bias Temperature Instabilities (HV-BTI) setup to monitor RON/VTH drift on GaN-on-Si E-mode MOSc-HEMTs under drain voltage", IRPS 2022
- M-A. Jaud, "Comprehensive TCAD Analysis of Threshold Voltage on GaN-on-Si MOS-Channel Fully Recessed Gate HEMTs", IEEE TED, 2022, doi: 10.1109/TED.2021.3136150
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- V. Maurya et al, "Understanding of the reverse transport characteristics of vertical GaN Schottky diode and its numerical simulation", IMAPS Tours, 2021
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- T. Lorin et al, "On the Understanding of Cathode Related Trapping Effects in GaN-on-Si Schottky Diodes", IEEE Journal of the Electron Devices Society, vol. 6, pp. 956-964, 2018, doi: 10.1109/JEDS.2018.2842100.
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- J. Biscarrat et al, "Performance enhancement of CMOS compatible 600V rated AlGaIn/GaN Schottky diodes on 200mm silicon wafers", ISPSD 2018
- T. Lorin et al., "Investigation of the role of back barrier depth and conductivity on the dynamic Ron and substrate ramping behavior of GaN Schottky diodes on silicon substrate", EPE'18 ECCE Europe
- L. Di Cioccio, "From epitaxy to converters topologies what issues for 200 mm GaN/Si?", IEDM 2015, doi: 10.1109/IEDM.2015.7409712.