

**SEMICON
EUROPA**

FORWARD
AS ONE

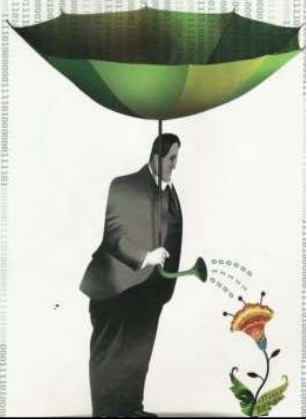
Will More-than-Moore Technologies with 3D Integration meet the Challenges of Edge AI Devices ?

Sylvie Joly CEA/Leti

March 8, 2021

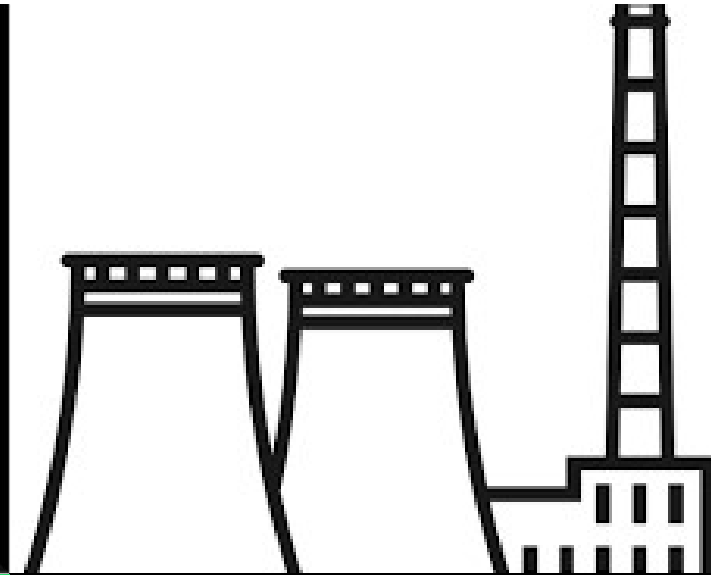


The data deluge



65

**billion of user messages
daily with whatsapp**



8.5

**billion of searches
processed by Google
each day**

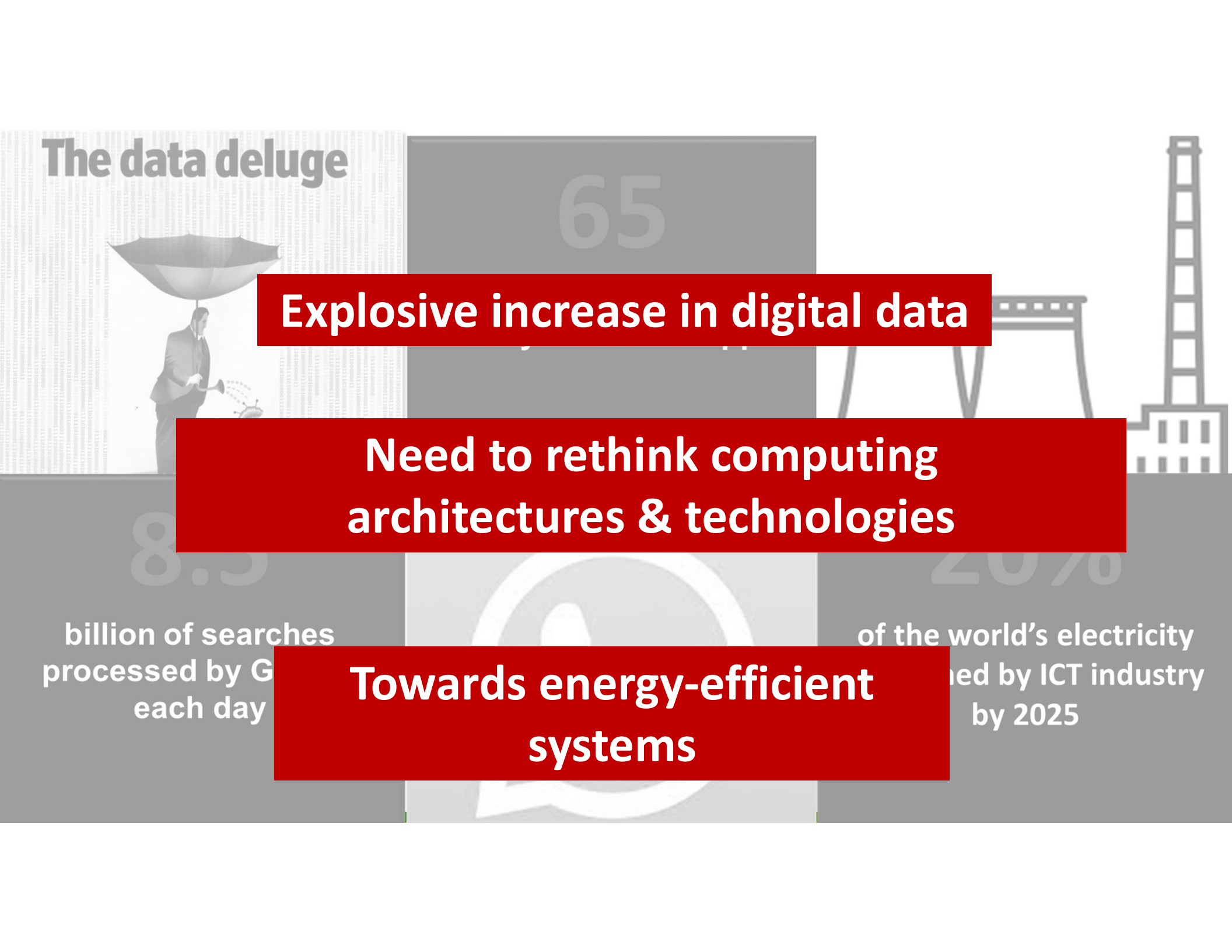


20%

**of the world's electricity
consumed by ICT industry
by 2025**

Source : <https://www.statistics.com>

The data deluge

The background of the slide is a grayscale illustration. On the left, a man in a suit holds a large umbrella, standing in front of a vertical stream of binary code (0s and 1s). In the center, there is a large, dark gray rectangular block with the number '65' in a light gray font. To the right, there are stylized outlines of industrial structures, including a tall chimney and a building. At the bottom, there are faint, large numbers '8.5' and '20%'.

Explosive increase in digital data

Need to rethink computing architectures & technologies

Towards energy-efficient systems

8.5 billion of searches processed by Google each day

20% of the world's electricity consumed by ICT industry by 2025

☐ Evolution in computing

Challenges, new architectures, key enabling technologies

☐ Four examples of architectures with More than Moore technologies

Intact : heterogeneity, modularity and reuse of 3D-Design

Photonic integration

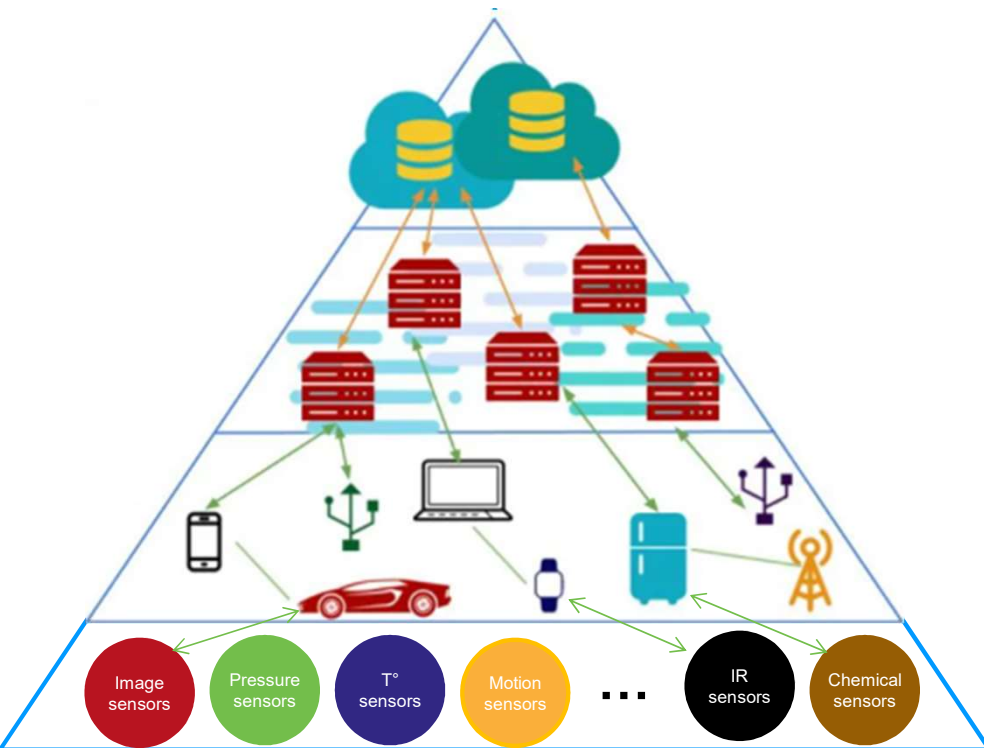
Sensors imager & Display

Lidar

☐ Conclusion

EVOLUTION OF COMPUTING

The 3 main levels ...



HPC & Cloud

Thousands of data centers / supercomputers

Distributed Cloud

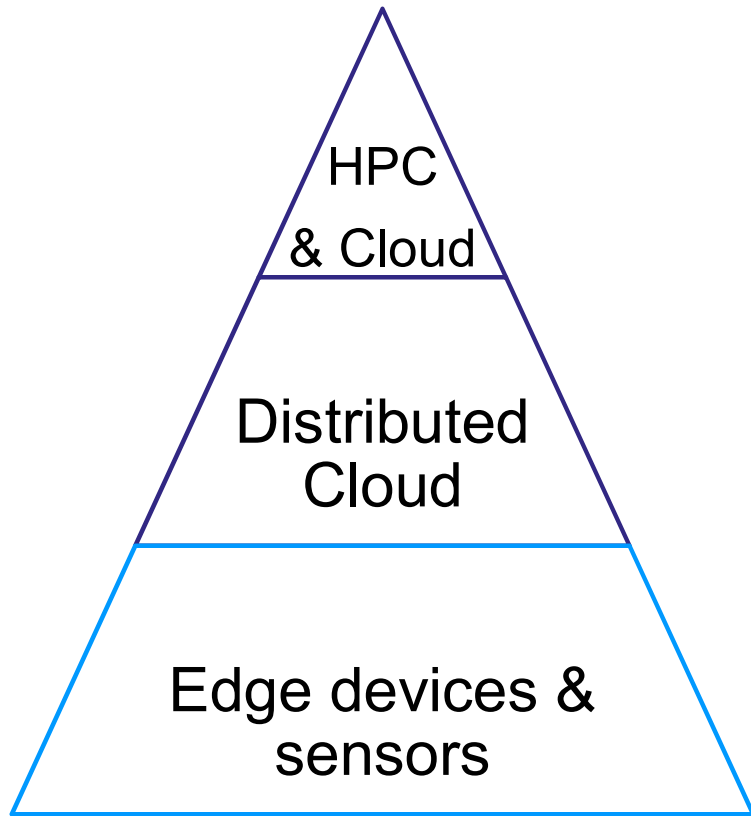
Millions of nodes

Rack-scale servers, hyper-converged infra-structures

Edge devices & sensors

Billions of devices, mobiles, glasses, displays, cameras, ...

EVOLUTION OF COMPUTING : WHAT ARE THE MAIN CHALLENGES ?

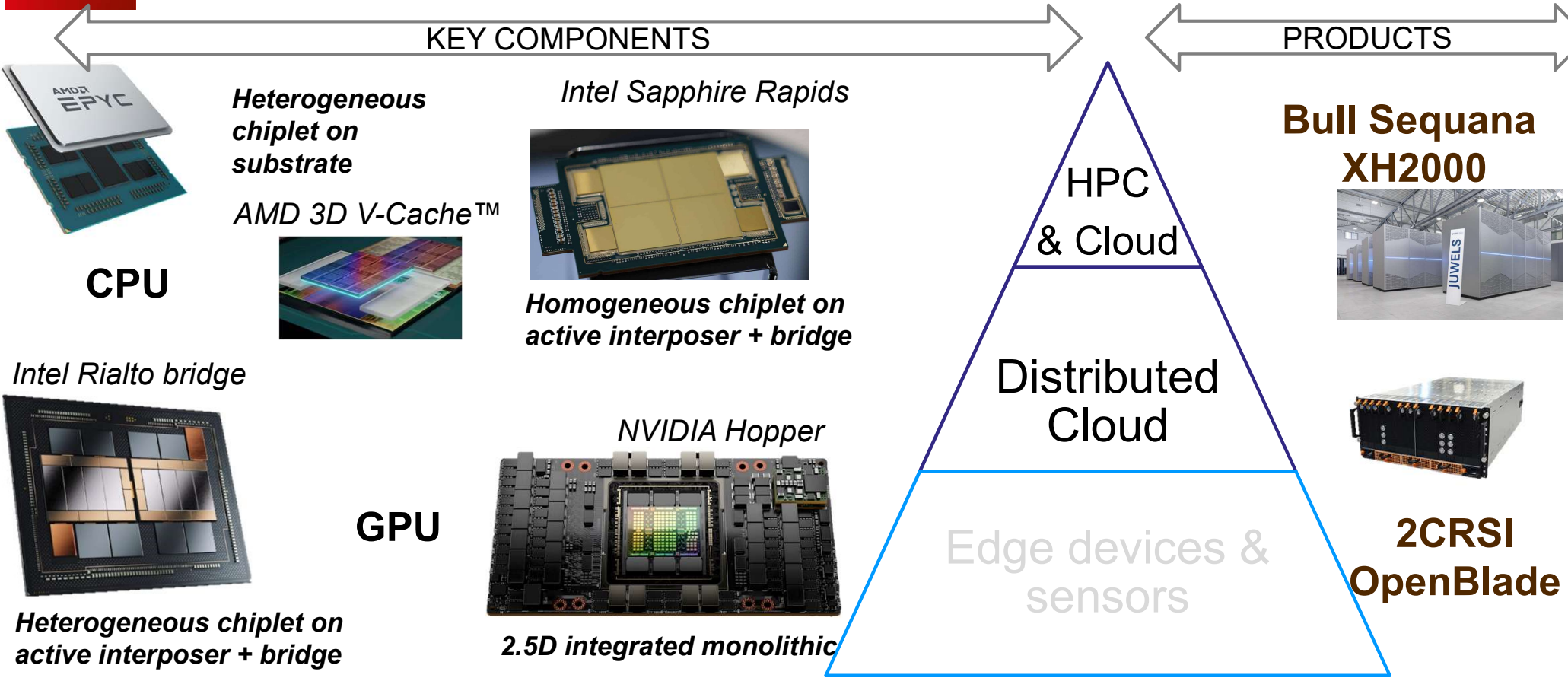


1. Sovereignty
2. Energy efficiency / performance
3. Architecture: memory centric and photonic links

1. Decrease of cost
2. High flexibility
3. Low latency

1. Compute close to the data
2. Real-time
3. Frugality, flexibility, modularity
4. Low cost

EVOLUTION OF COMPUTING
EXAMPLES : PRODUCTS AND COMPONENTS (1/2)



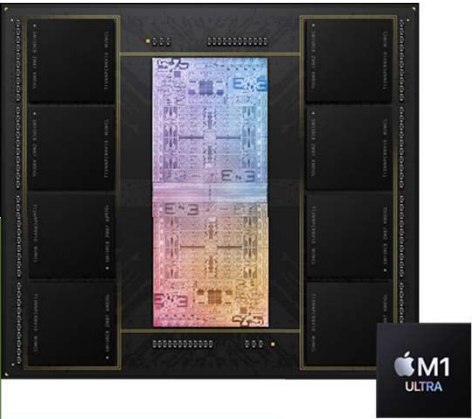
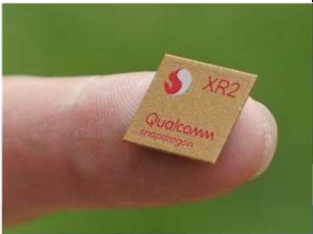
More than Moore technologies are highly implemented
to allow an ever scaling performance development



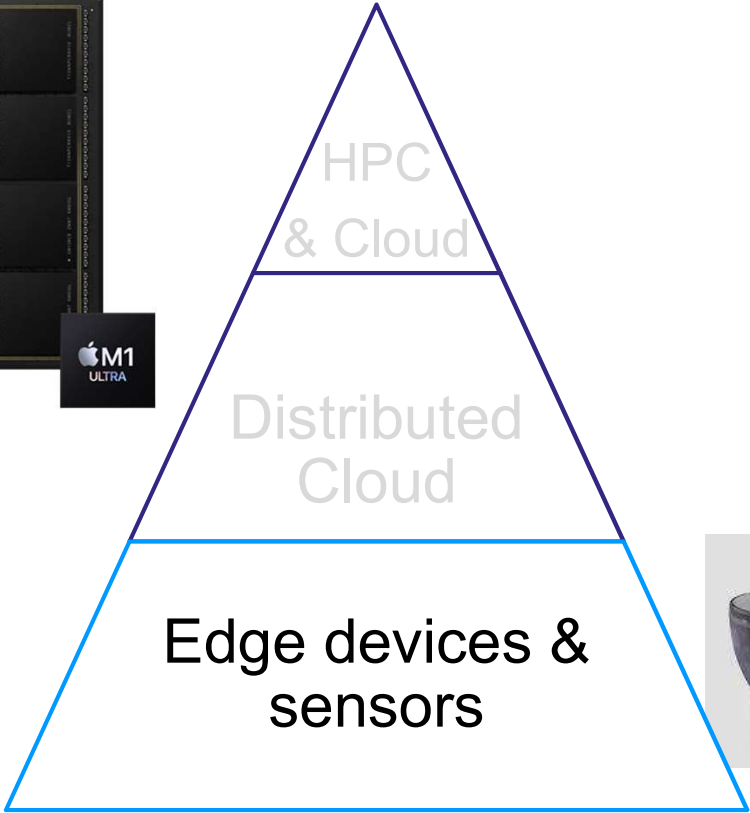
EVOLUTION OF COMPUTING
EXAMPLES : PRODUCTS AND COMPONENTS (2/2)



M1 Ultra from two M1 Max dies



Iphone



Hololens 2



Snapdragon XR3

Platform

Key components selection

- 5G, 60GHz enabled stand alone
- 2K Dual panel LCD
- 7 Camera support

Product/HW design files

schematics, BOM, layout files, thermal design guidelines

XR SW features

- Head tracking
- 3DR
- Eye tracking
- Hand tracking
- Adreno foveation
- 6DoF controller
- Boundless XR

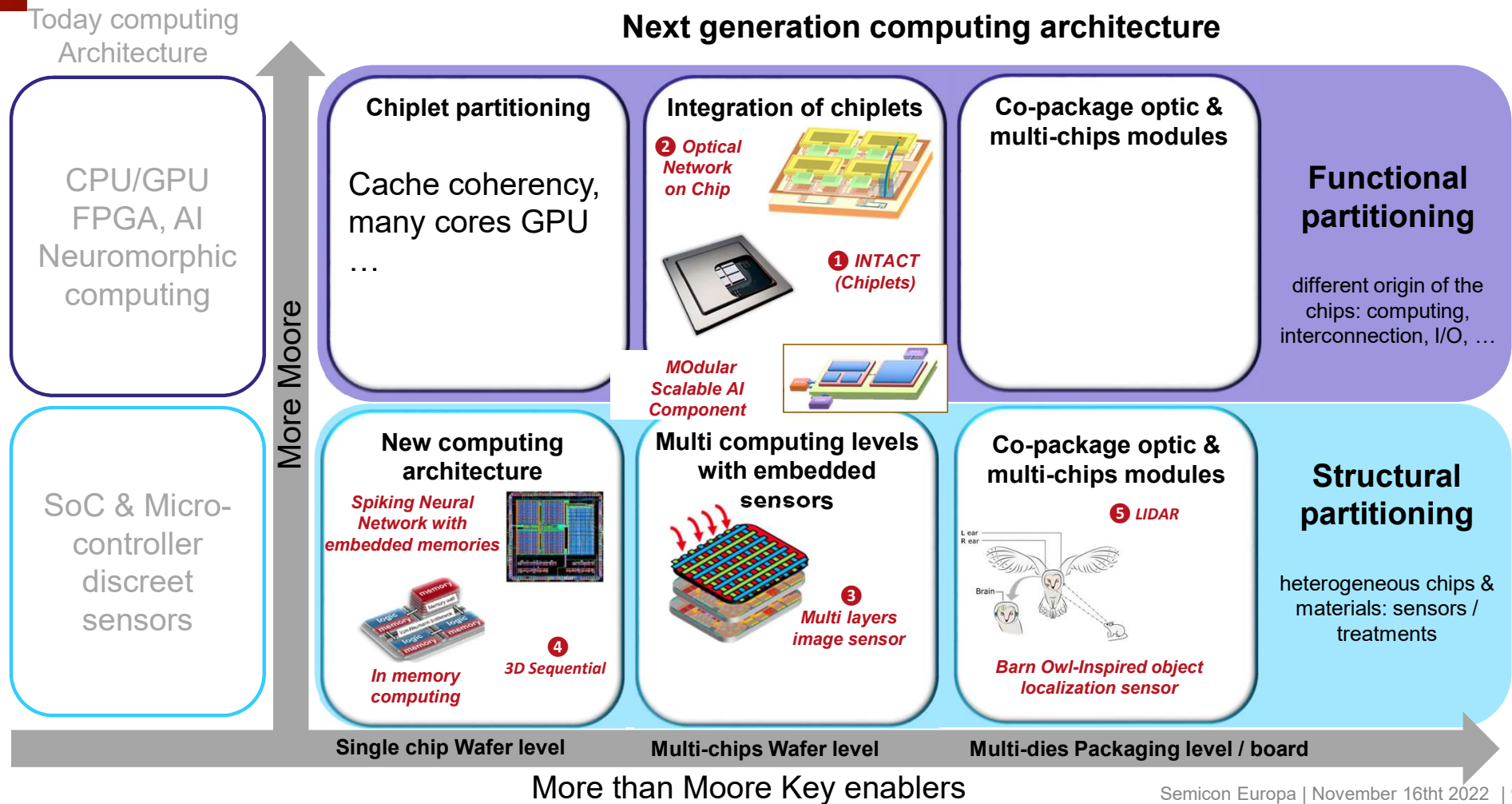
Partners

- Goertek
- NDI
- tobii

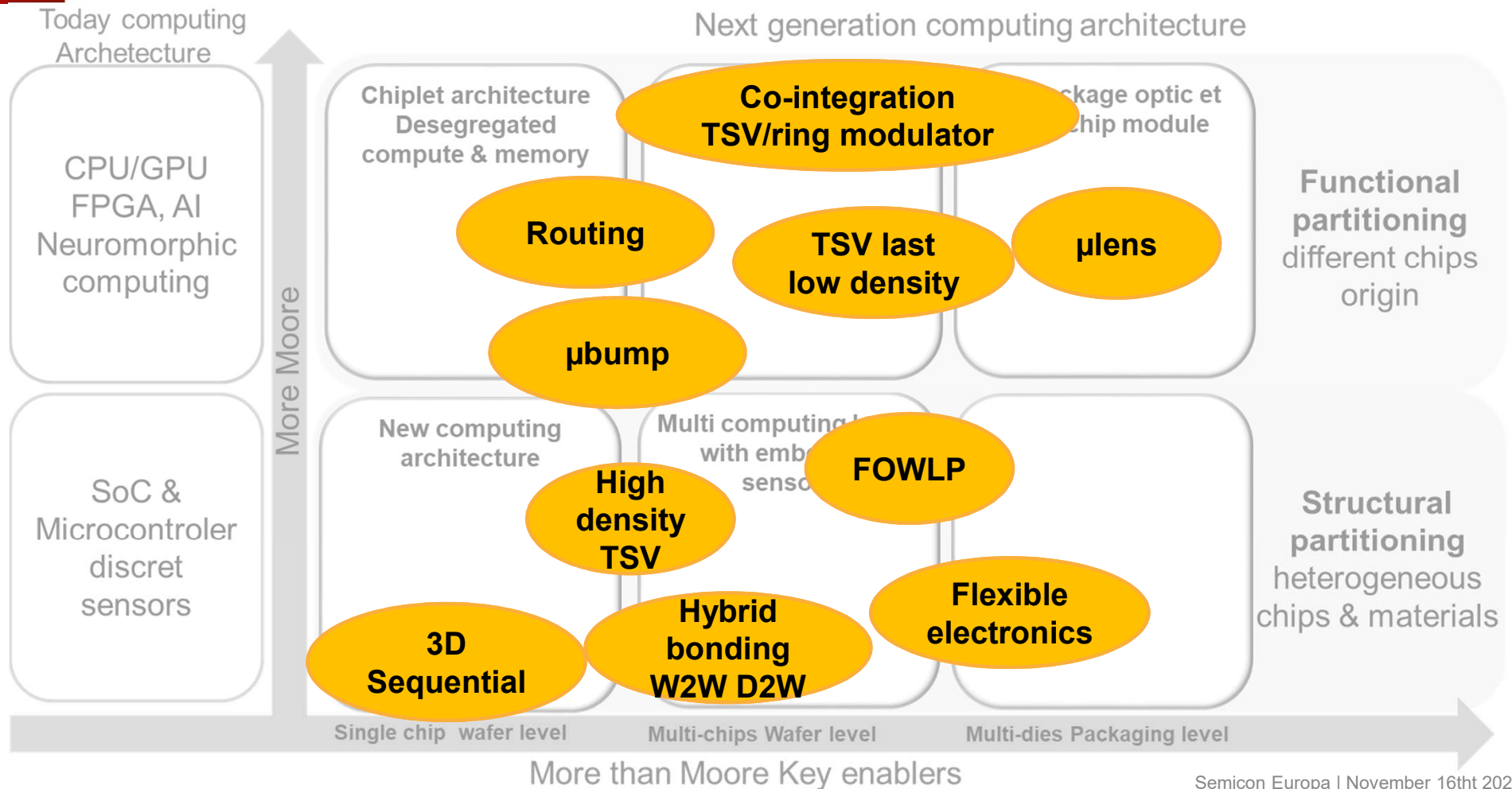
Snapdragon XR2 5G Reference design

More than Moore technology is popping-up for edge device processors

THE SOLUTION : CO-OPTIMIZATION ARCHITECTURE / MORE MOORE / MORE THAN MOORE

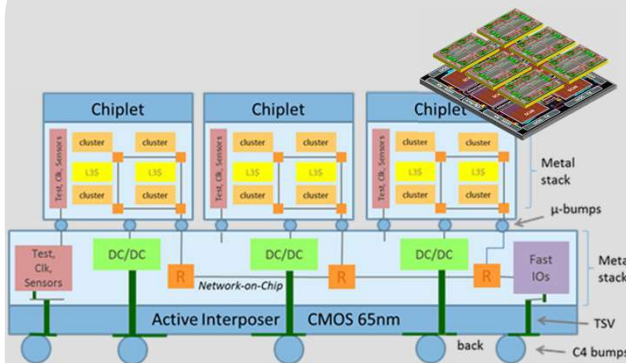


CO-OPTIMIZATION: KEY ENABLING TECHNOLOGIES



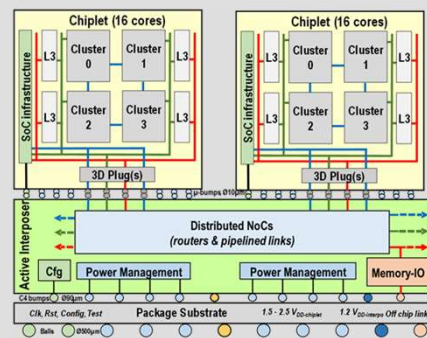
EXAMPLE 1: INTACT - HETEROGENEITY, MODULARITY AND REUSE OF 3D-DESIGN

System Architecture



<https://www.design-reuse.com/sip/?q=CEA>

Design

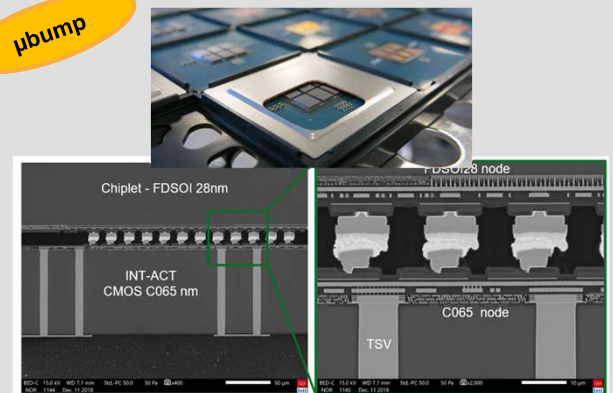


Proven with our 96-cores compute demonstrator
6 chiplets stacked on an active interposer

TSV
Middle

μbump

Technologies



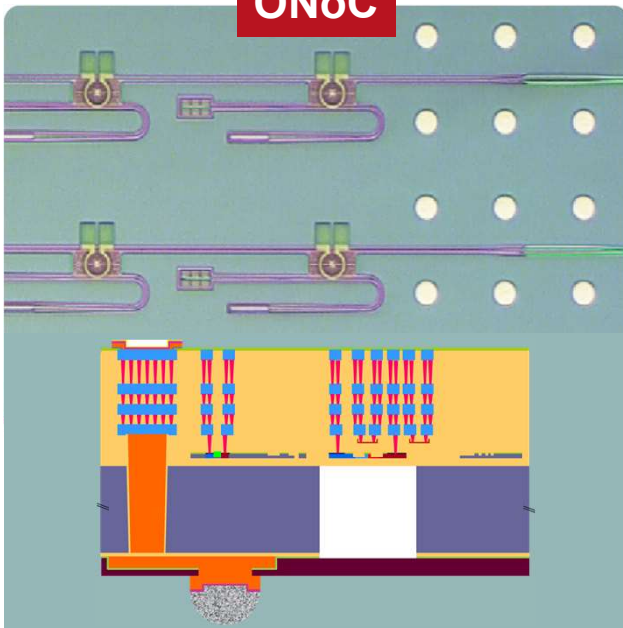
Copper pillar
Ø 10 μm
Pitch 20 μm

TSV middle
Ø 10 μm
Height 100 μm

**Making 3D design heterogeneity, modularity and reuse real
With further cost, TTM and yield improvements**

EXAMPLE 2: INTEGRATION SILICON PHOTONICS & ELECTRONICS FOR MORE EFFICIENT I/O

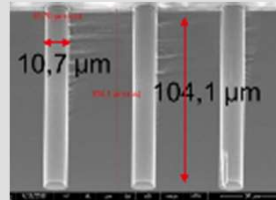
ONoC



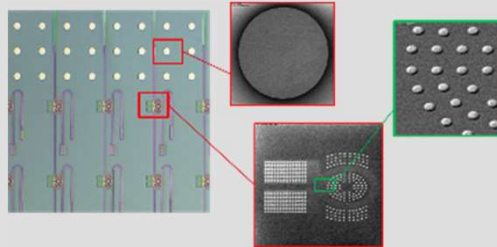
TSV
Middle

μ bump

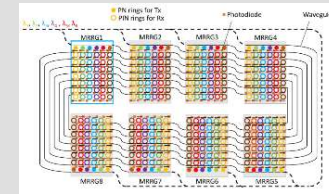
- Photonics TSV mid and last



- Co-integrated bricks

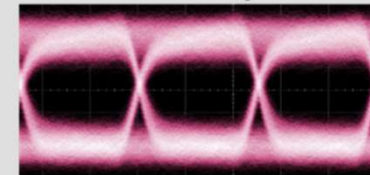


- WDM link for ONoC architecture



- E/O micro rings & thermal tuning

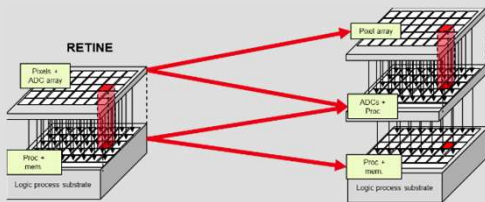
Wob.+Thermal tuning activated



**Active silicon photonic interposer
For shortened electrical links**

EXAMPLE 3: SMARTER IMAGER

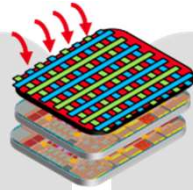
Architecture smart imager



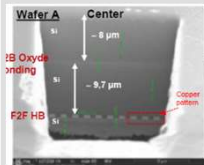
AI features in Smart Imager

- Low energy
- Low latency
- Safety & Privacy

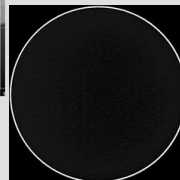
Distributed computing clusters support both standard vision and AI applications



2nd step & Interface



1st step & interface



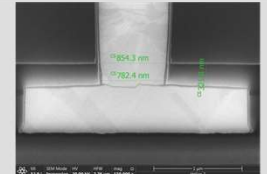
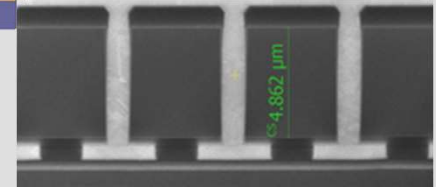
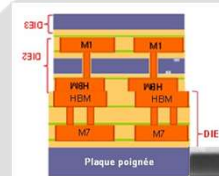
*Scanning Acoustic Microscopy
After hybrid bonding and annealing*

Hybrid
bonding
W2W

Misalignment :
Max. (3σ) $1\ \mu\text{m}$
Avg $200\ \text{nm}$

Misalignment :
Max. (3σ) $350\ \text{nm}$
Avg $100\ \text{nm}$

High
density
TSV

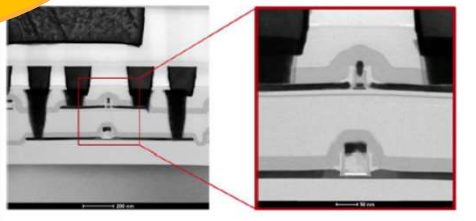


TSV : $1\ \mu\text{m} \times 5\ \mu\text{m}$
Hybrid bonding : $4\ \mu\text{m}$ pitch

3D stacked imager for AI applications

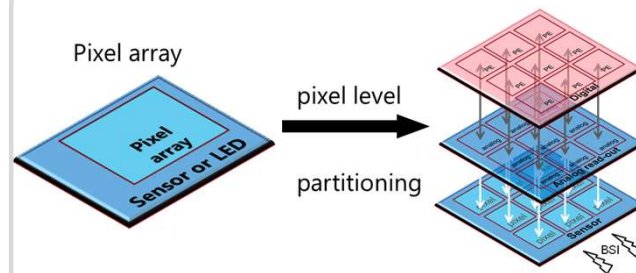
EXAMPLE 4: 3D SEQUENTIAL FOR IMAGER OR DISPLAY

3D Seq

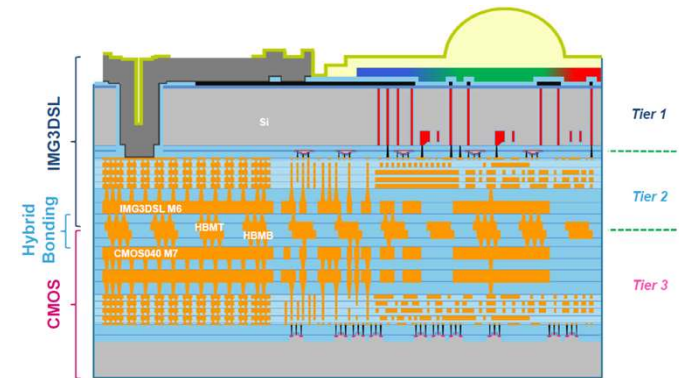


- Sequential / vertical process CMOS
- Low temperature top level
- Nano-metric alignment between gate level
- Applicable to heterogeneous and CMOS 3D

Architecture smart imager/Display

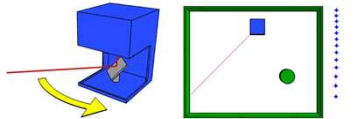


Increased Photodiode area
(44% for 1.4 μ m pitch)
Smart 3D pixel / In pixel processing
(Adaptation, calibration, pre-processing...)

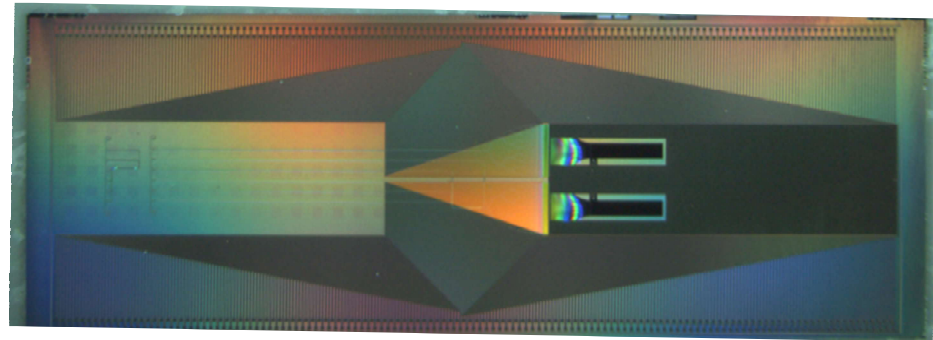
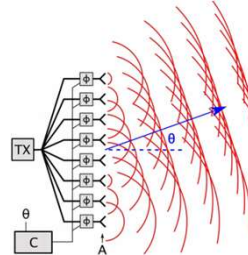


Combining sequential (monolithic) with parallel (Hybrid-bonding) integration offer a great opportunity for pixel partitioning with pitch in the 1 μ m range and distributive computing for high efficiency

EXAMPLE 5: LIDAR MINIATURIZATION FOR AUTONOMOUS VEHICLE DRIVING

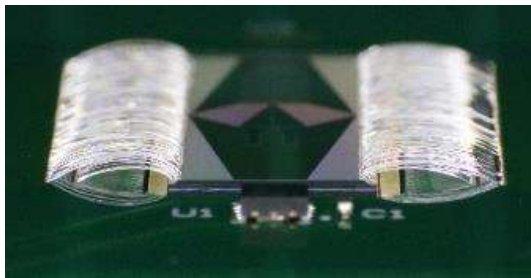


Mechanical steering is huge,
slow and expensive



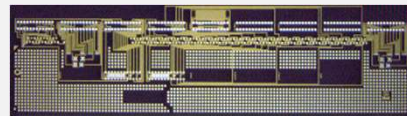
Optical Phase Array (Si wafer level technology)

It works well ! But ...

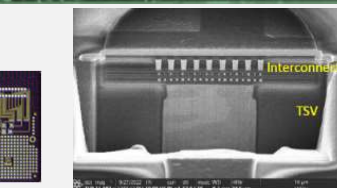
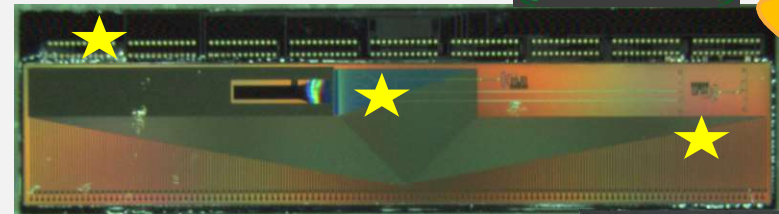


Too many wires for a 256 channels OPA
>1000 channels required for ADAS

3D packaging integration of Photonic IC on Interposer



Interposer
OPA, CMOS drivers & Laser



OPA Back side surface for higher
connections density
10x100µm TSVs



High density
Collective Flip chip
20µ Φ Copper pillars

TSV
last
µbump
Routing

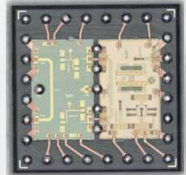
3D INTEGRATION: FROM TECHNOLOGIES TO SYSTEM AT CEA-LETI

> Wide range of fields



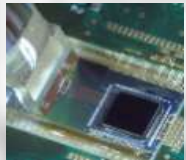
Advanced Digital Circuit

Chiplet approach, In memory computing, ANOC, ONOC, AI, etc.



RF Integrated circuits

FOWLP, Antenna on package, ... etc.



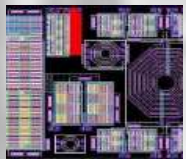
Si Photonics IC with TSV integration

Drivers, Analog Read Out, Data Processing, Lidar



3D integration from 3DSeq to hybrid bonding

Embedded AI for Imager, Smart display, ...



Layout and Masks

“3rd Innovative Public
Research Organization
Worldwide” 2012-2020

Derwent™
A Clarivate Analytics company



Since **1967**



2,000 people

Patents:



- > 3,000 in portfolio
- 40% under license agreement

Startups:



- 68 created for 20 years (75% in activity)
- 3500 jobs created

Cleanrooms:



- 500 state-of-the-art equipment in 200 & 300 m²
- 10 000 square meters cleanroom

Budget:



- 315 M€
- 85% from R&D contracts

SEMICON® EUROPA

FORWARD AS ONE



THANK YOU FOR YOUR ATTENTION



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Silicon Components Division

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