



Nicolas Daval

Sustainable SiC

The Advantages of Engineered Substrates

Semicon Europa | 2022 November 17th



AGENDA

Sustainable SiC : The Advantages of Engineered Substrates

Engineered substrates

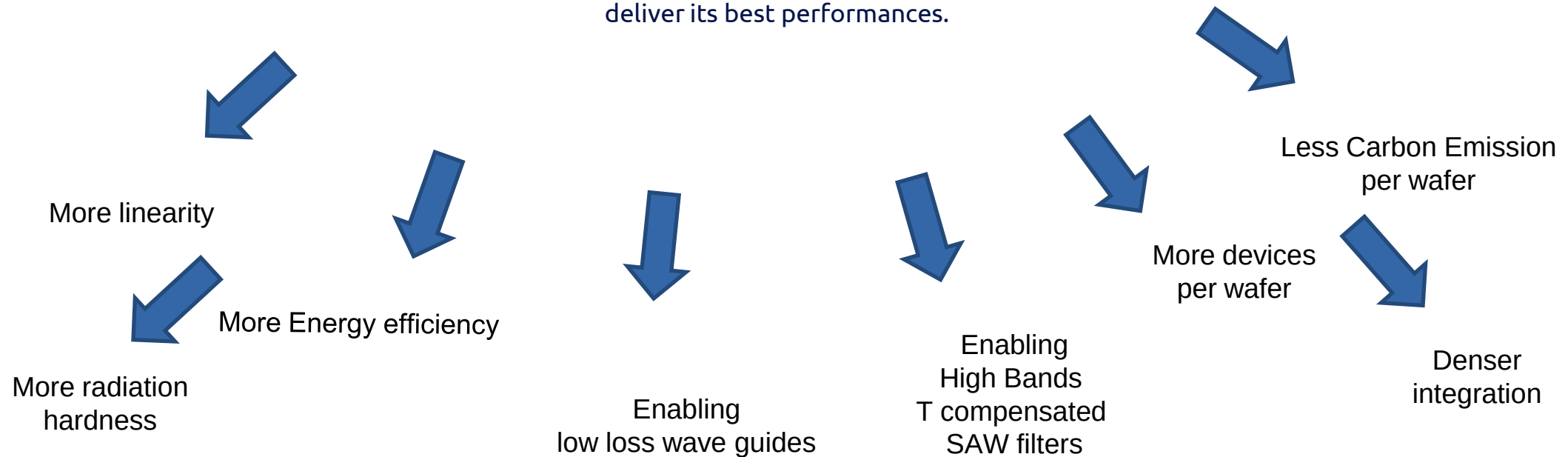
SmartSiC™

Conclusions



Engineered Substrates

Think the starting material of your device,
NOT as a disk of your needed semiconductor
BUT as an ideal stack of layers that will enable your device to
deliver its best performances.

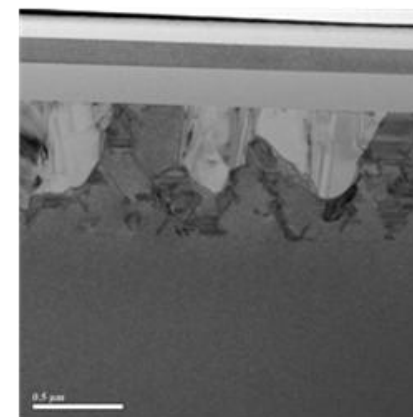
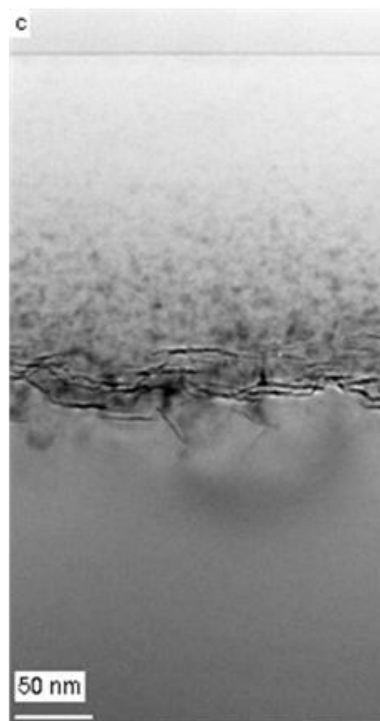
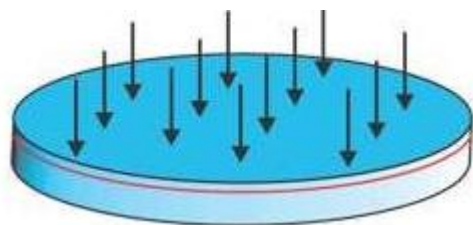


Single crystal layer transfer



Smart Cut™

H⁺ Implantation



that we can manipulate and
put on top any type of
substrate

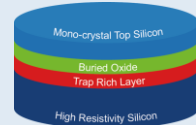
delached a thin membrane

Soitec Product Portfolio

Mobile communications

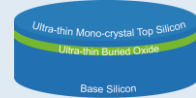
RF-SOI

For highly efficient mobile communication



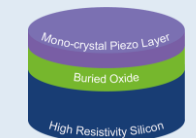
FD-SOI

Integrated technology



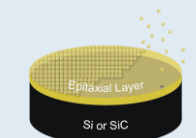
POI

High performance 5G filters



GaN

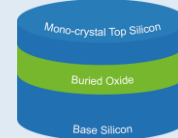
High performance power amplifier



Automotive & industrial

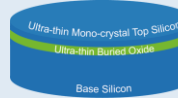
Power-SOI

Power management IC, In-vehicle networking & gate driver



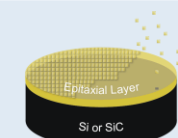
FD-SOI

MCUs, ADAS-Radar, ADAS-Vision



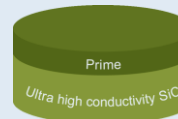
GaN

DC-DC 48V converters



Smart SiC

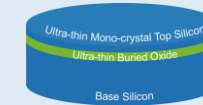
Automotive electrification



Smart devices

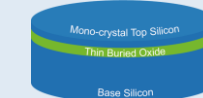
FD-SOI

Crossover MCU, connected MCUs, scalable FPGAs



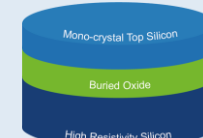
Imager-SOI

For improved imager performance in NIR



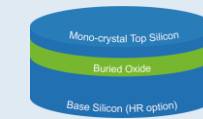
Photonics-SOI

Optical transceivers and bio-sensing



PD-SOI

High performance computing



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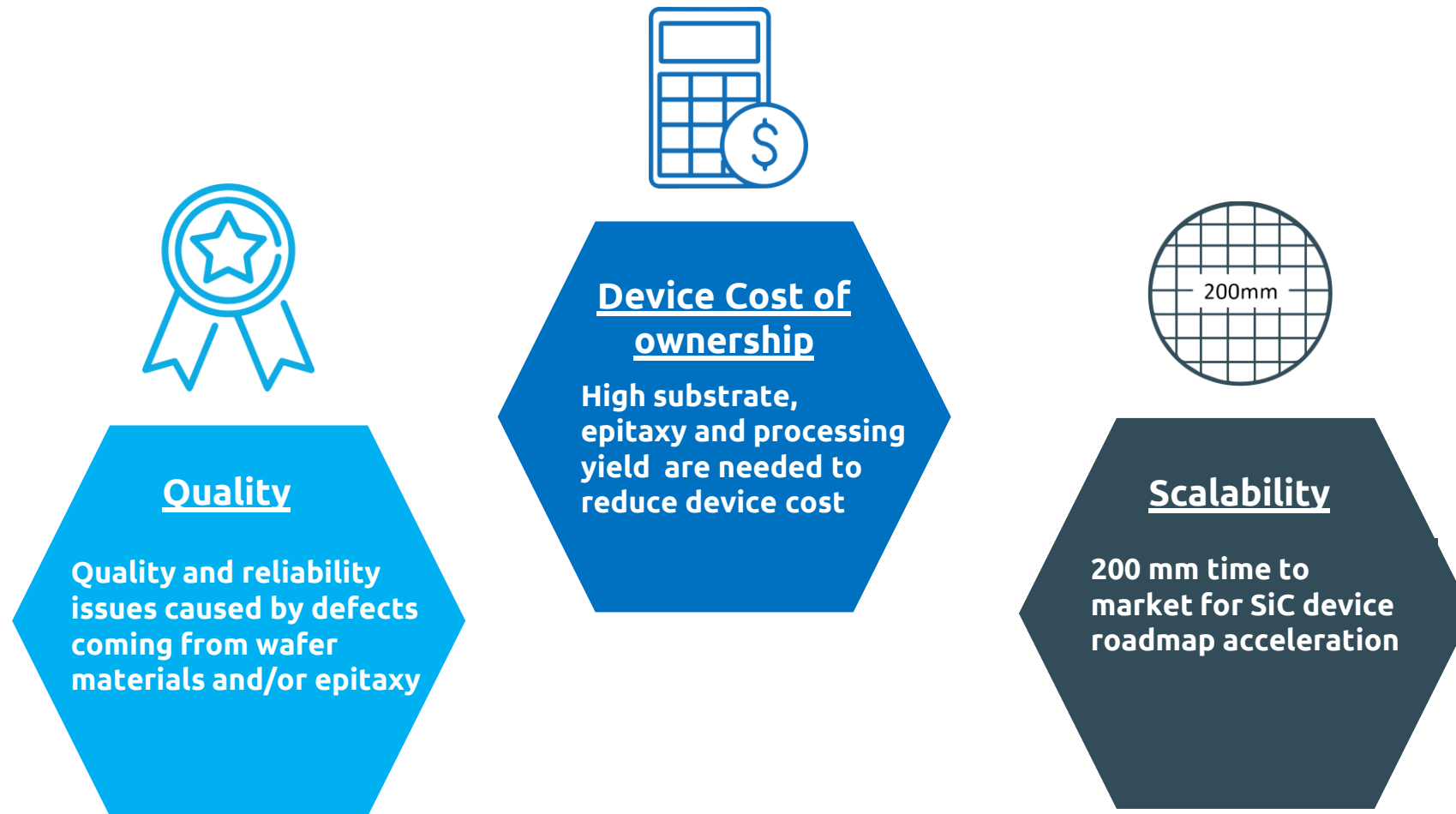
Sustainable SiC : The Advantages of Engineered Substrates

Engineered substrates

SmartSiC™

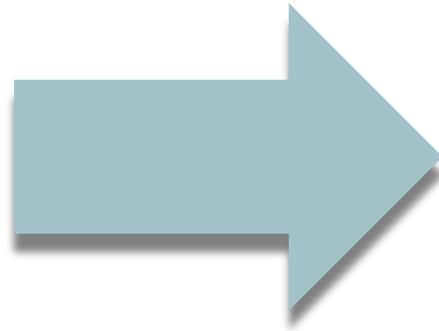
Conclusions





The key challenges for greater SiC market adoption

From 4H-SiC Bulk

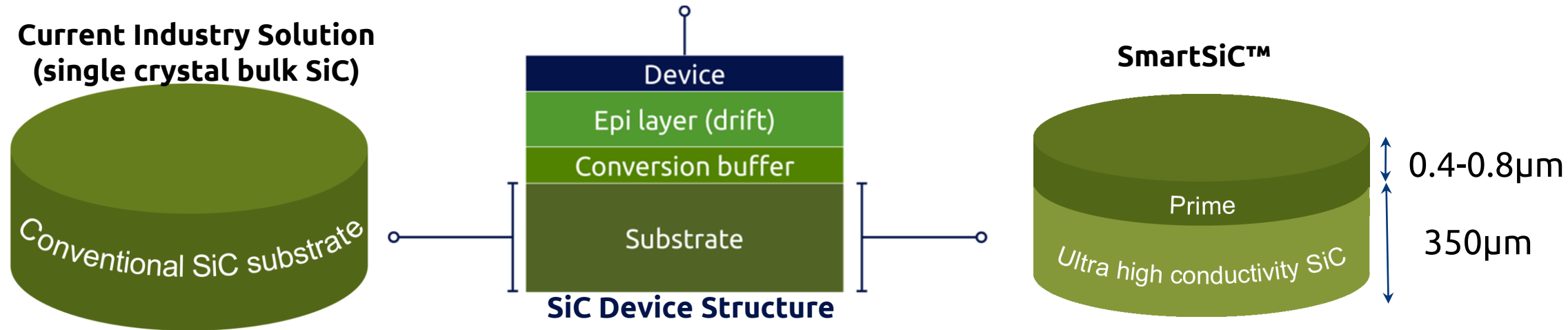


To SmartSiC™



6" and 200mm

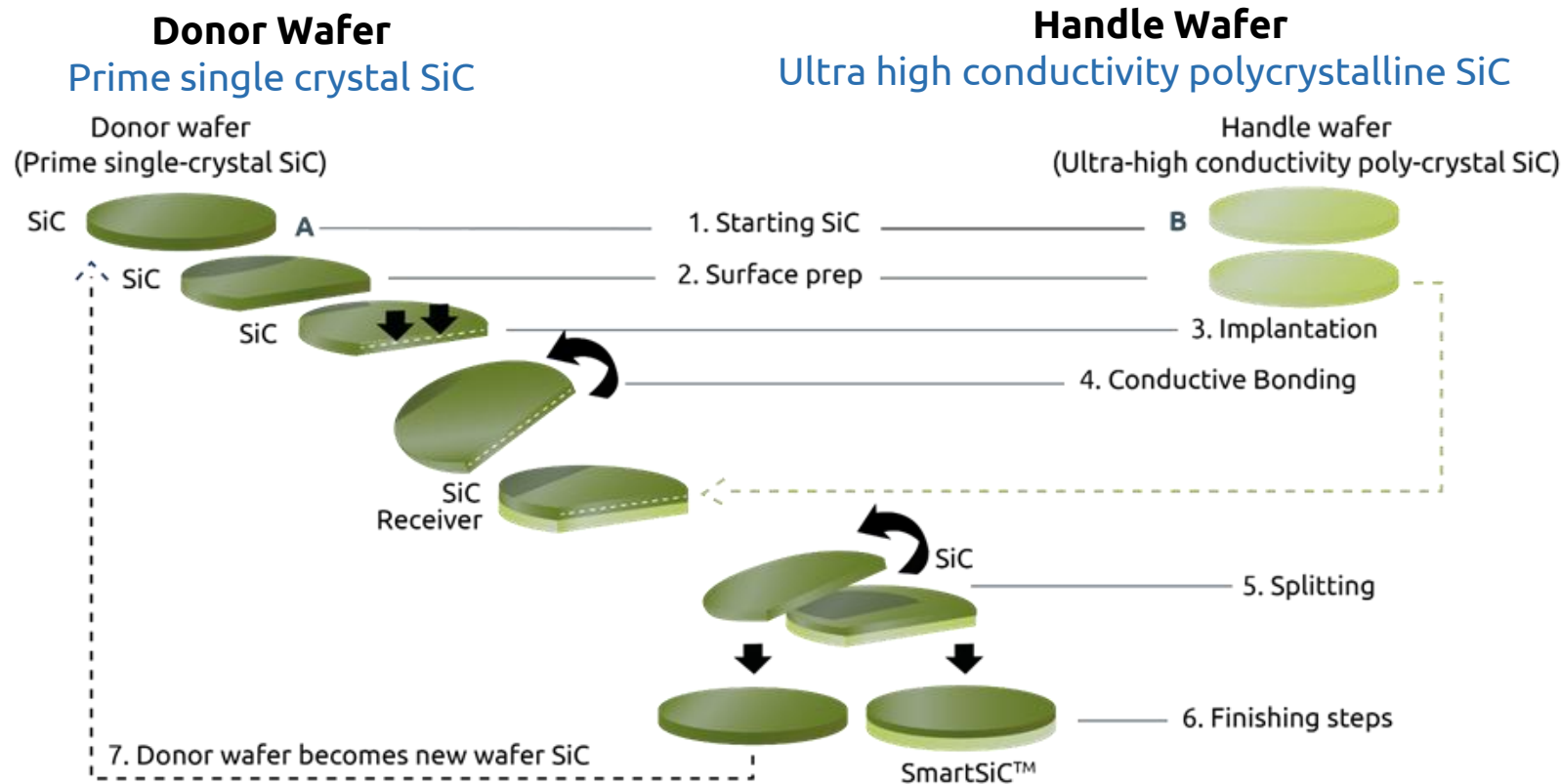
SmartSiC™: optimum design for a unique value proposition



- **Smaller size / Higher current** rating devices
- **Higher** manufacturing **yield**
- **Improved local flatness**
- More **ultra-prime substrates** available
- **Pure-play** substrate **supplier**
- **Fastest path to 200mm** transition

Lower \$ / device

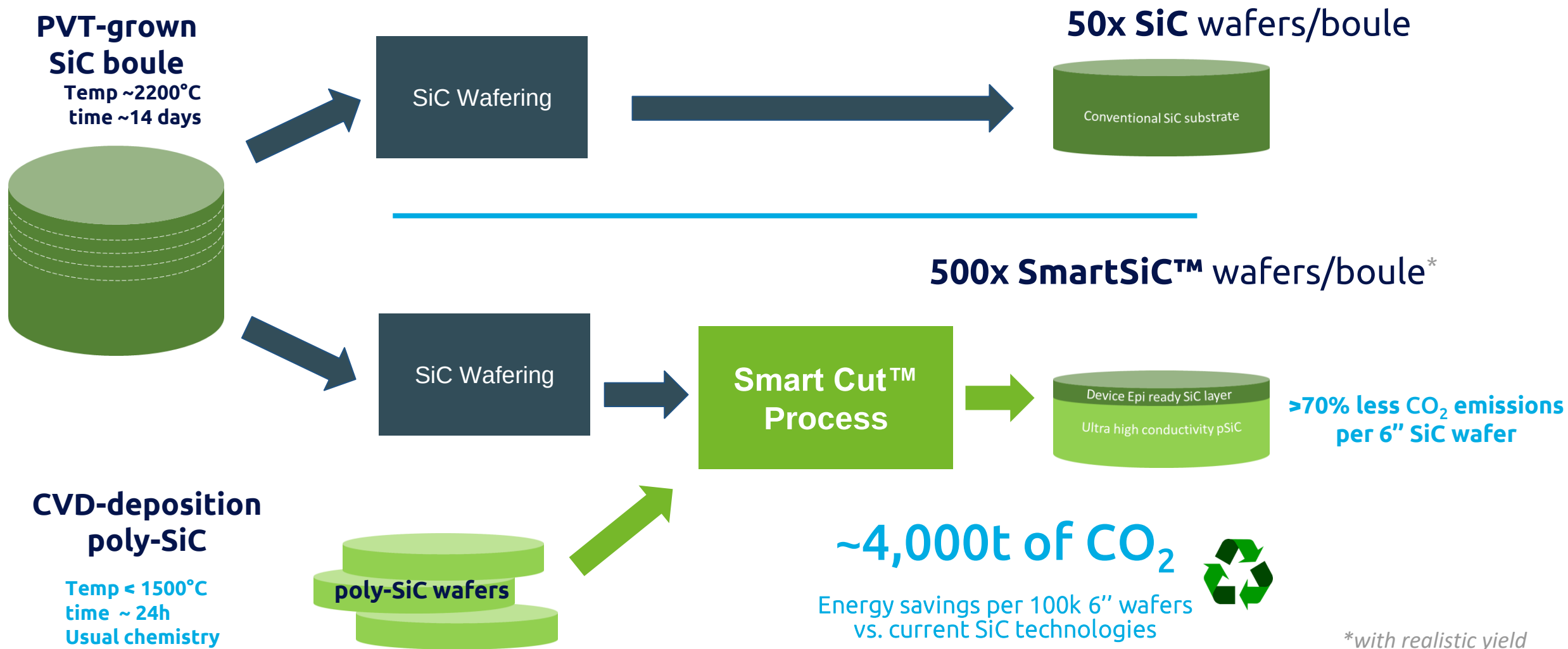
Smart Cut™ process adapted to Silicon Carbide



MAJOR STAGES OF SMART CUT™ for SiC

- Donor wafer: Prime quality SiC
- Handle wafer: Ultra High Conductivity polySiC
- Conductive bonding interface
- Finishing including polishing & high temperature anneal to be epi ready
- Donor wafer re-use (>10x) for new process cycle

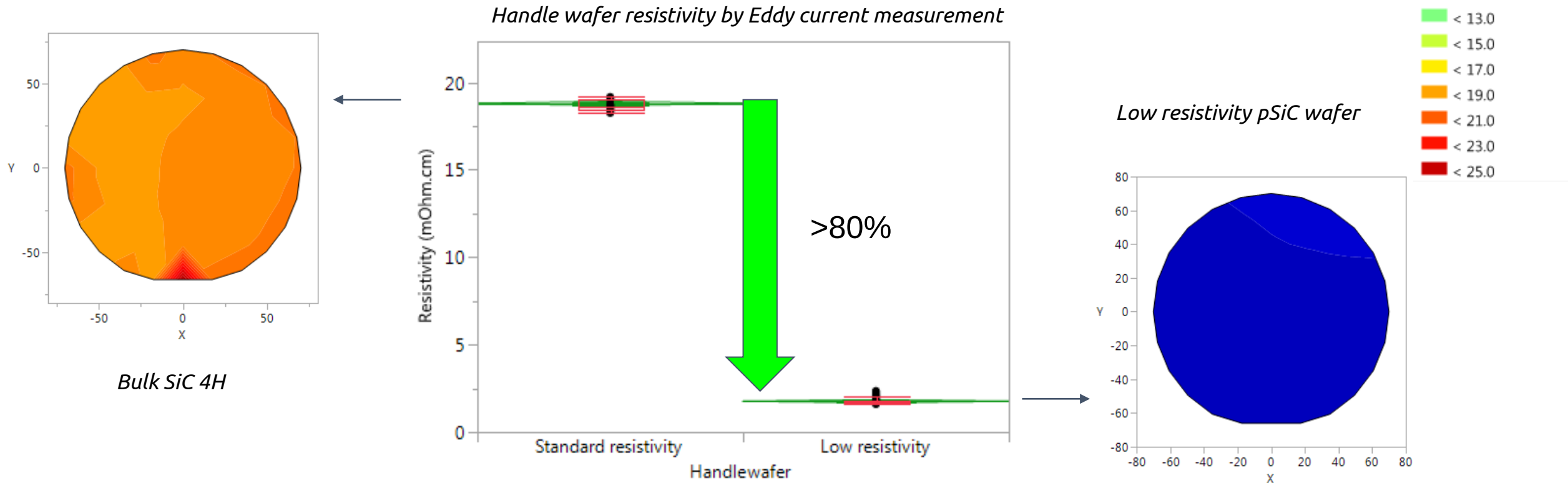
Making the most of high value monocrystalline crystal



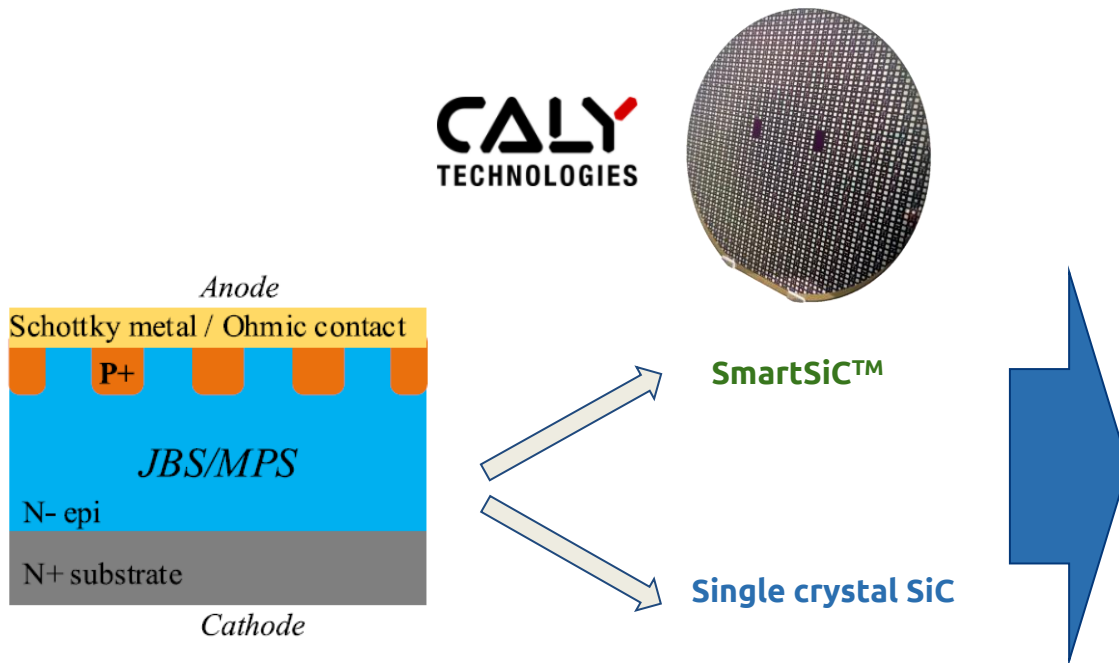
**with realistic yield*

Handle wafer: ultra high conductivity performance

Reduced conduction losses

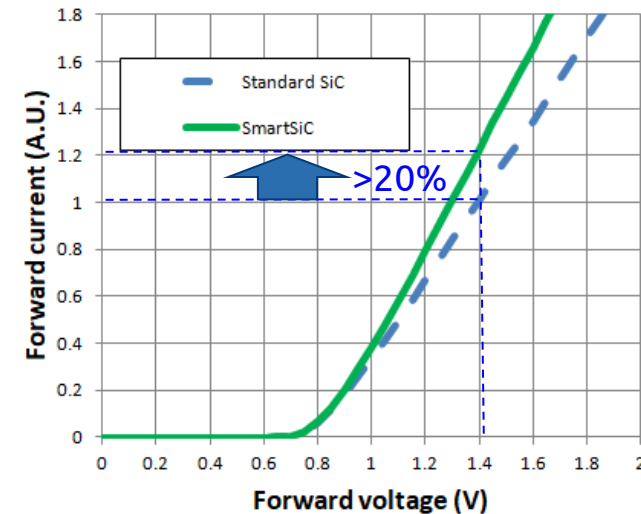


SmartSiC™: device validation results (1200V JBS diode)



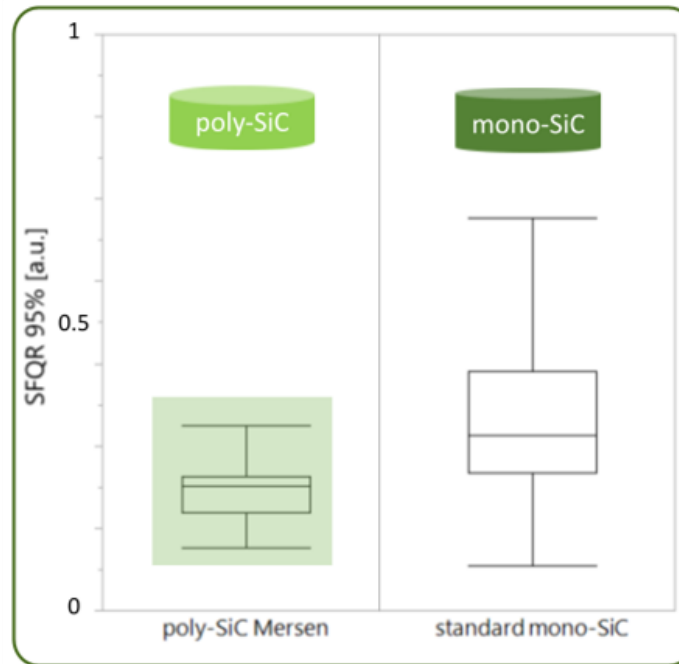
- Wafer level measurement
- Unthinned 1200V JBS diode

Forward characteristics of JBS diode
Standard SiC vs SmartSiC™



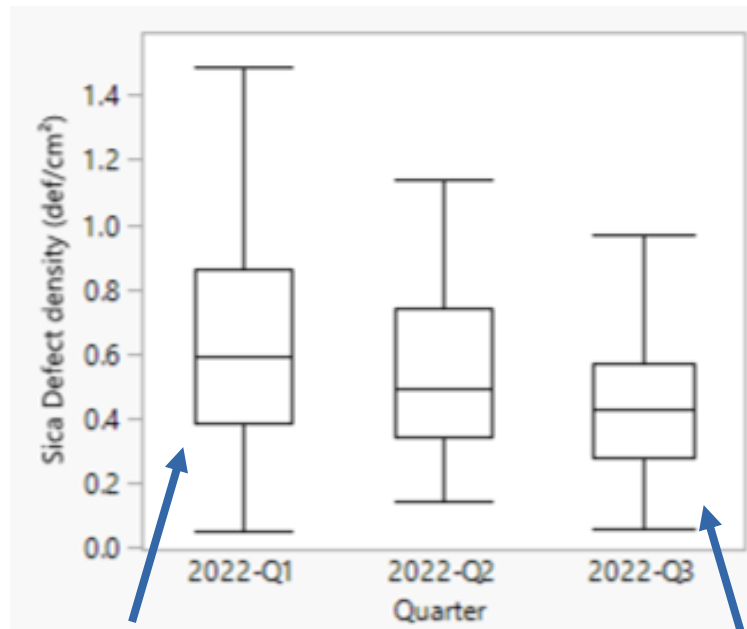
SmartSiC™ : forward current improvement (>20%) or die shrink

pSiC better wafer geometry control



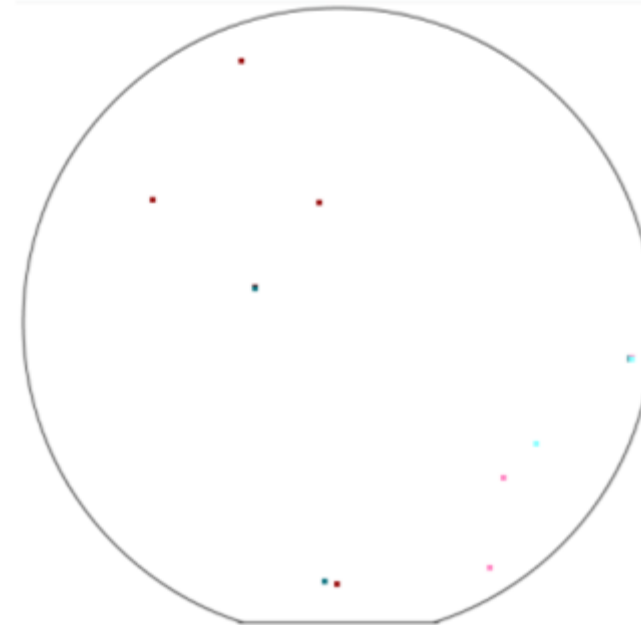
Smart SiC™ continuous improvement

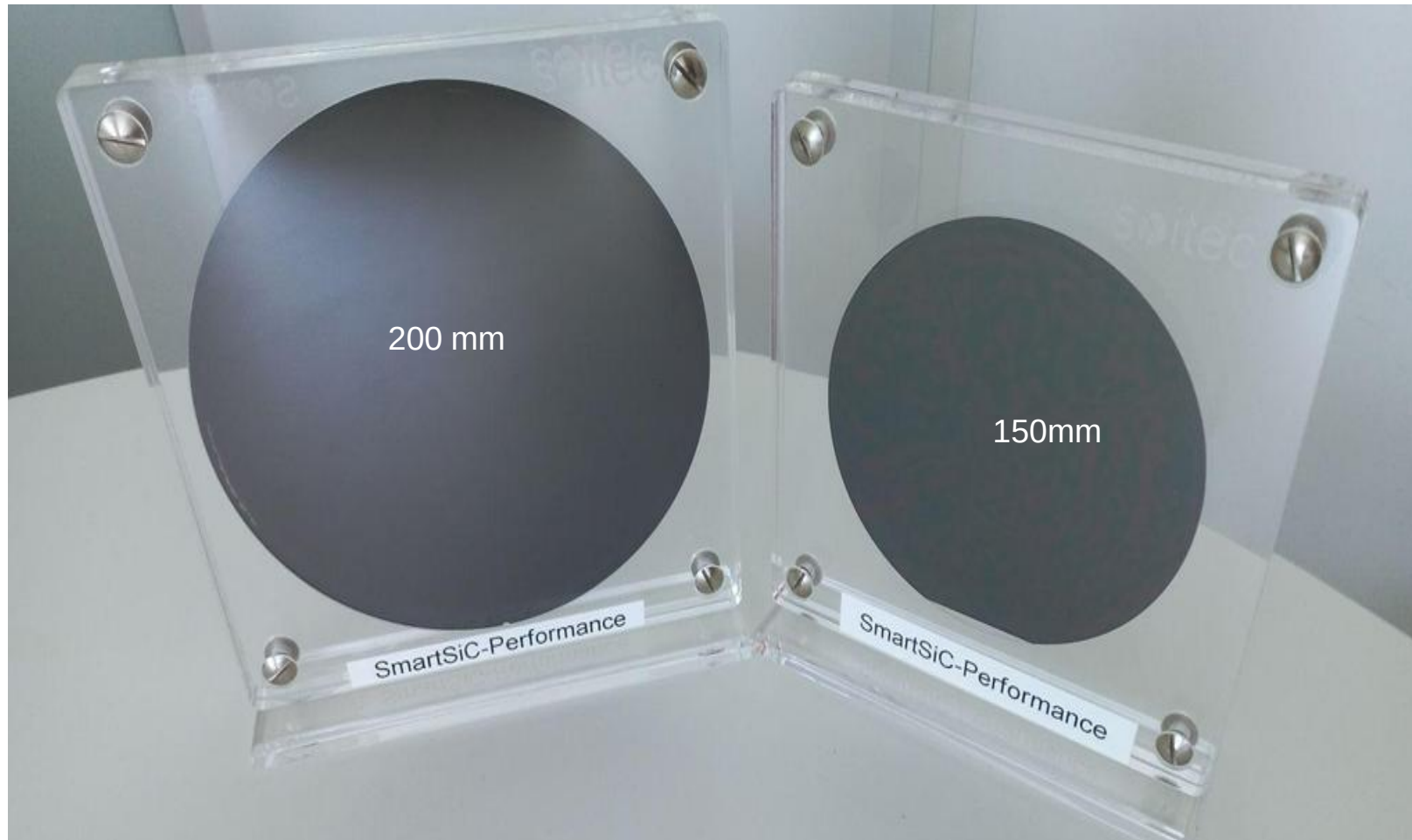
Sica surface defect density



ICSCRM 2022
Davos, Switzerland

Gen1.2 - Spring'22
Surface defect density : 0.1 / cm²





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Engineered substrates

SmartSiC™

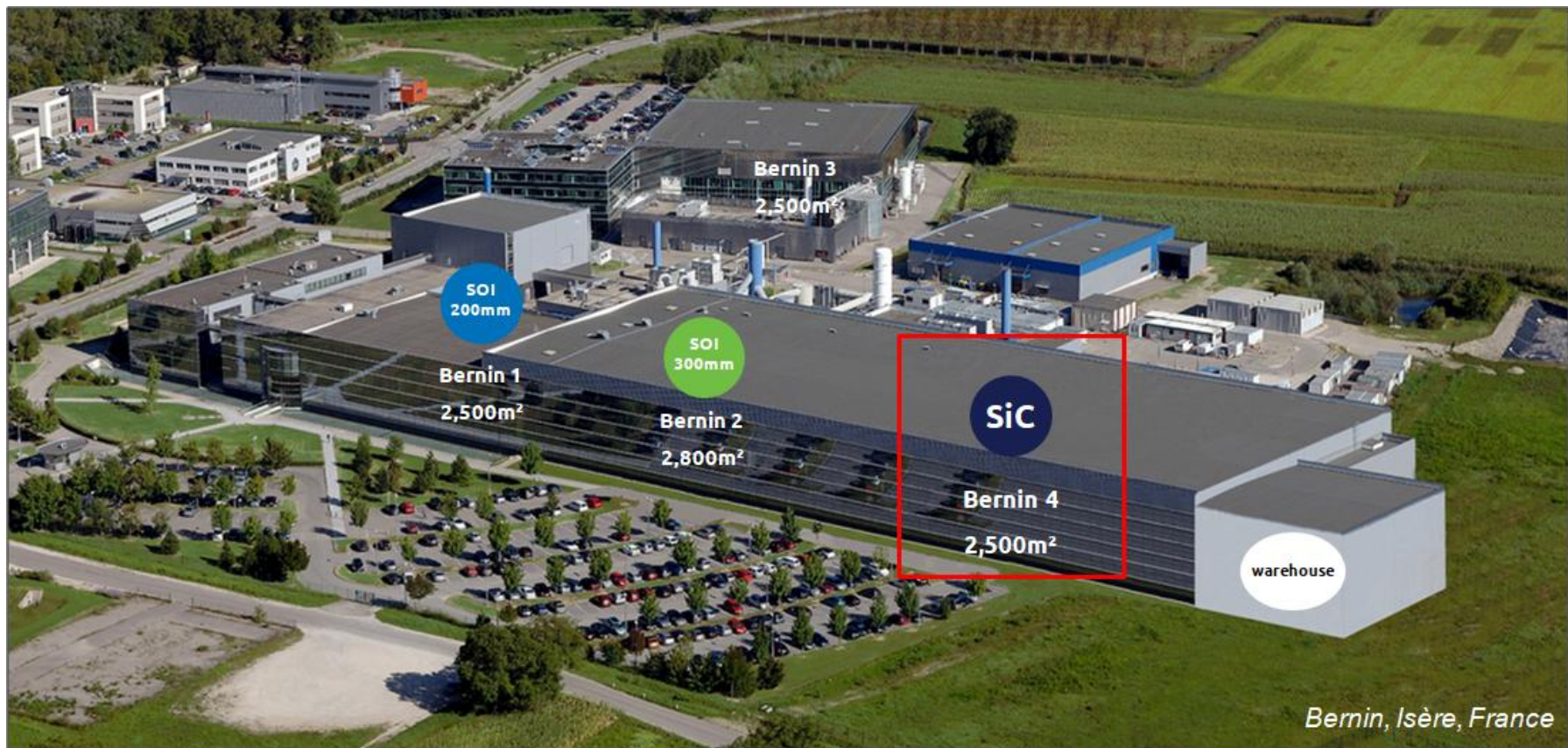
Conclusions



Conclusion

- Engineered substrates are an efficient way to bring device performances
- For Silicon Carbide the benefits are significant :
 - More devices per wafers,
 - More energy efficiency,
 - Less Carbon Emission.
- SmartSiC™ will be manufactured in Soitec HVM fab in Q3 2023.

Soitec to bring SiC to Silicon standards





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THANK YOU

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