



mec

Towards Sustainable Wet Processing for Advanced Integration
Technologies

Efrain Altamirano-Sanchez on behalf of the SIP team

SEMICON[®] EUROPA

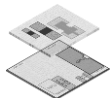
TechARENA 2022

SCREEN: Innovation Inspired by Sustainability

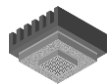
Core CMOS Research Enables Future Systems

System Technology Co-optimization

STCO



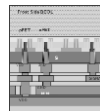
3D SOC
PARTITIONING



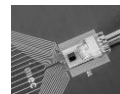
POWER WALL



NVM FOR
MACHINE
LEARNING

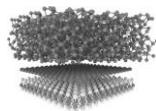


FUNCTIONAL
BACKSIDE



CO-PACKAGED
OPTICS

New Materials and Devices



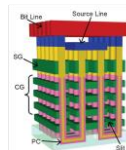
ATOMISTIC
MODELING



MATERIAL
SCREENING



CFET



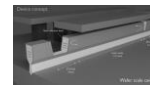
3D DRAM



VGSOT MAGNETIC
MEMORY

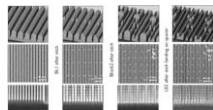


COLLOIDAL
STORAGE



III-V/ SILICON
LASER

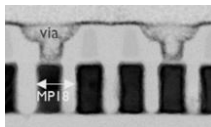
Density Scaling



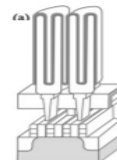
EUV MULTI-
PATTERNING



HIGH NA EUV



LOGIC
SCALING



DRAM CAP
SCALING



3D NAND
SCALING



3D
INTERCONNECT
SCALING

Wet processing: CIP & new challenges



Continues process improvement

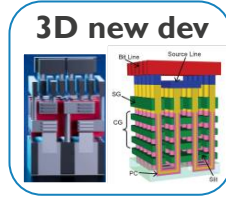
- Defectivity,
- Selectivity,
- Uniformity,
- Pattern collapse...

Density Scaling

EUV MULTI-PATTERNING HIGH NA EUV

DRAM CAP SCALING

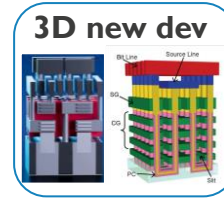
3D NAND SCALING LOGIC SCALING



New challenges in wet etch/clean

- Semiconductor Multicolour etching,
- Controlled recess,
- Dielectric multicolor etching,
- nm controlled recess,
- Wafer thinning,

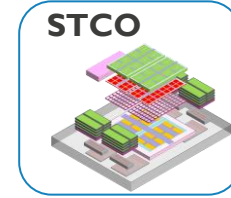
CFET 3D DRAM 3D IC SCALING



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CFET 3D DRAM 3D IC SCALING



New challenges in wet strip/clean

- High topography (>50 μm),
- μm thick PR strip,
- μm thick TBM strip,
- High selectivity to Cu/SiCN,
- Particles clean

STCO

D2W RDL FUNCTIONAL BACKSIDE W2W FOWLP

New Devices

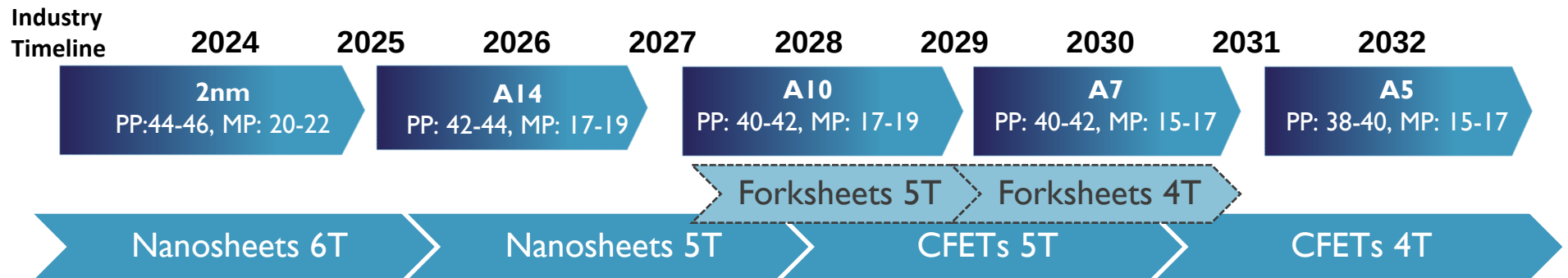
Energy efficiency

Water management

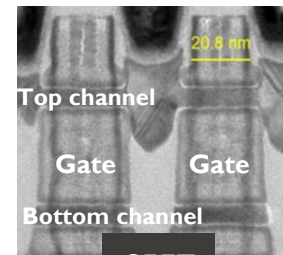
Sustainability

Formulated chemicals lifetime

Logic Scaling Roadmap

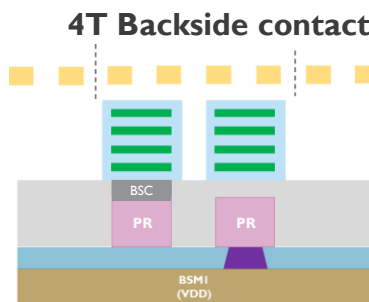
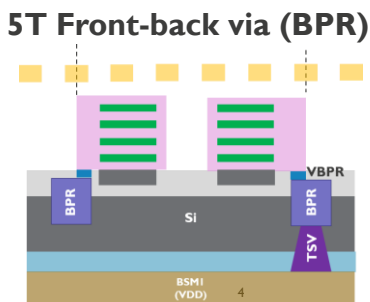
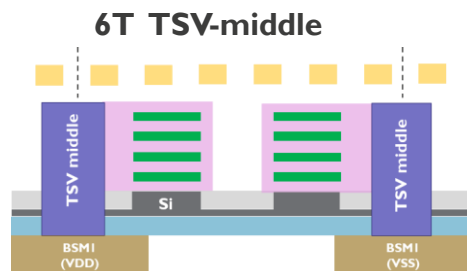


Device Architectures



PP: poly pitch (nm)
MP: dense metal pitch (nm)
CFET: Complementary FET

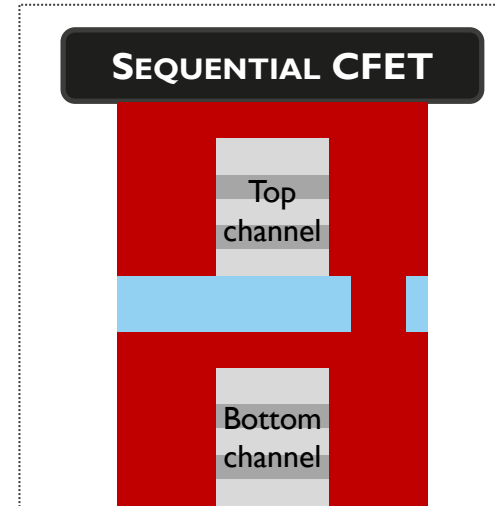
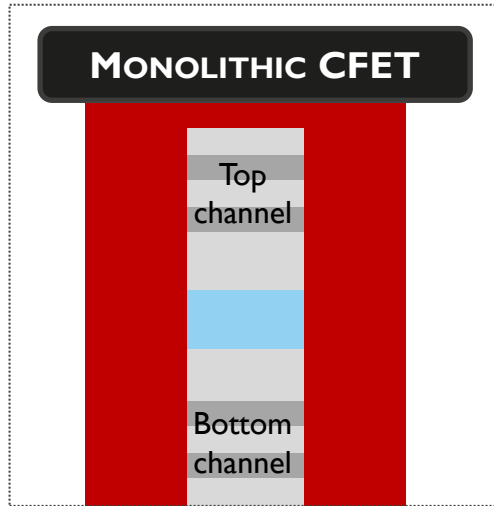
Back-side power delivery



CFET Back-side power delivery options

PR: Power rail
BPR: Buried power rail
BSC: Backside contact
VBPR: Via to BPR

CFET integration options

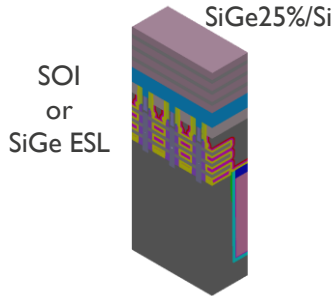


	Monolithic	Sequential
Pros	• Low cost & low R&C • Top-bottom self-aligned active & gate patt.	• 2D integration in top & bottom tiers • Top-bottom high m hybrid channel
Cons	• High AR patterning • Vertical integration in SD/Contact/RMG • Top-bottom high m hybrid channel difficult	• More process steps and cost • Wafer transfer defects & bonding ox scaling • Top-bottom gate connection & alignment • Top-bottom thermal budget constraints

CFET flow wet processing challenges

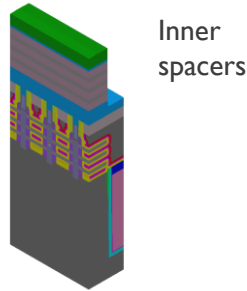
SEQUENTIAL CFET

Wafer bonding

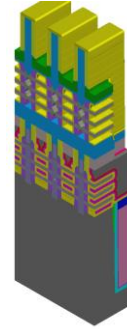


Wet challenges Wafer bonding defect

Active patterning

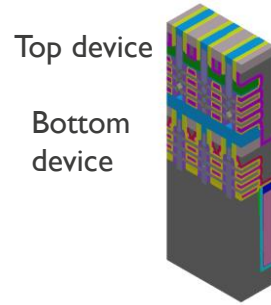


Top-bottom gate connection

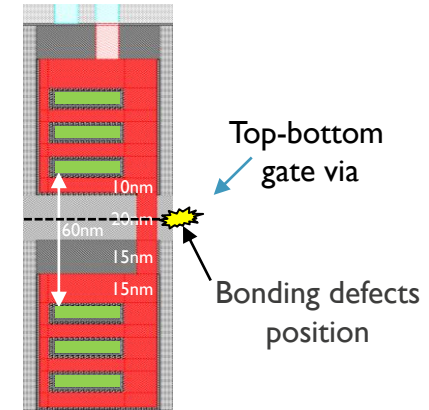


Top-bottom critical alignment

Finish top device process

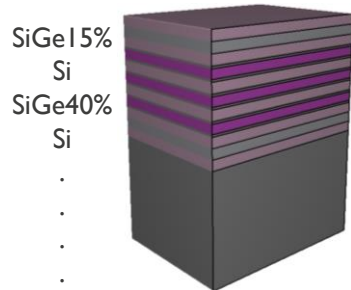


Top-bottom gate connection (defects)

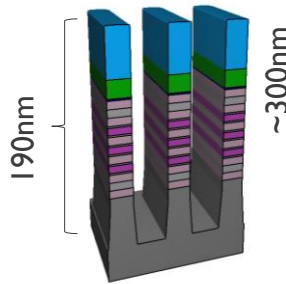


MONOLITHIC CFET

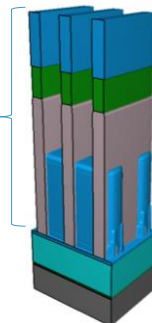
Super lattice



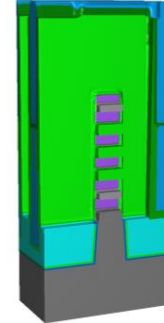
Active patterning



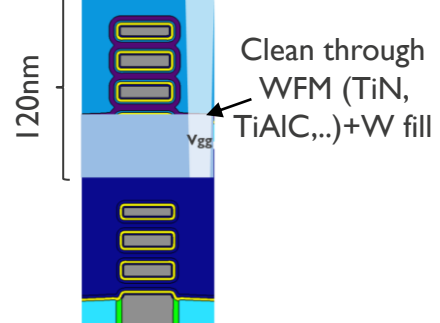
Gate and SiGe40% SE



SiGe15% + RMG

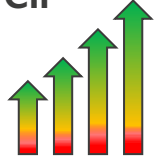


Via patterning



Wet processing: CIP & new challenges

CIP



Continues process improvement

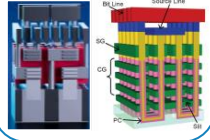
- Defectivity,
- Selectivity,
- Uniformity,
- Pattern collapse...

EUV MULTI-PATTERNING HIGH NA EUV

DRAM CAP SCALING

3D NAND SCALING LOGIC SCALING

3D new dev

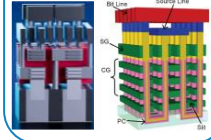


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CFET 3D DRAM FUNCTIONAL BACKSIDE 3D IC SCALING

3D new dev

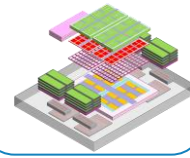


New challenges in wet etch/clean

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CFET 3D DRAM FUNCTIONAL BACKSIDE 3D IC SCALING

STCO



▪ New challenges in wet strip/clean

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- μm thick TBM strip,
- High selectivity to Cu/SiCN, W2W

D2W RDL 3D INTERCONNECT SCALING FOWLP

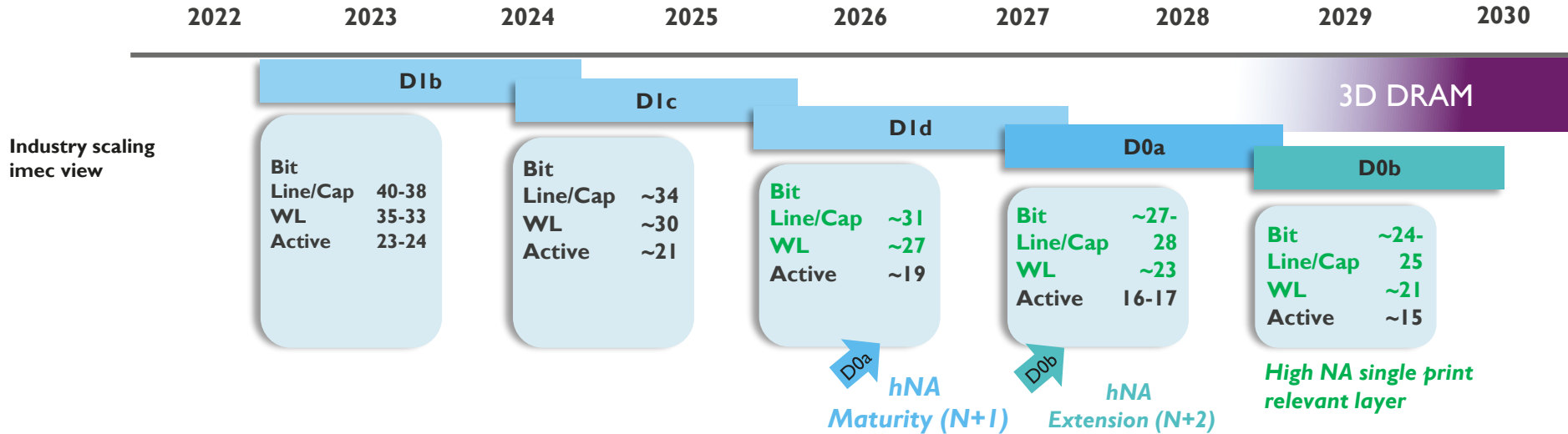
Energy efficiency

Water management

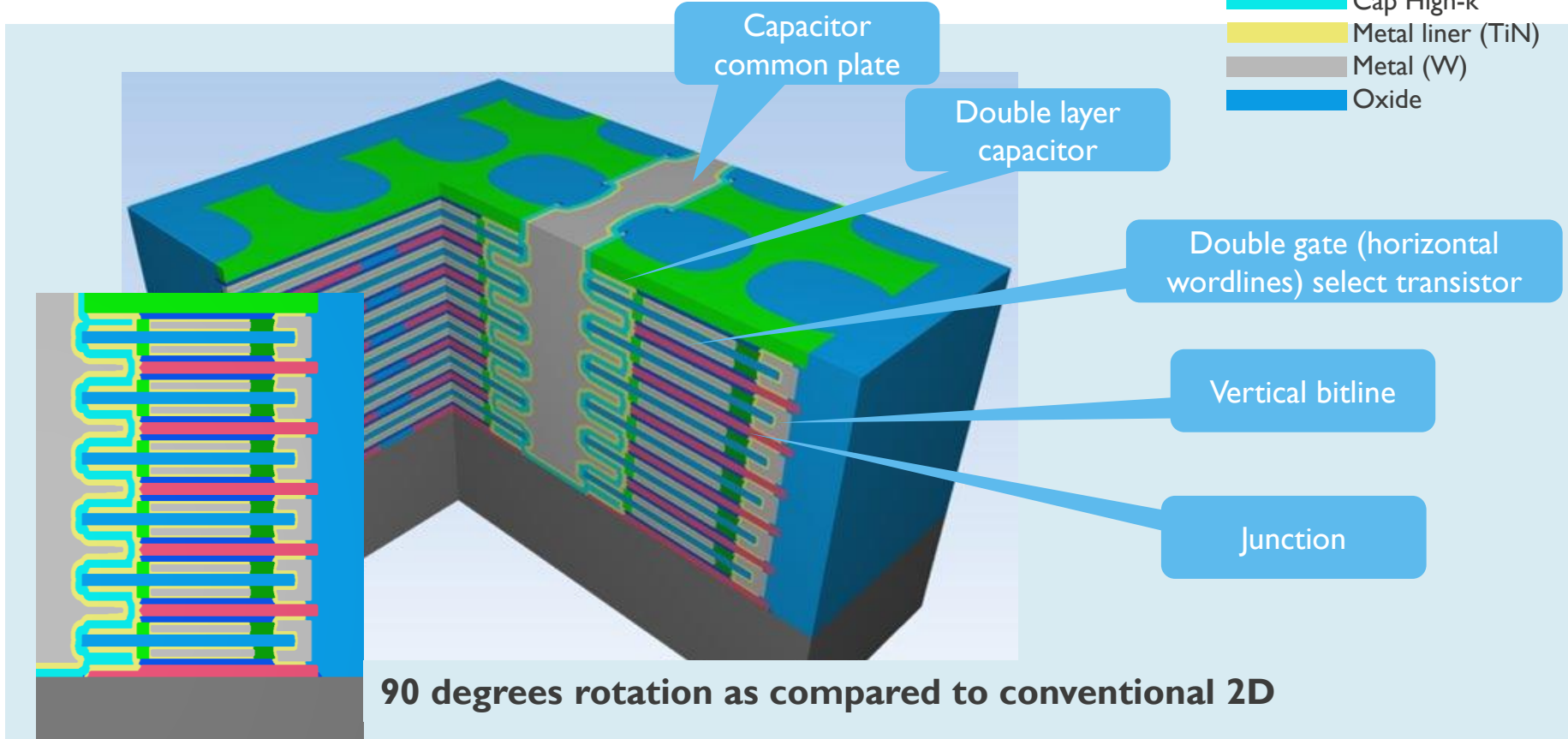
Sustainability

Formulated chemicals lifetime

IMEC High NA single patterning DRAM roadmap

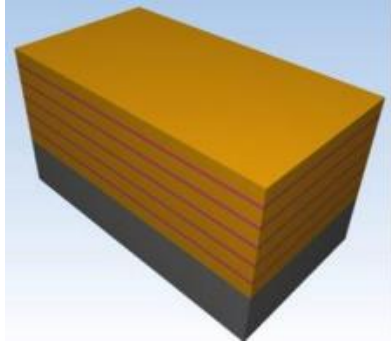


3D DRAM with silicon channel



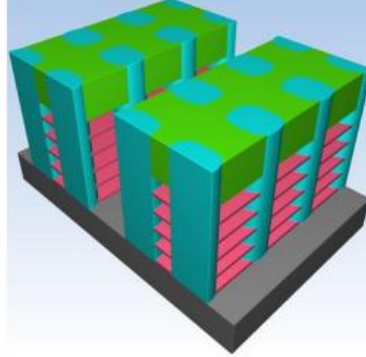
3D DRAM with silicon channel

Si/SiGe20% EPI superlattice

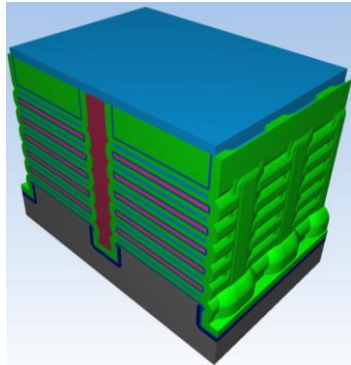


SE and residues cleaning

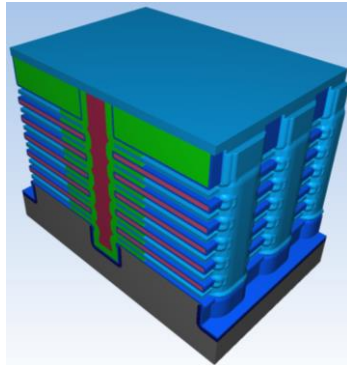
SiGe20% Sheet release



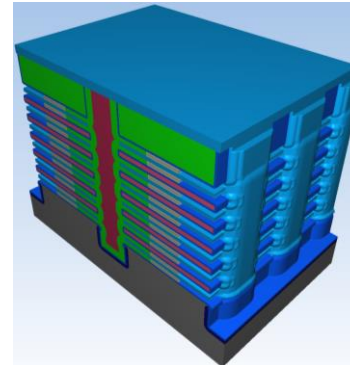
SiN deposition



Selective GOx

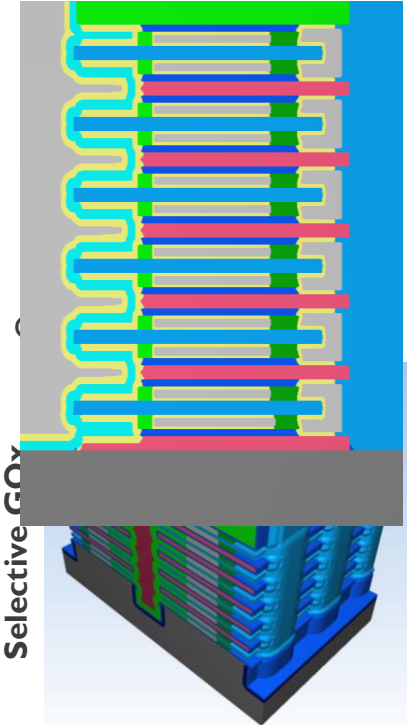


Metal Gate (TiN/W,Mo) recess



Selective GOx

- Si
- Gate dielectric
- Cap High-k
- Metal liner (TiN)
- Metal (W)
- Oxide



Wet processing: CIP & new challenges



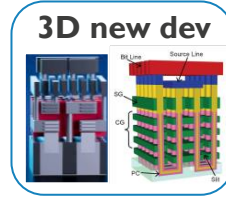
Continues process improvement

- Defectivity,
- Selectivity,
- Uniformity,
- Pattern collapse...

EUV MULTI-PATTERNING HIGH NA EUV

DRAM CAP SCALING

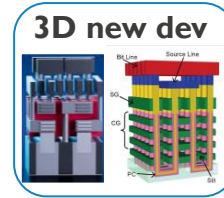
3D NAND SCALING LOGIC SCALING



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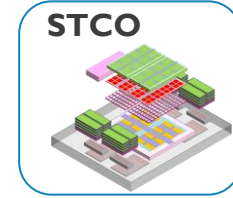
CFET 3D DRAM FUNCTIONAL BACKSIDE 3D IC SCALING



New challenges in wet etch/clean

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CFET 3D DRAM FUNCTIONAL BACKSIDE 3D IC SCALING



▪ New challenges in wet strip/clean

- High topography ($>50 \mu\text{m}$),
- μm thick PR strip,
- μm thick TBM strip,
- High selectivity to Cu/SiCN, W2W

D2W RDL 3D INTERCONNECT SCALING FOWLP

Energy efficiency

Water management

Sustainability 

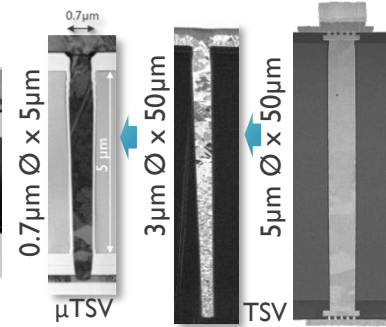
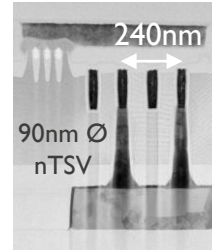
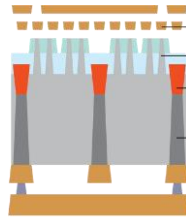
Formulated chemicals lifetime

Vision and Grand challenges 3D System Integration

High Performance
Heat Spreading
& Heat Removal

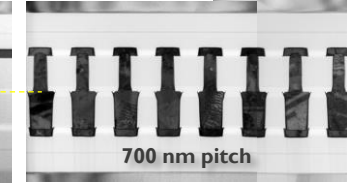
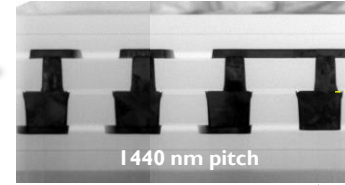


Improved Power
delivery network
architecture



Through-Si Via connections

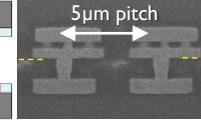
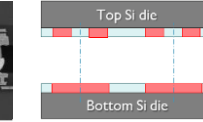
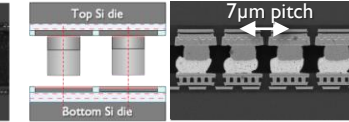
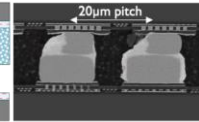
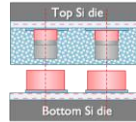
High Density
W2W Stacking



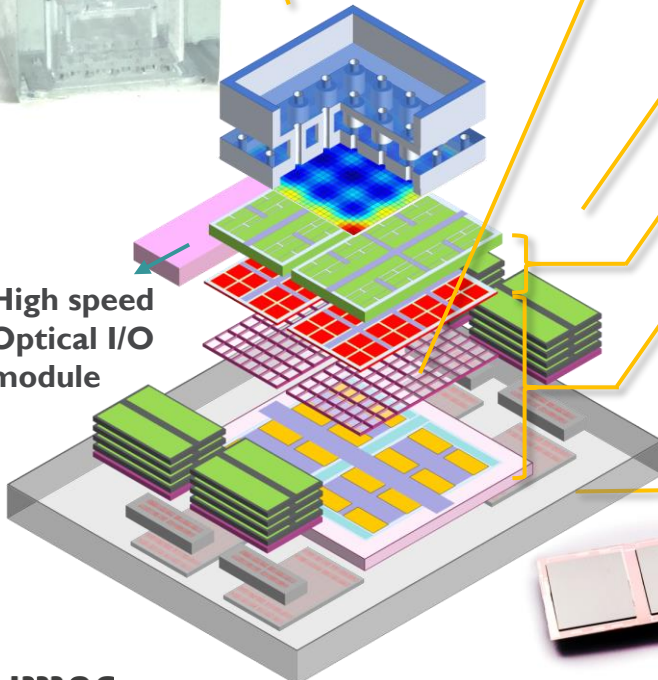
High Density
D2W Stacking
Pitch = 40 $\Rightarrow$ 20 μ m

EMBEDDED μ BUMPS
 $\Rightarrow$ 10 $\Rightarrow$ 7 μ m $\Rightarrow$ 5 μ m

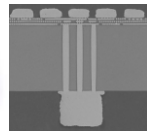
CU/CU DIRECT BONDING
 $\Rightarrow$ 5 $\Rightarrow$ 2 μ m



High speed
Optical I/O
module



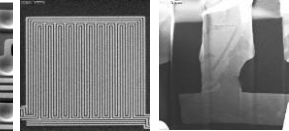
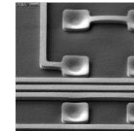
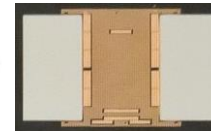
Si-interposer



Reconstructed wafer interposer



High Density RDL



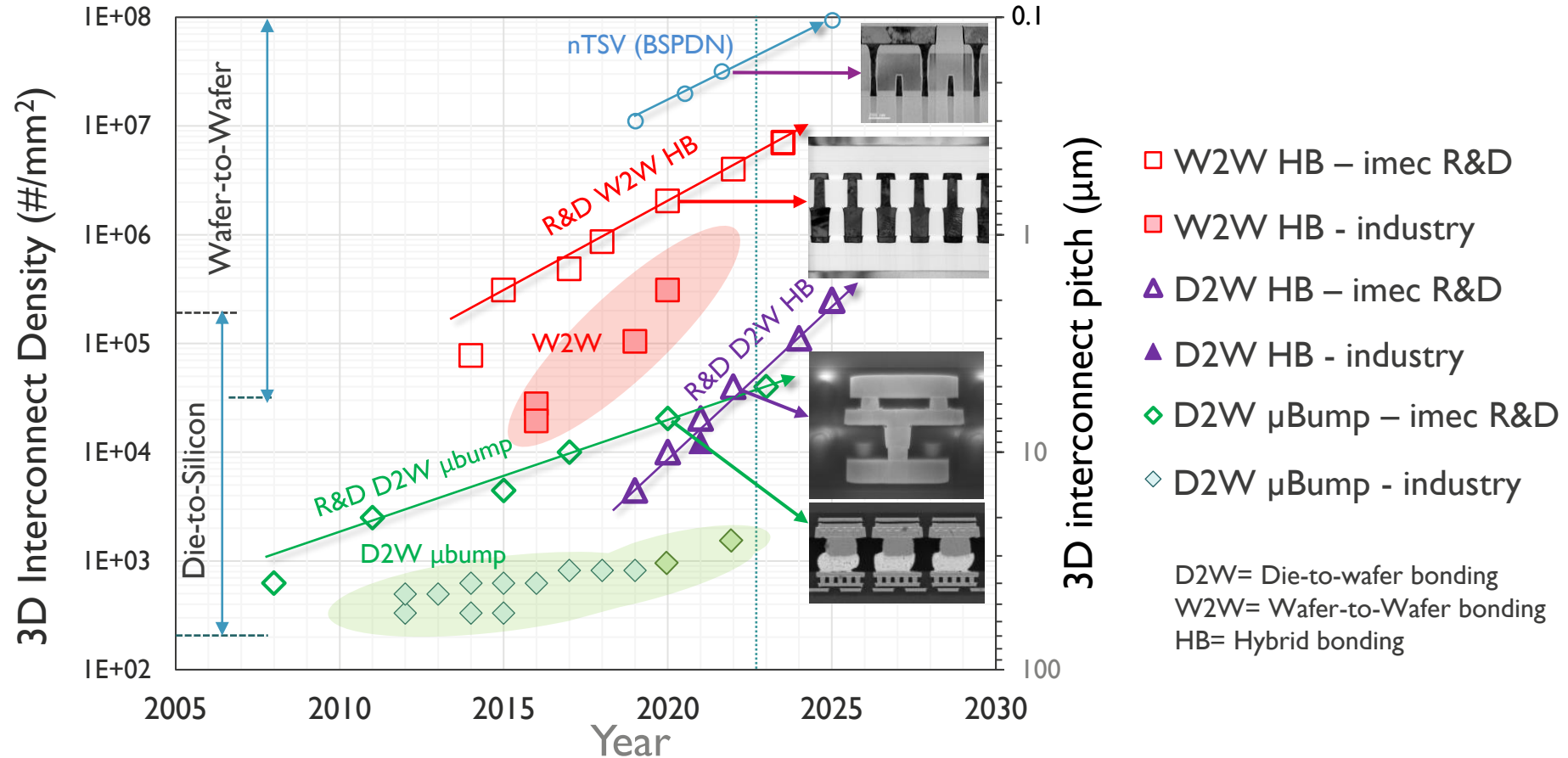
Si Bridge in FO-WLP

2 μ m L/S

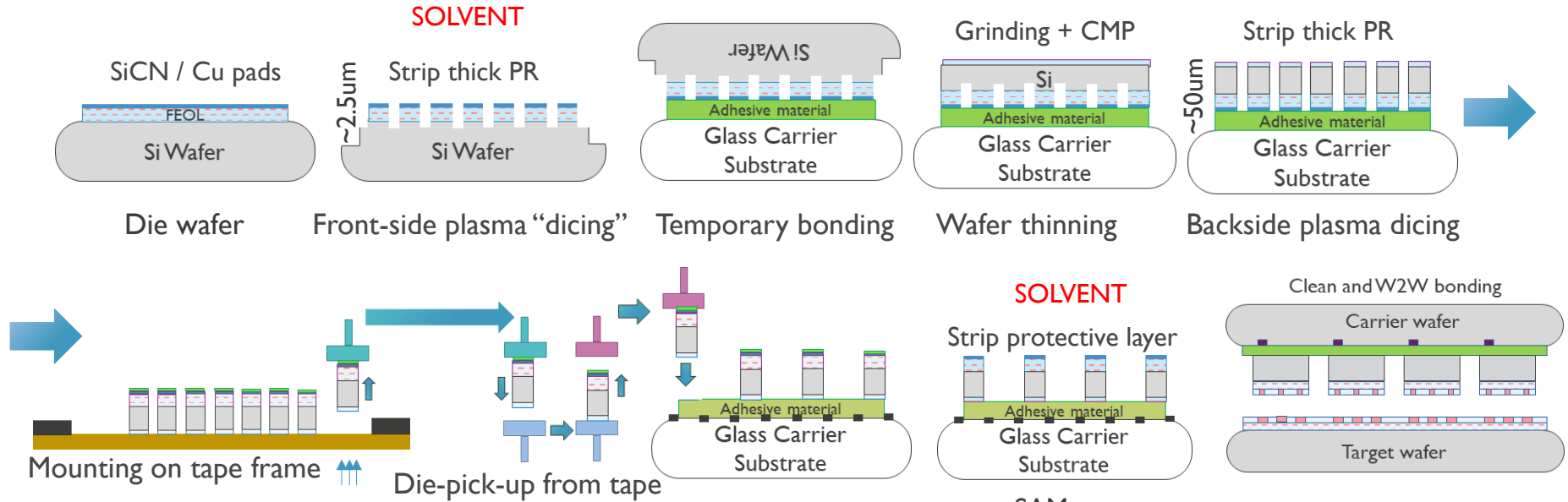
1 μ m L/S Dual Damascene

Efrain Altamirano-Sanchez

3D Landscape and imec 3D Interconnect R&D Roadmap

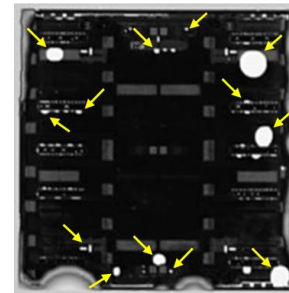


Strip of TBMs and Photoresist



... and very loooong DIW rinsing

*TBM = Temporary bonding material

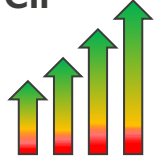


Large distribution in void size

- Killer void size $\sim \frac{1}{2}$ pitch (?)
- Void size $\sim 10(0) \times$ defect size

Wet processing: CIP & new challenges

CIP



Continues process improvement

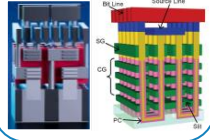
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3D NAND SCALING LOGIC SCALING

3D new dev

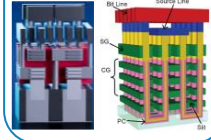


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CFET 3D DRAM FUNCTIONAL BACKSIDE 3D IC SCALING

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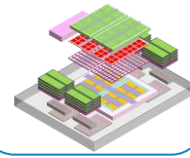


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D2W RDL 3D INTERCONNECT SCALING FOWLP

Energy efficiency

Water management

Sustainability

Formulated chemicals lifetime

WET: Electricity and Water use per Process

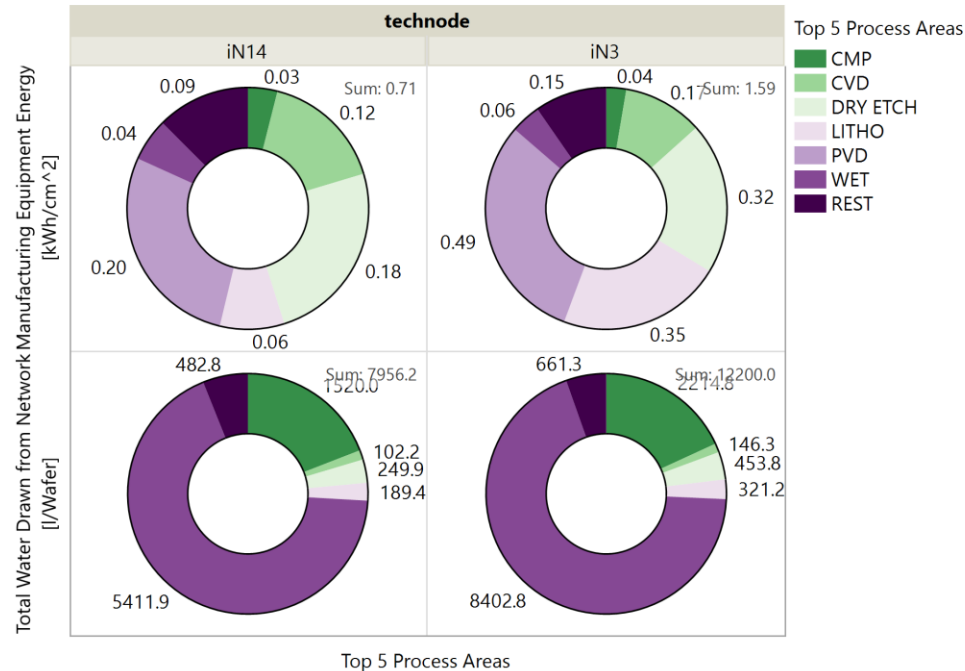
Imec logic v0.2 – Pareto Per Process Area

Energy efficiency

Water management

Sustainability 

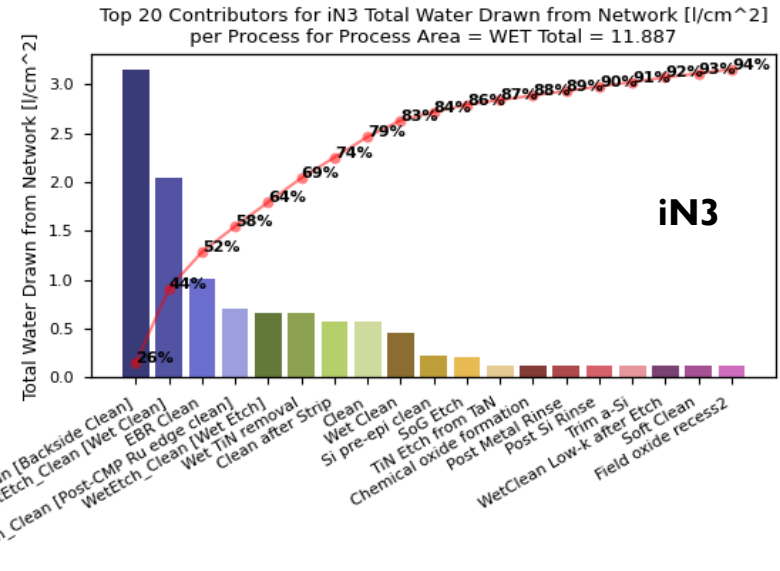
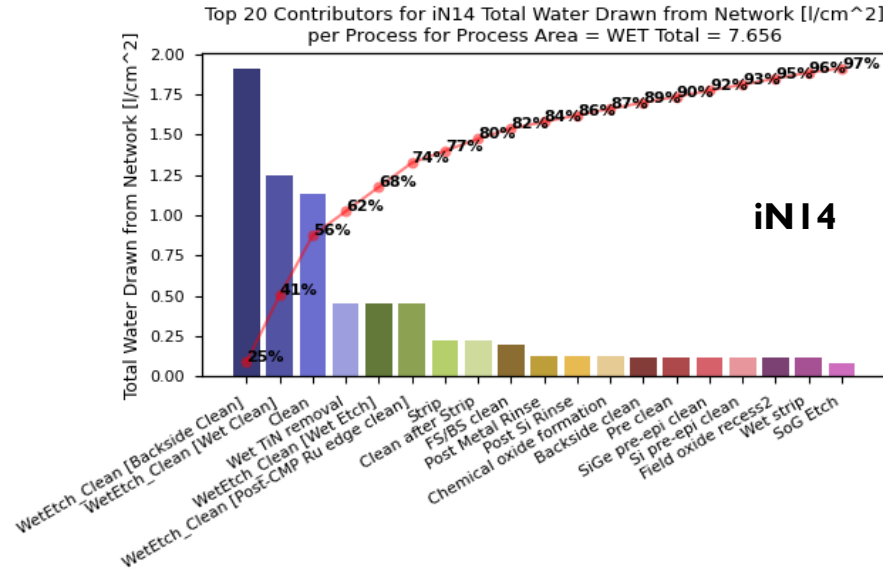
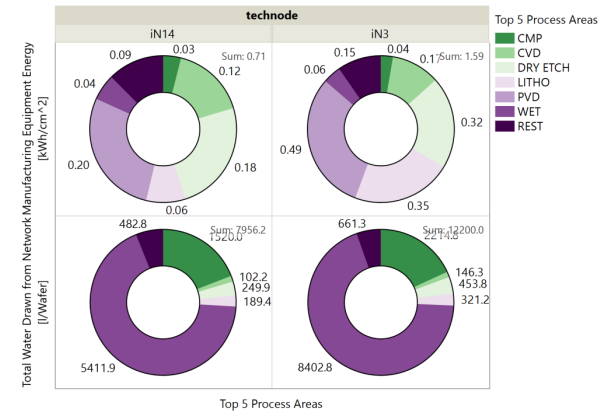
Formulated chemicals lifetime



WET: Electricity and Water use per Process

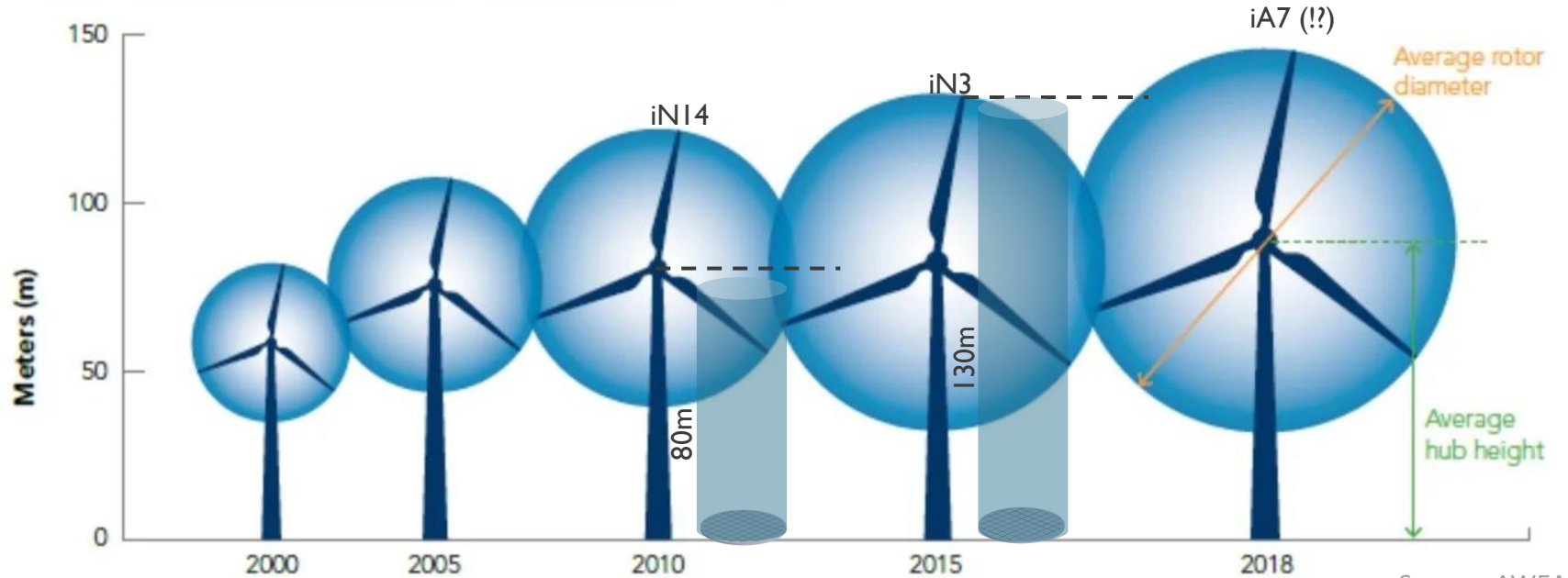
Pareto Per Process Area

- Further classification of wet processes required...



Water usage per technology

Consumption normalized to total chip area produced: (V/A: dimension Length)



<https://www.greentechmedia.com/articles/read/the-pros-and-cons-of-ultra-tall-wind-turbine-towers>

Source: AWEA

M. Garcia Bardon, 2020 IEEE (IEDM) | 978-1

P.W. Mertens et al., ECS2017 fall: ECS Transactions, 80 (2) 73-79 (2017).

Ian Brown, SCREEN SPCC 2022

Efrain Altamirano-Sanchez

In a nutshell

- **Continues process improvement (CIP)**
 - Defectivity, selectivity, uniformity, pattern collapse... --> Sustainability → Energy efficiency, water management,
- **What are the new challenges in cleaning?**
 - Multiple selective isotropic etch → Formulated chemistries
 - Metal cleaning & residue removal → Commodity and formulated chemistries
 - Polymer strip → Solvents and formulated chemistries
 - Sustainability → Energy efficiency, water management, and chemistries' lifetime
- **Where are those challenges?**
 - New architectures → Logic (3D CFET), Memory (3D DRAM) and 3D system integration
- **What is different?**
 - Multicolor etching
 - Controlled isotropic etching
 - Selective μm thick polymers (photoresists and temporary bonding materials)
 - More formulated chemicals needed
- **How are we addressing these challenges to maximize the wet processing performance and the cost-benefit?**
 - Disruptive technologies



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