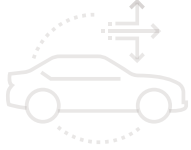


Automotive Semiconductor Reliability – A New Collaborative Approach

Contamination management
and maturity of the
ecosystems

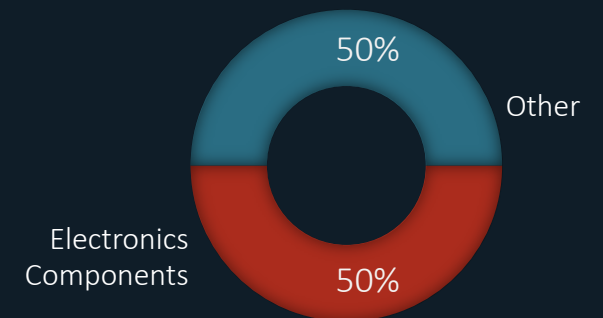




90% of auto innovation is
driven by electronics

Quality ↔ Speed

Expected 2030 Car Costs



The Necessity to Create Frameworks

GAAC – EUROPE CHAPTER

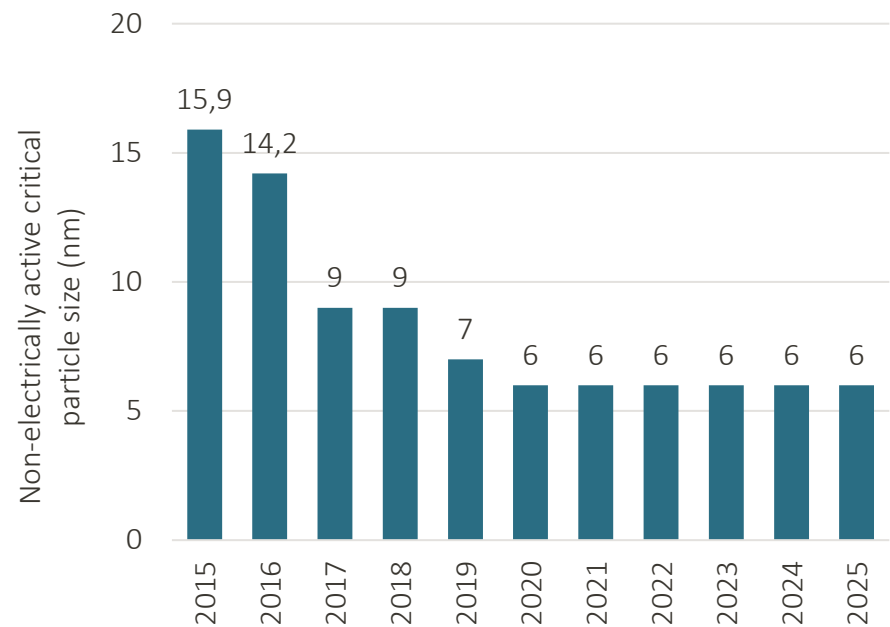


Automotive Electronics Council
Component Technical Committee

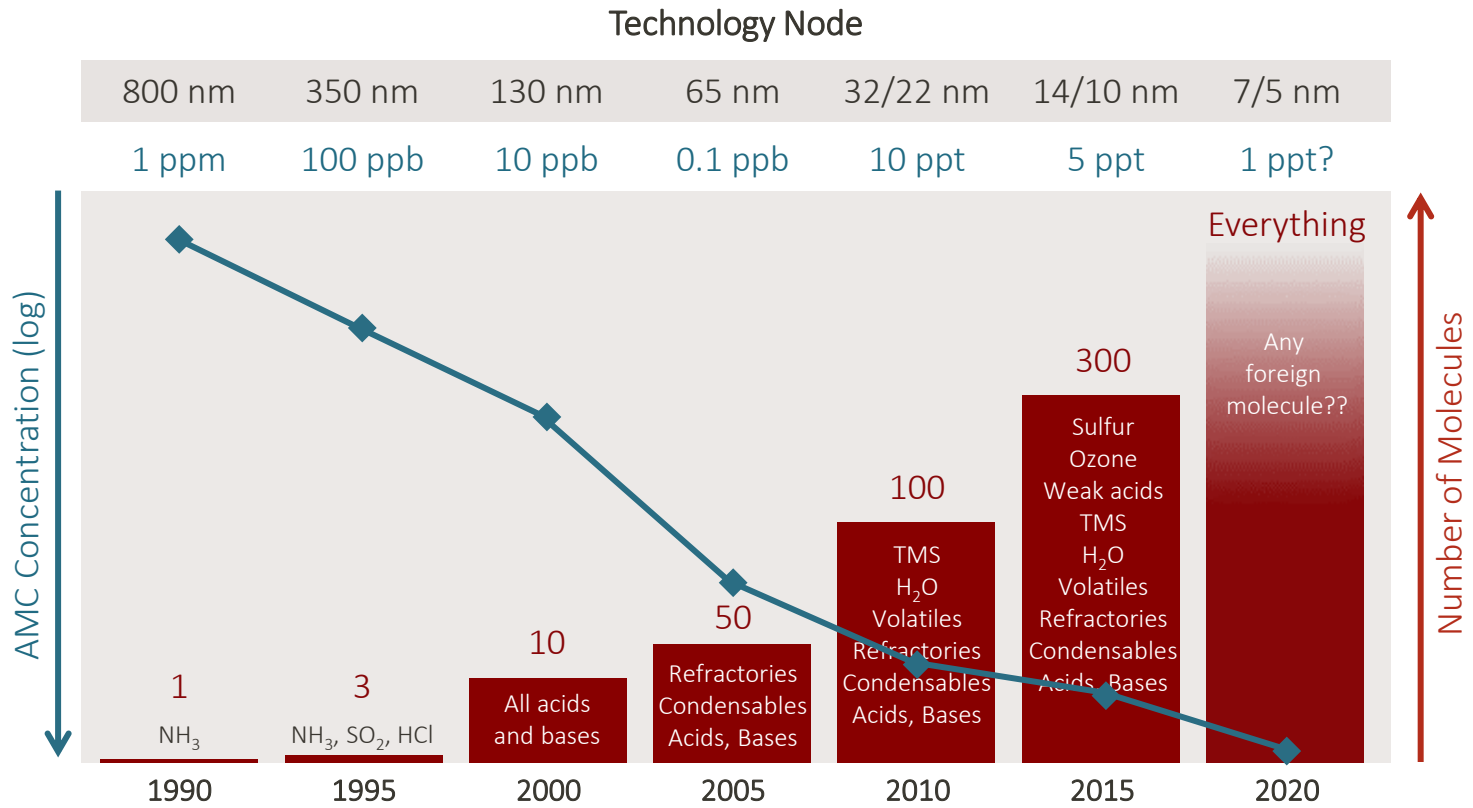
AEC-Q004
Automotive Zero Defects

Best practices focused
on the areas of
manufacturing, test,
reliability and continuous
improvement methods

Pervasive Contamination



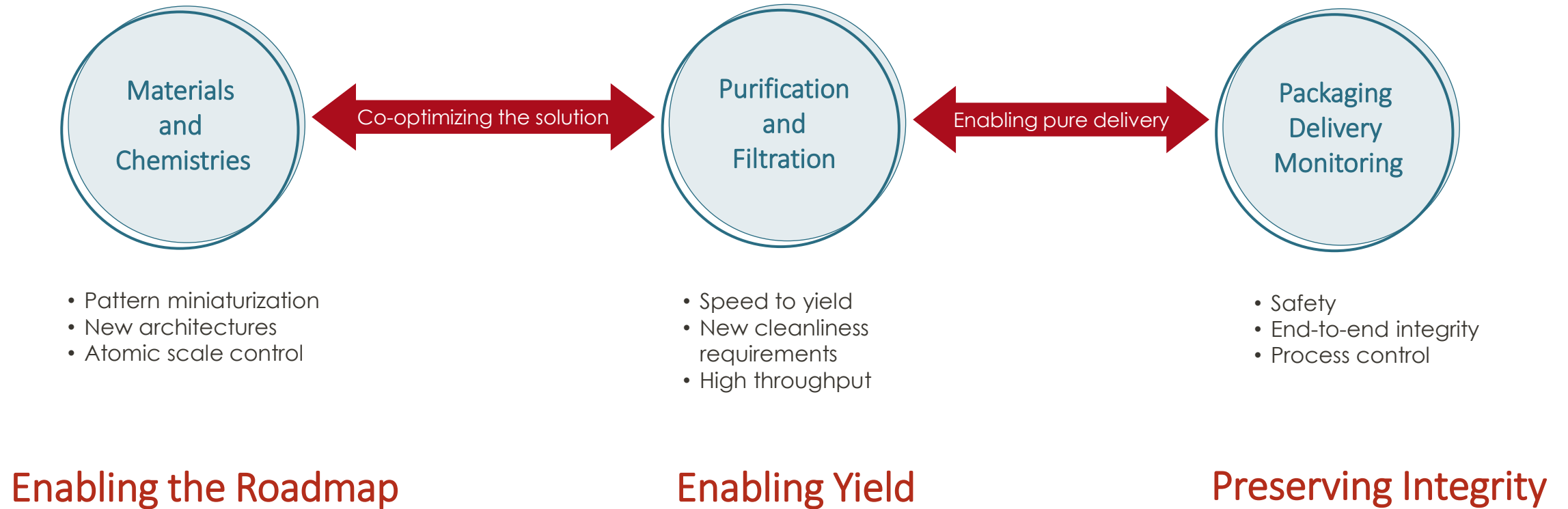
Critical particle size and total metals identified by the IRDS roadmap



AMC contamination concerns by technology node

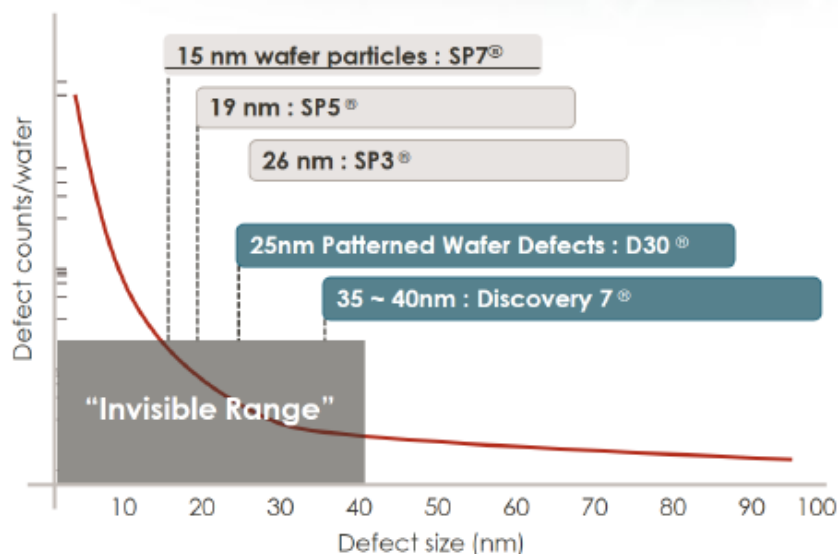
A range of contaminants that cannot be seen

Entegris value proposition



Capture the Root Cause of Latent Defects

Functional Safety Appetizer Statements



Entegris / VWAG, IQPC –
The Zero Defect Conference
for Semiconductors, 30 Sept.
– 2 Oct. 2019

Graph source: ASM (2008, 2015, 2019)

In-line Fab monitoring reaches its limits when reliability defects are out of the detection limit – **you do not see!**

Can we capture those latent defects on an electrical basis via smart testing ?

No, only to a limited extent → testing cannot compensate this.

What to do ?

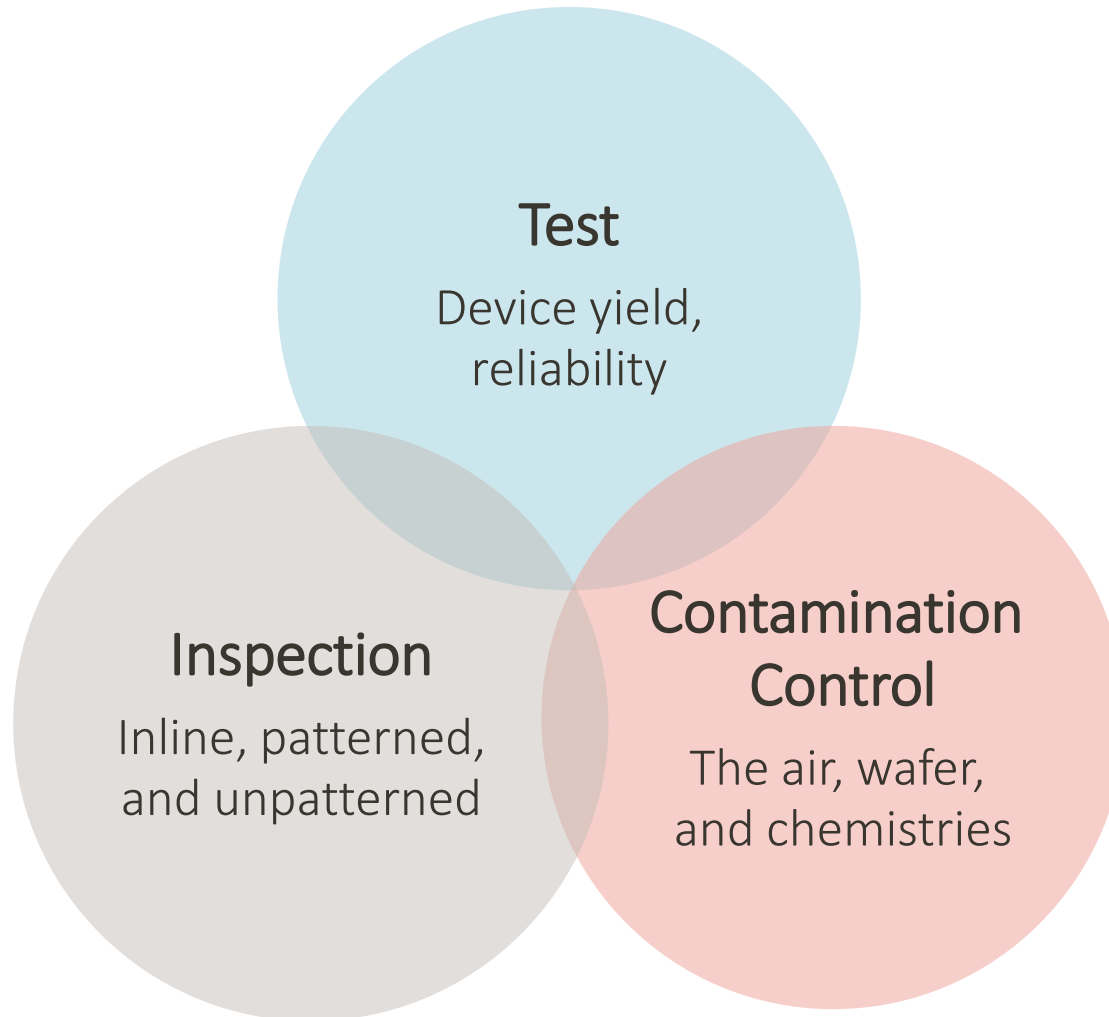
Quality assurance is a through the supply-chain approach - electrical testing a part of it!

Contamination Control – air, wafer, chemistry

Here, material supply chain management, filtration & purification needs to be effectively applied to capture the root cause of latent defects.

► Compliance to safety = Re-think the assurance chain – who can do what?

Addressing Weak Links in Auto Reliability

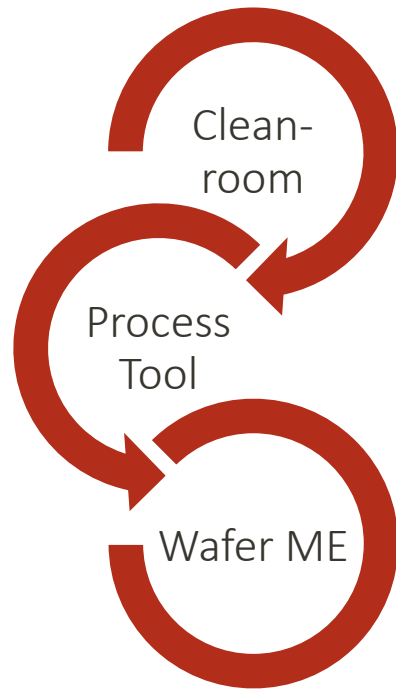


Improve baseline and
reduce excursions



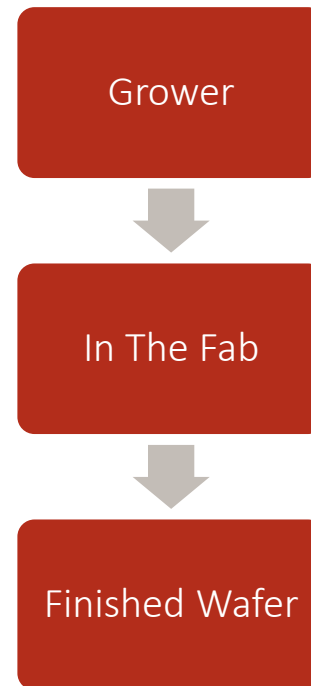
Contamination Management Strategy

The Air



AMC Control

The Wafer



Wafer Management

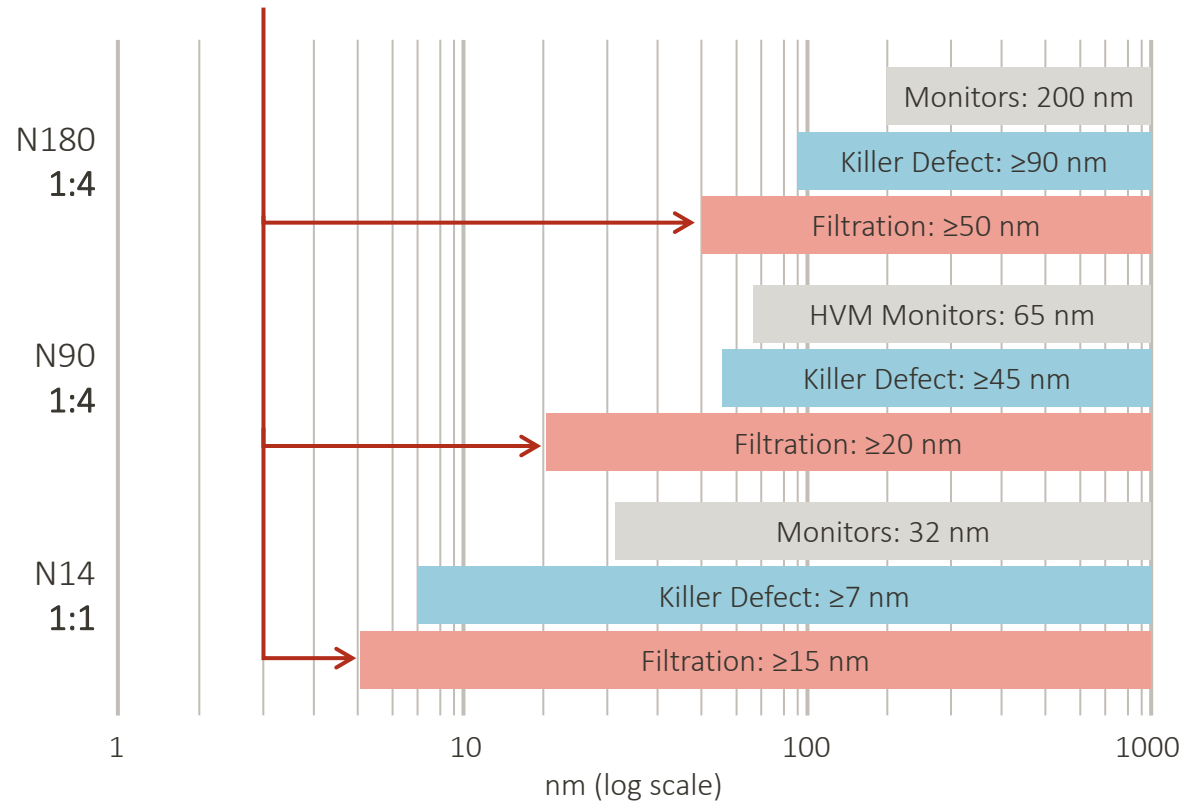
The Chemistries



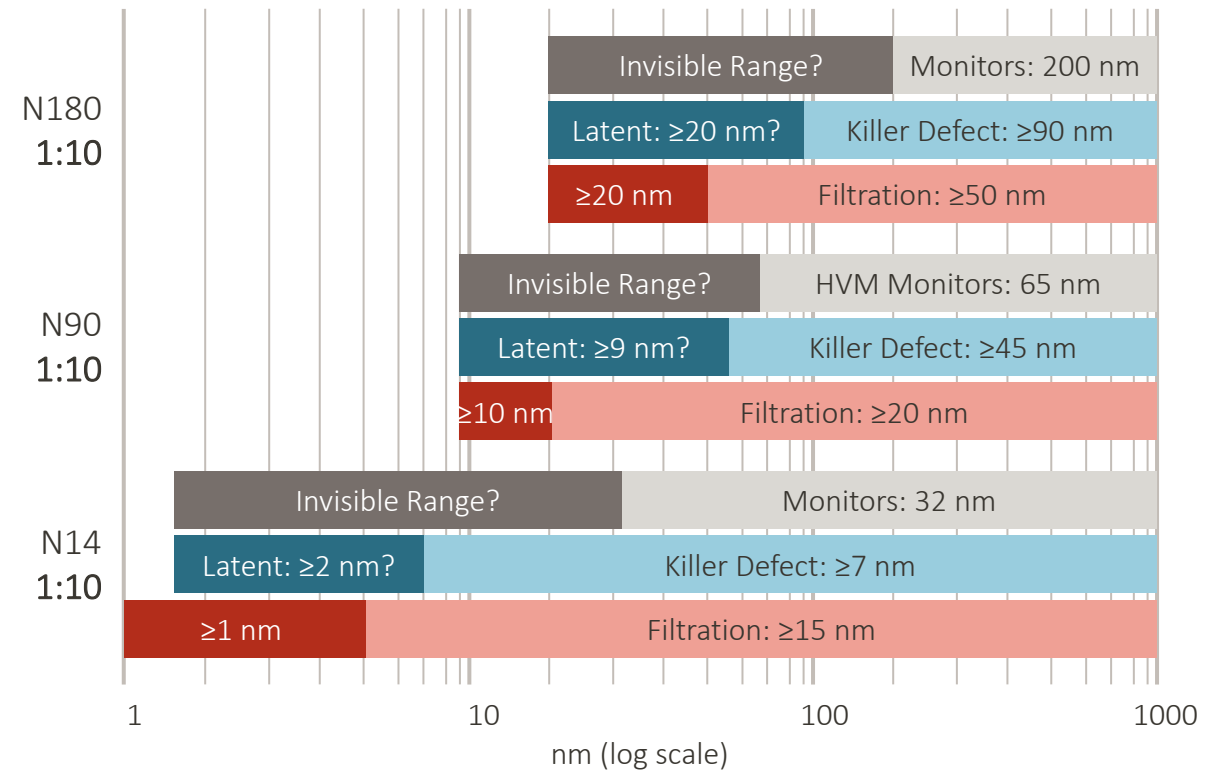
Clean Delivery

New Filtration Strategies with Auto IC

Historical Filtration Strategies with “1:4 Rule”

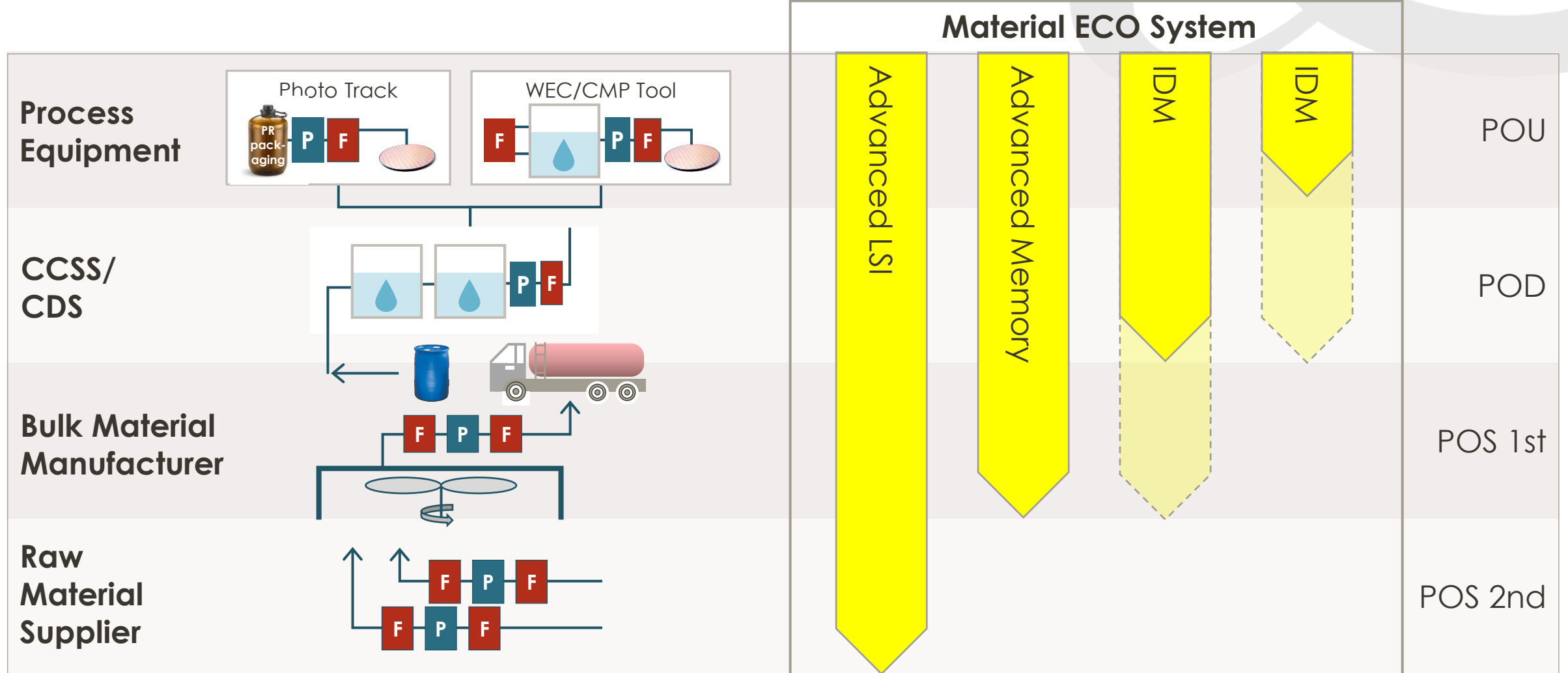


Improvement of Latent Defect Management with “1:10 Rule”



Note: all dimensions related to filtration are an indicator of retention rating

Management across supply chain



F Filtration P Purification

- Need to consider total ECO system improvement for chemical induced wafer defectivities

Sustain the strategy



Improve total quality
without relying solely
on inspection and testing

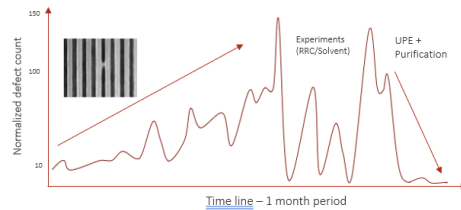
Case studies, case studies, case studies...

Metal Contamination in Solvents

Lithography

Results

- Resist pattern on Si



Lessons Learned – Changes Made

Upgrade particle filtration stage from 10 nm UPE to 3 nm UPE

Widespread usage of solvent purification and UPE 3 nm filtration at POU for improvement of stack defectivity

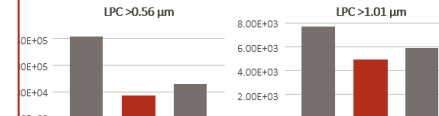
Upgrade facility's solvent filtration into purification

Microscratch Defect

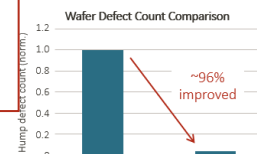
CMP

Results

Results Comparison



Pattern Wafer Results Comparison



Lessons Learned – Changes Made

The drop in particle count as measured inline correlated to approximately **96% reduction** in hump defects after film deposition

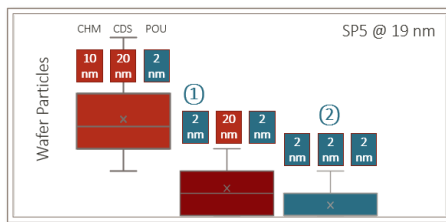
The increased surface area of the slurry filter has a positive impact on the removal efficiency of defect-causing particles

Coherent approach from BCM till POU

Wet Cleans

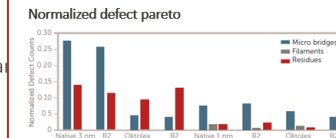
Results

Large improvement of on-wafer defects with same filtration at Chemical Manufacturer, Chemical Distribution System and Process tool

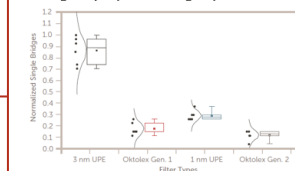


Space Pattern in 193i

Results



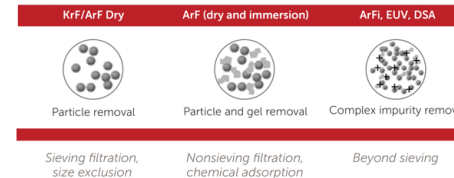
Normalized single bridge count/wafer, arranged by experimental group



Lessons Learned – Changes

Retention can be enhanced by **membrane technology** with dimensions (CD), line width and the exposure dose

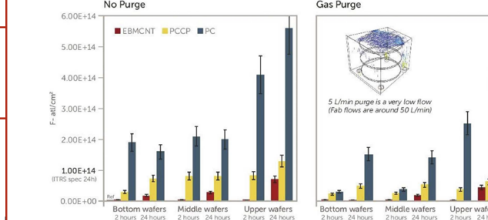
Complexity of contamination removal increases with the technology



AMC Control During Queue Time

AMC

Results



Lessons Learned – Changes Made

Purge, wet cleaning, and FOUF material are a set of variables that have great impact on yield

The **best strategy** to improve yield and minimize wafer loss is through a combination of these solutions: using a lower absorbing material, purging in highly sensitive process steps, and wet cleaning

Technology node	Process location	Process	Purge type	Contaminant	Defect	Result with EBM	Result with PC
28-nm	FEOL	After High-k etch	Standard	H ₂ O	Condensation defect after High-k etch	2 particles	75 particles
45-nm and below	FEOL	Shallow trench isolation (STI)	Standard	H ₂ O	Excessive etch	Excellent side wall profile	
45-nm and below	BEOL	Many different steps	Standard	H ₂ O	Condensation defect after M1 etch	100 particles	2000 particles
45-nm and below	BEOL	Top metal etch	Standard	H ₂ O	Crystal defect after top metal etch	<50 particles	>1000 particles
45-nm and below	BEOL	Dual-damascene on metal line	Standard	H ₂ O	Excessive etch	Excellent side wall profile	

How does the ecosystem perform?

	Contamination Control Solution	Location A	Location B	Location C	Location D	Location E
Lithography	Bulk Solvent Purification	●	●	●	●	●
	Resist Packaging		●	●	●	●
	Dispense Pumps	●	●	●	●	●
	POU Filter – Resist	●	●	●	●	●
	POU Filter/Purifier – Solvent	●	●	●	●	●
	Reticle Pod		●	●	●	●
	AMC Filter	●	●	●	●	●
Etch & Clean	Bulk Filter	●	●	●	●	●
	POU Filter – FEOL	●	●	●	●	●
	POU Filter – BEOL	●	●	●	●	●
	Metal Purification DIW	●	●	●	●	●
	Metal Purification IPA	●	●	●	●	●
	Post-Etch Clean	●	●	●	●	
CMP	Bulk Filter	●	●	●	●	
	Particle Monitoring	●		●	●	●
	Concentration Monitoring			●	●	●
	CMP FEOL POT Filter	●	●	●	●	●
	CMP BEOL POT Filter	●	●	●	●	●
	Pad Conditioner	●	●	●	●	●
	Brush	●	●	●	●	●
	Post-CMP Clean	●	●	●	●	●
Deposition	CVD Deposition Precursor Delivery	●	●	●	●	●
	Plating Chemistries		●	●	●	
	Cu Plating Filtration		●	●	●	
Implant	GeF ₄	●	●	●	●	●
	Insitu cleaning gas					
	Gas AsH ₃	●	●	●	●	●
	Gas PH ₃	●	●	●	●	●
	Gas BF ₃	●	●	●	●	●
Fab Facility	Bulk Gas Purification			●	●	●
	AMC Filter		●	●	●	●
	FOUP or SMIF Pods	●	●	●	●	●
	Finished Wafer Shipper (HWS)		●	●		●

When compared to the optimized solution, the current solution in place:

- Is not adequate
- Can be improved
- Is equal or better
- Is not known

Benchmark for contamination control

- A list of reference
- A comparator
- A tool
- An indicator of maturity

Maturity of the car maker's ecosystem

	Contamination Control Solution	Maturity	Location A	Location B	Location C	Location D	Location E
Lithography	Bulk Solvent Purification	1	●	●	●	●	●
	Resist Packaging	1		●	●	●	●
	Dispense Pumps	1	●	●	●	●	●
	POU Filter – Resist	3	●	●	●	●	●
	POU Filter/Purifier – Solvent	2	●	●	●	●	●
	Reticle Pod	3		●	●	●	●
	AMC Filter	2	●	●	●	●	●
Etch & Clean	Bulk Filter	1	●	●	●	●	●
	POU Filter – FEOL	1	●	●	●	●	●
	POU Filter – BEOL	1	●	●	●	●	●
	Metal Purification DIW	1	●	●	●	●	●
	Metal Purification IPA	3	●	●	●	●	●
	Post-Etch Clean	3	●	●	●	●	●
CMP	Bulk Filter	1	●	●	●	●	●
	Particle Monitoring	1	●		●	●	●
	Concentration Monitoring	1			●	●	●
	CMP FEOL POT Filter	1	●	●	●	●	●
	CMP BEOL POT Filter	1	●	●	●	●	●
	Pad Conditioner	1	●	●	●	●	●
	Brush	1	●	●	●	●	●
	Post-CMP Clean	3	●	●	●	●	●
Deposition	CVD Deposition Precursor Delivery	3	●	●	●	●	●
	Plating Chemistries	1		●	●	●	
	Cu Plating Filtration	2		●	●	●	
Implant	GeF ₄	3	●	●	●	●	●
	Insitu cleaning gas						
	Gas AsH ₃	2	●	●	●	●	●
	Gas PH ₃	2	●	●	●	●	●
	Gas BF ₃	2	●	●	●	●	●
Fab Facility	Bulk Gas Purification	3			●	●	●
	AMC Filter	2		●	●	●	●
	FOUP or SMIF Pods	2	●	●	●	●	●
	Finished Wafer Shipper (HWS)	3		●	●		●

Maturity of the Ecosystem

Percentage of the players who have an adequate solution in place:

3	Minimum 75%
2	Between 50% and 75%
1	Less than 50%

When compared to the optimized solution, the current solution in place:

- Is not adequate
- Can be improved
- Is equal or better
- Is not known

Example: assessment of the 28N ecosystem

1. Deposition, Implant, and Fab Facility are more mature
2. Litho and CMP are less mature
3. Etch & Clean is an area of focus

Current SiC Industry Challenges



CAPACITY

Increased demand leading to capacity constraints in SiC fabs and substrate manufacturers



QUALITY

High efficiency devices require high-quality substrates with low defectivity



COST OF OWNERSHIP

Achieving consistent yields at low cost of ownership while maintaining quality

SiC – A New Collaborative Approach

At the wafer and device manufacturing level

Hot Topics



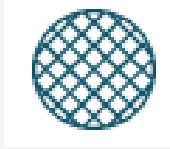
POLISHING TIME AND
MICROSCRATCHES

Achieve consistent low surface
roughness and low defectivity



GATE OXIDE
BREAKDOWN

Prevent contamination at
deposition and cleaning steps



FRAGILE WAFER
HANDLING

Address both edge defects
and shipping damage

A New Collaborative Approach

Holistic – Test, inspection and contamination control

“The Air, the Wafer, the Chemistries”

Maintain the strategy over the long term



Links to joint paper and panel discussion:

[A Collaborative Approach for Automotive Electronics \(semiconductordigest.com\)](https://semiconductordigest.com)
April/May 2021 edition

[SEMI – ENTEGRIS – CARIAD SE \(Volkswagen\) Panel Discussion | SEMI](#)
July 2021

Thank you!

Q&A