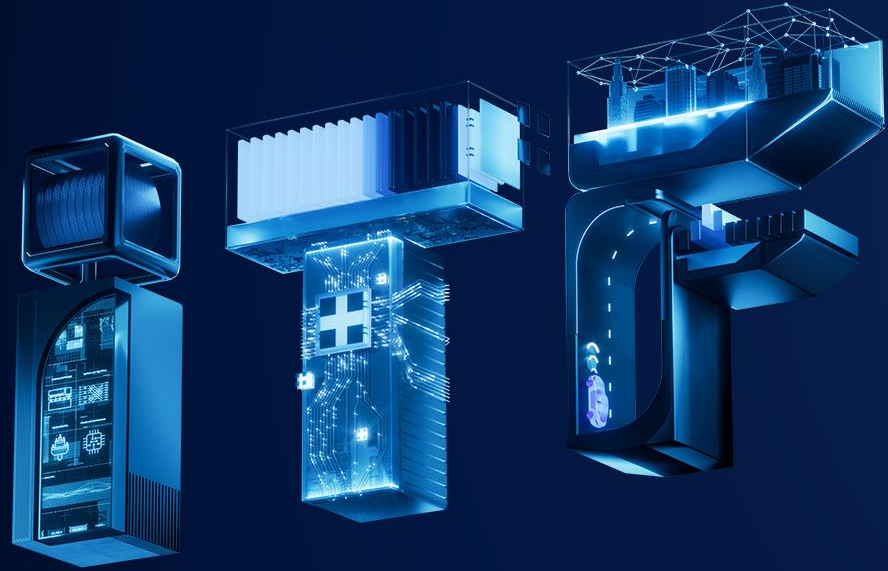




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Explore
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+

How heterogeneous integration will shape the future of wireless communications

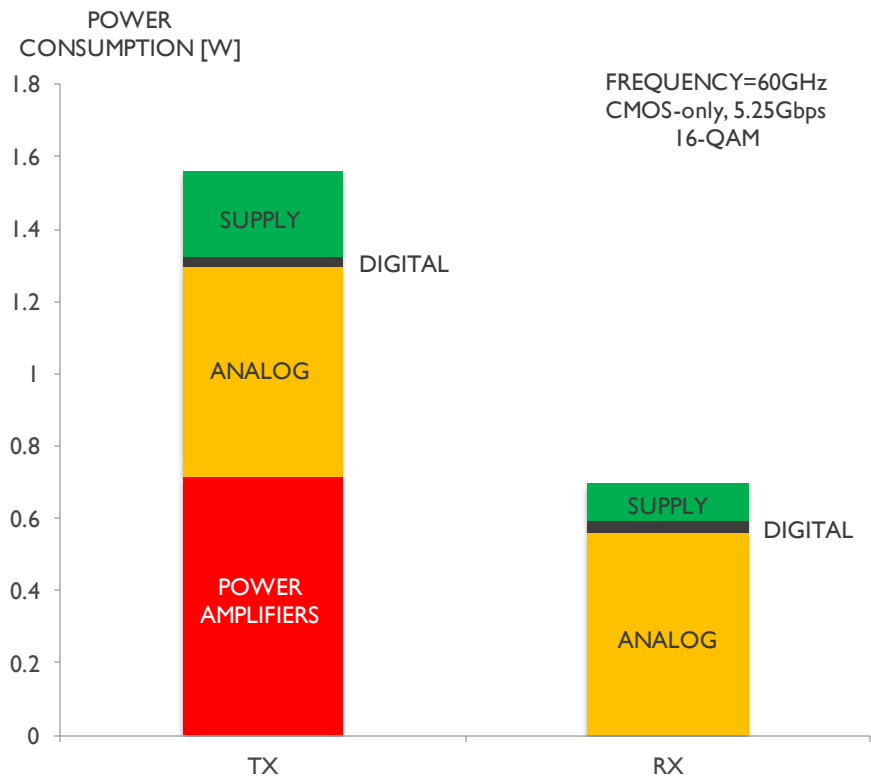
Nadine Collaert, program director Advanced RF



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IMEC TECHNOLOGY FORUM

Power and efficiency are challenges for mm-wave and sub-THz applications



C. Desset et al., GlobeCom WS 2021.

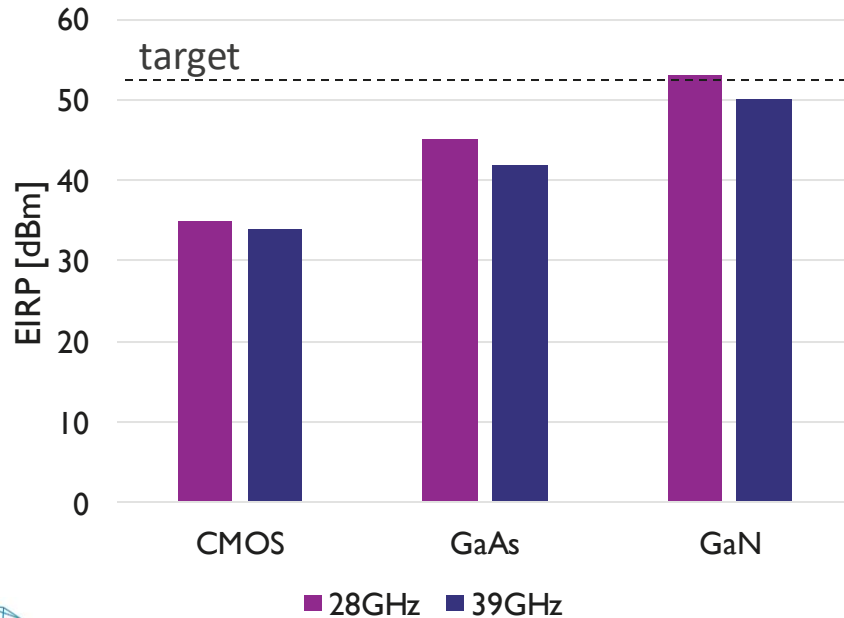
System level study shows:

- + TX-side most power-hungry
- + Total power consumption is heavily PA-dominated
- + Becomes even more challenging at higher frequencies, longer distance and for footprint restricted use cases

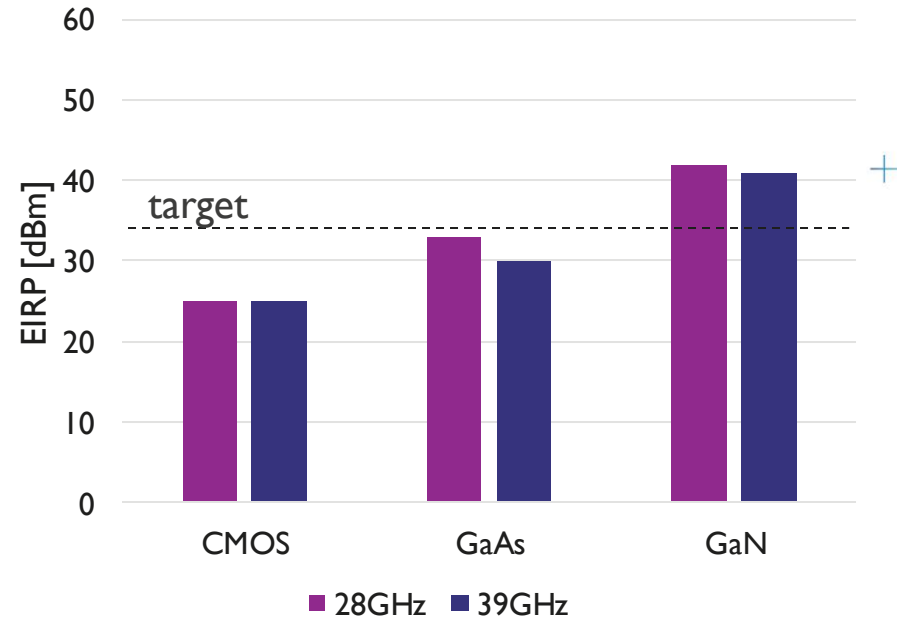
GaN for infrastructure and UE at FR2 mm-wave frequencies?



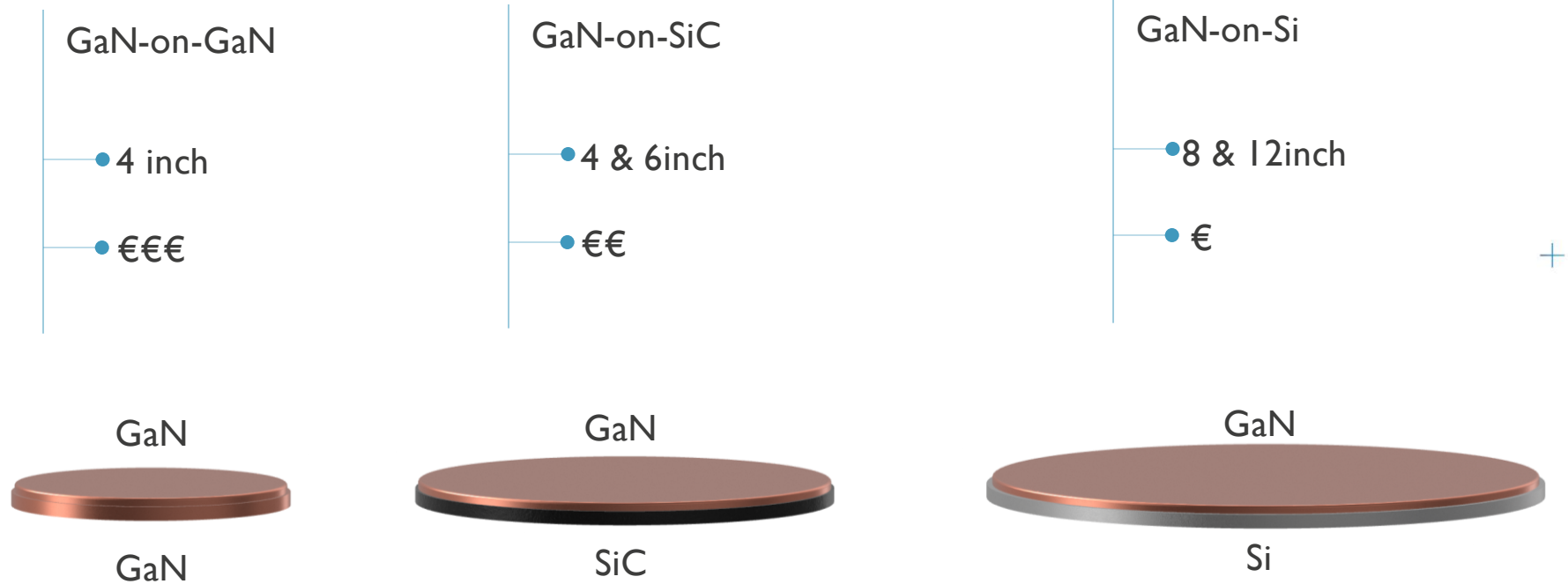
Fixed Wireless Access – 4x4 array



User equipment – 1x4 array

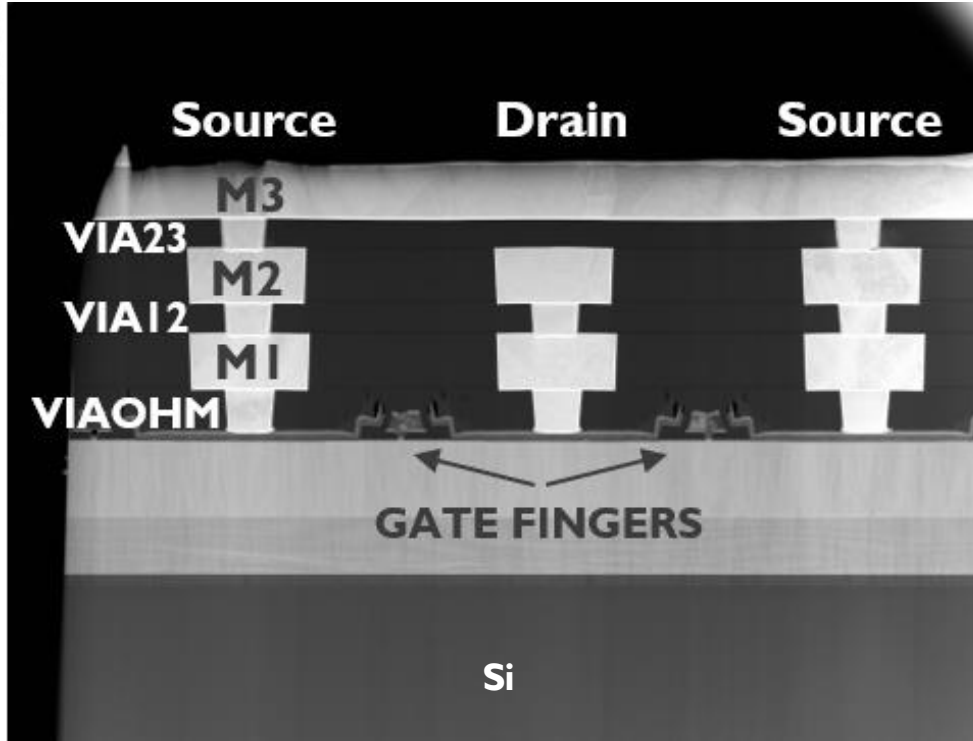


There are different flavors of Gallium Nitride (GaN)



200mm GaN-on-Si platform for mm-wave applications

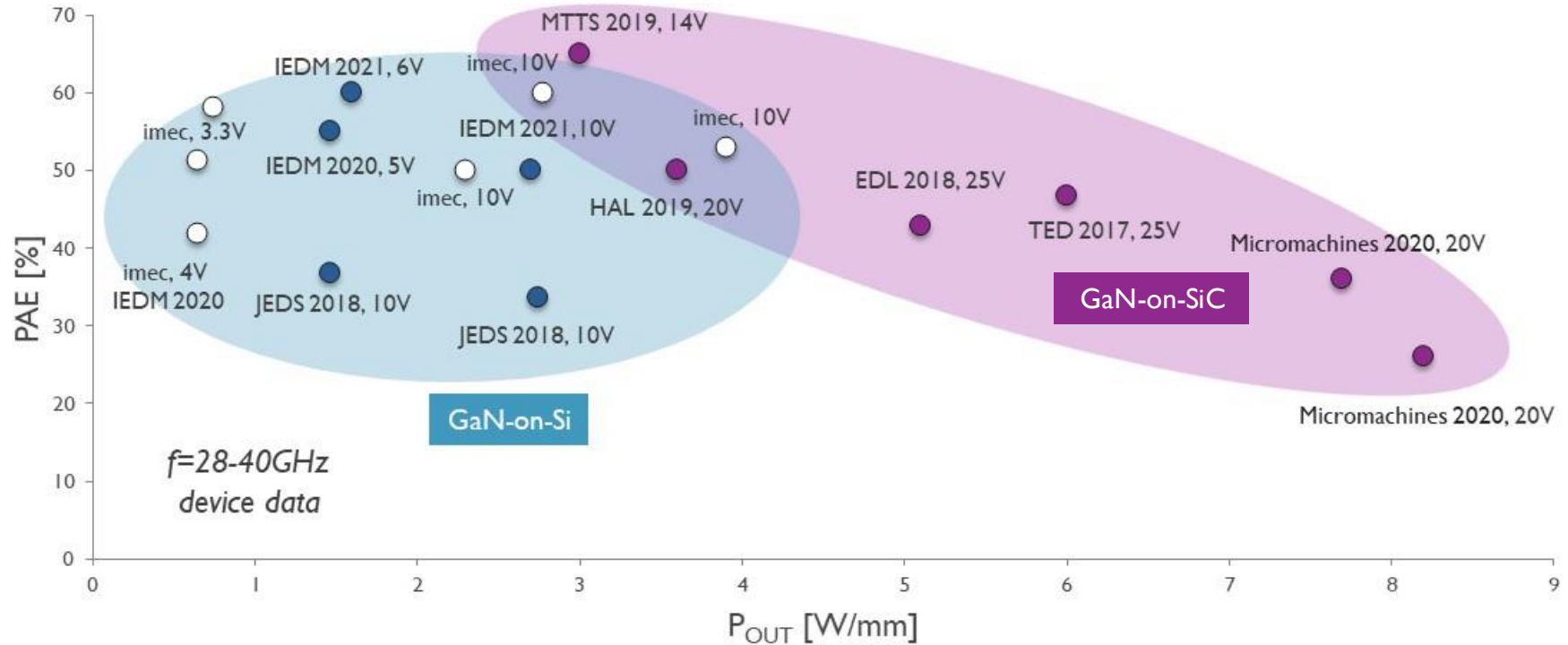
B. Parvais et al., IEDM 2020.



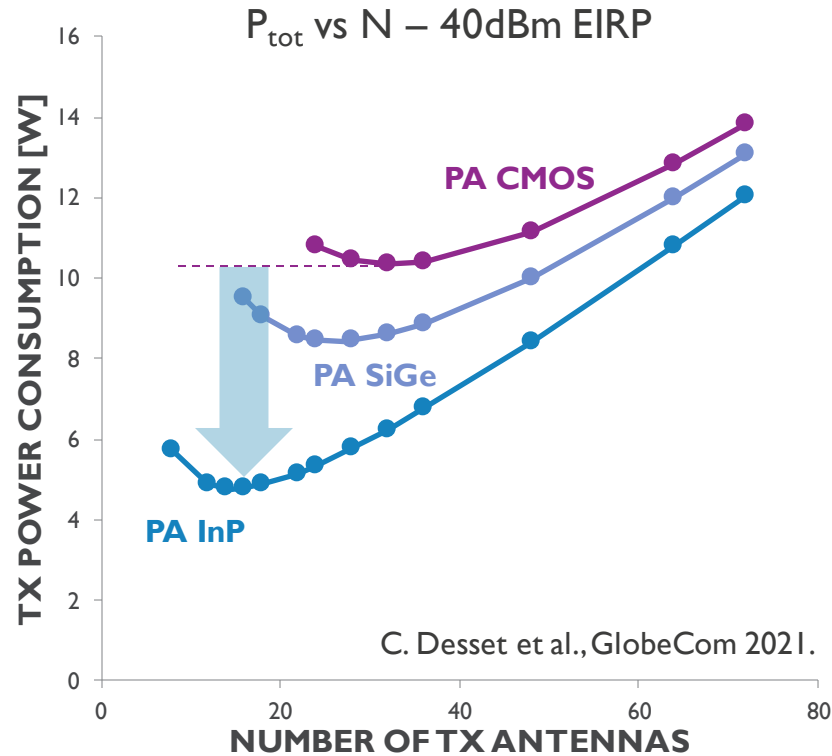
- + CMOS-compatible 200mm GaN-on-Si process
- + MOCVD growth of RF buffer and active layers (AlGaN, InAlN)
- + HEMT and MISHEMT devices with $L_g < 100\text{nm}$ and low resistive Ohmic contacts with $R_c < 0.15 \Omega \text{ mm}$
- + Advanced multi-layer Cu BEOL & integration of passives

Scaled GaN-Si devices come close to GaN-SiC performance

N. Collaert et al., accepted IEDM 2022.

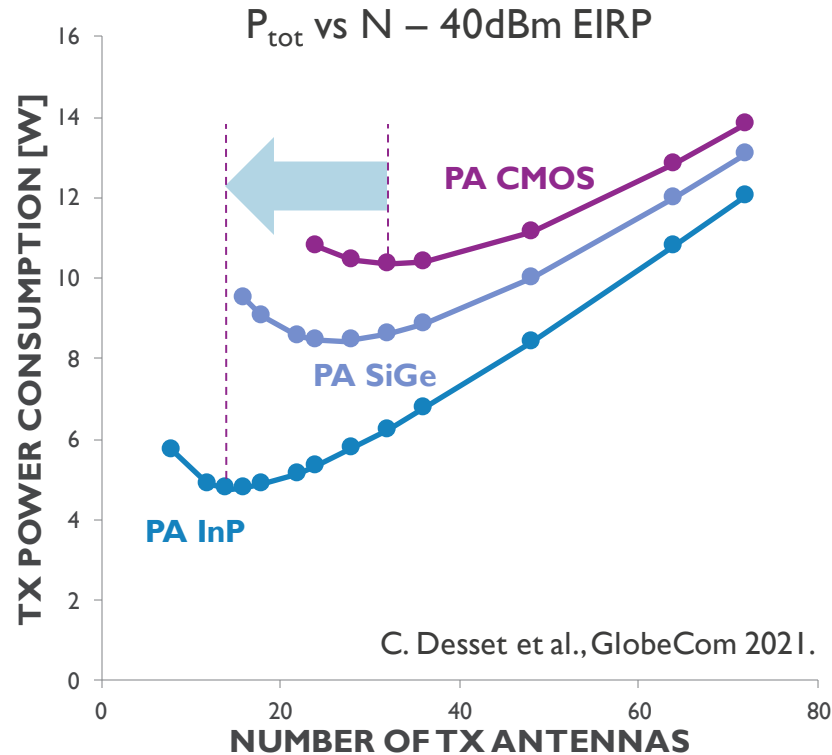


Power reduction possible with InP at 140GHz



2x lower power consumption

And footprint reduction possible with InP at 140GHz



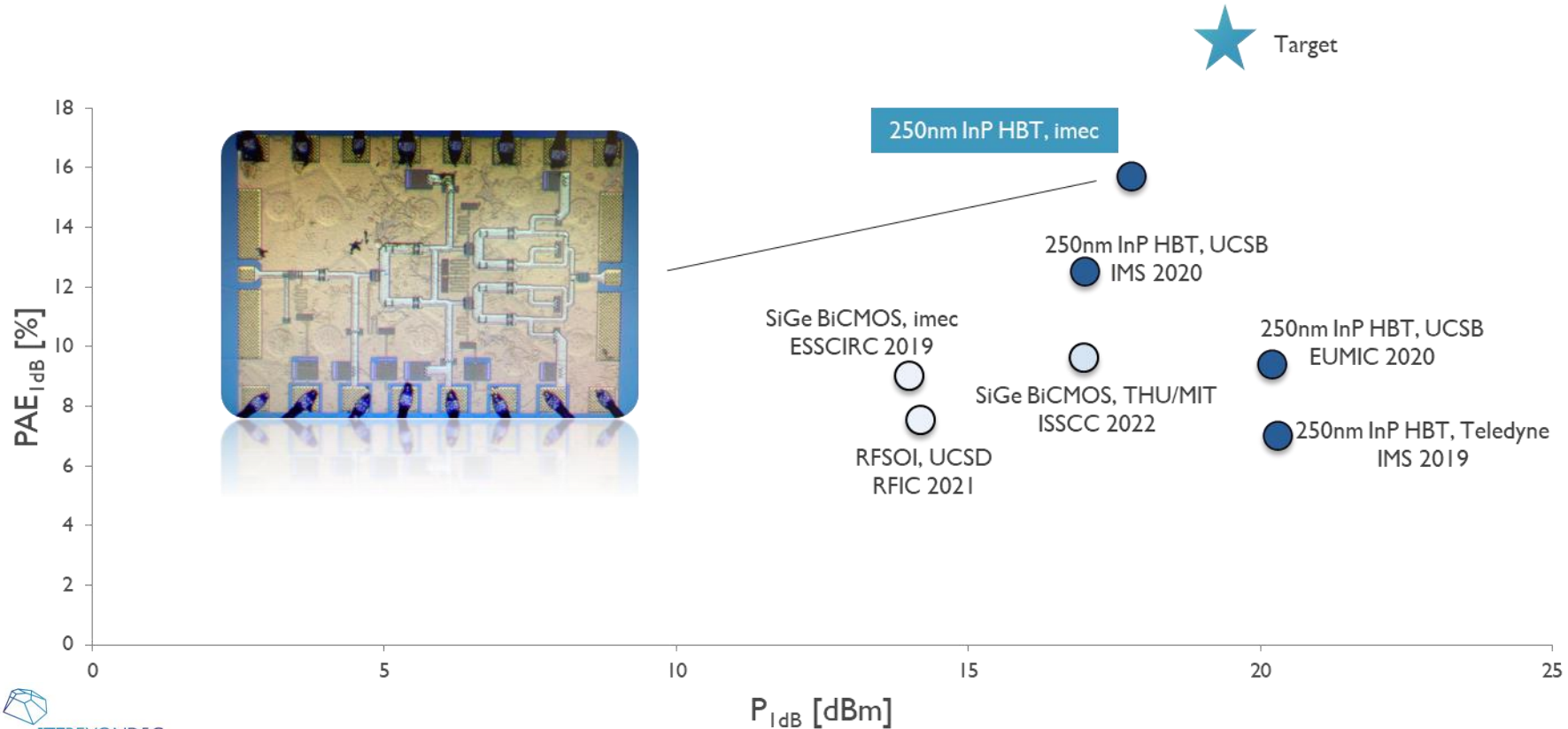
2x lower power consumption

2x smaller footprint

But requires:

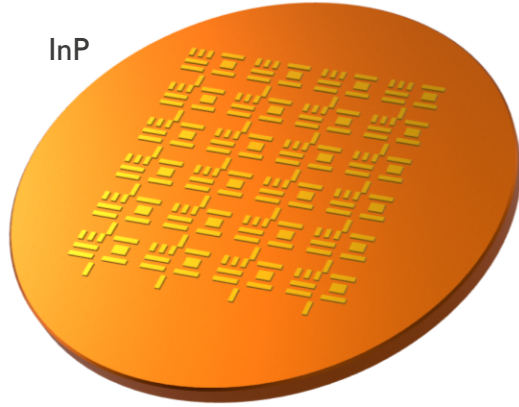
- + A mature and cost-efficient InP technology
- + Requires integration with CMOS

InP combines high output power and efficiency at 140GHz



There are different InP technologies

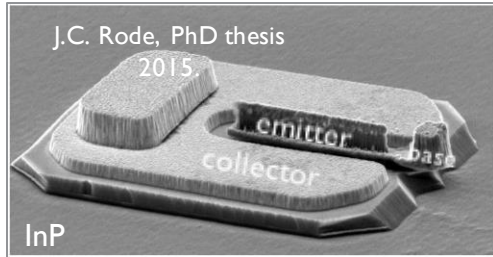
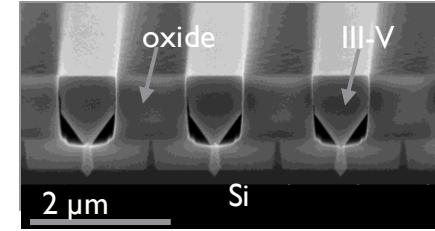
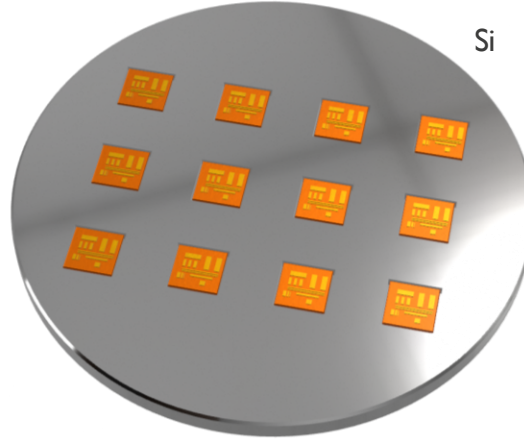
InP



InP substrates

Reconstructed wafers

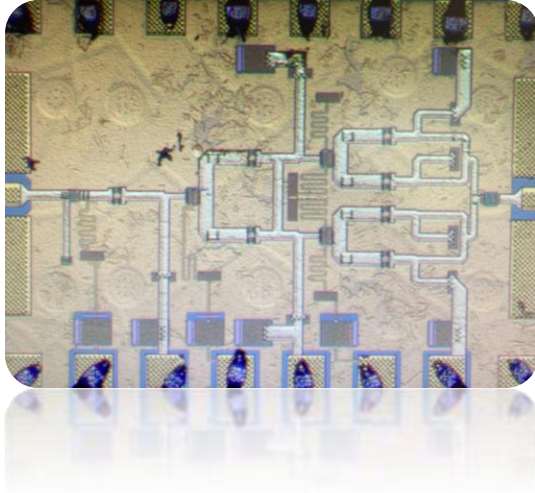
Si



**Hetero-epitaxy
(Nanoridges)**

But we need CMOS for beamforming, control, convertors ...

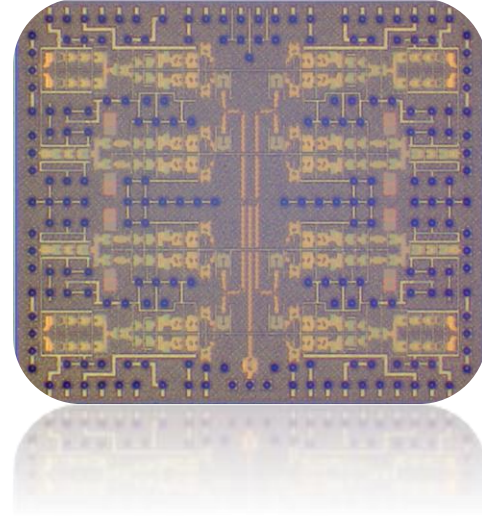
InP



High output power and efficiency
Gain bandwidth: 30GHz
Small footprint



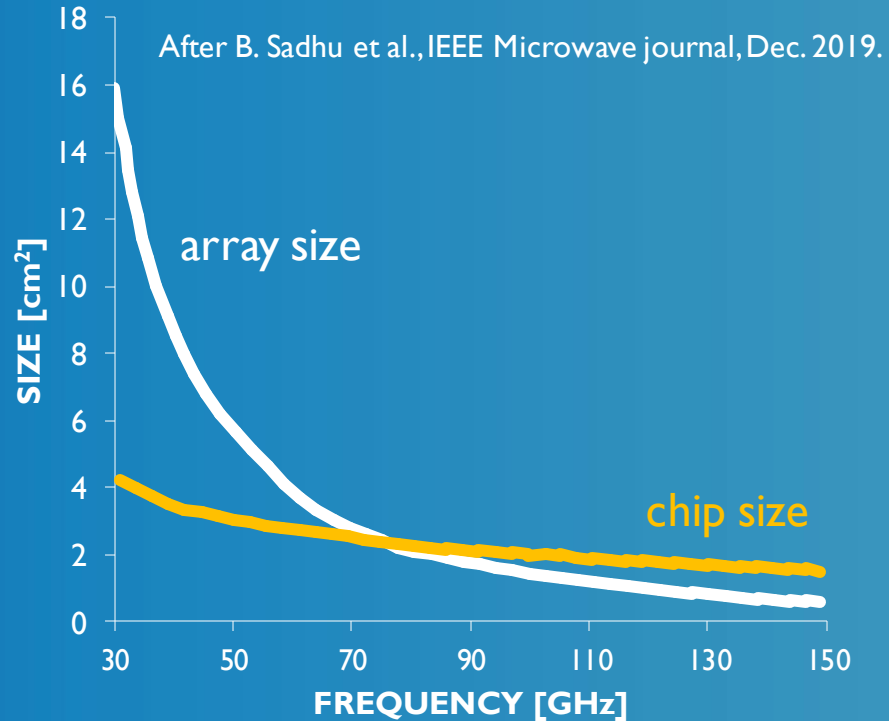
CMOS



Modular beamforming architecture
Joint communication & sensing
RF frequency range: 120-150GHz with
Multiple channels of > 4GHz

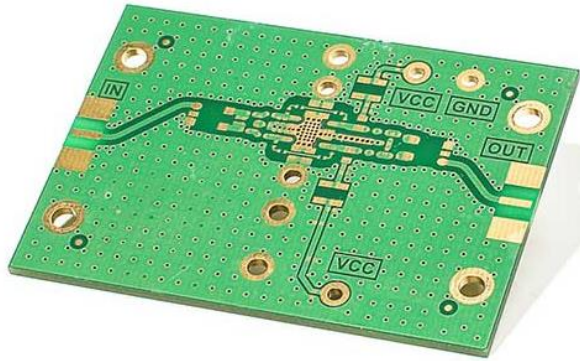
At freq. >90GHz packaging strategy challenged by antenna pitch

- + Phased array pitch limited to $\frac{\lambda}{2}$
 - + 1mm @ 150 GHz
- + Interconnect loss
 - + High metal and dielectric losses
- + Thermal density increases
 - + Dedicated thermal pathways needed

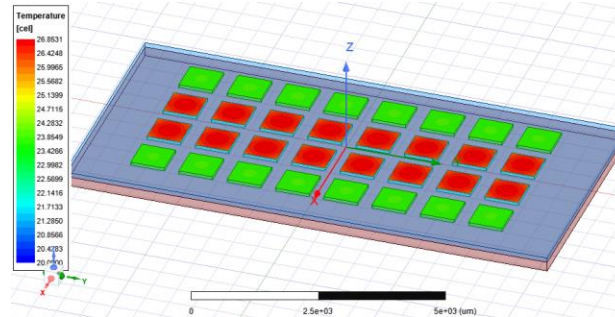
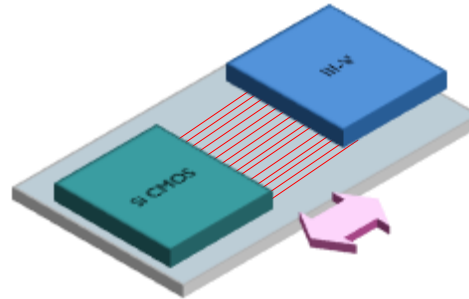


Heterogeneous integration comes in many forms

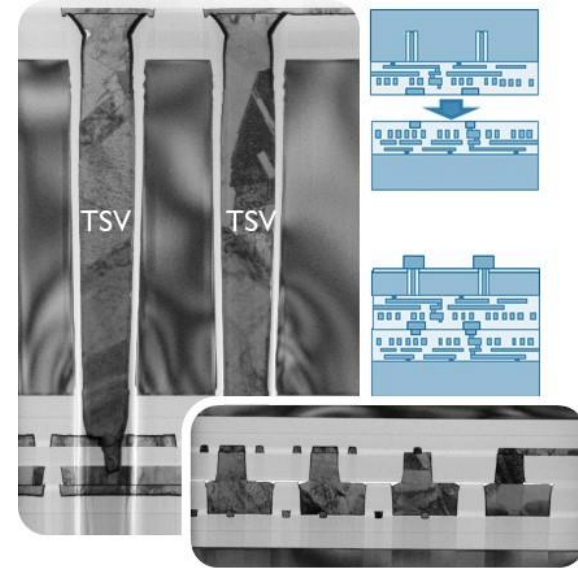
State-of-the-art PCB



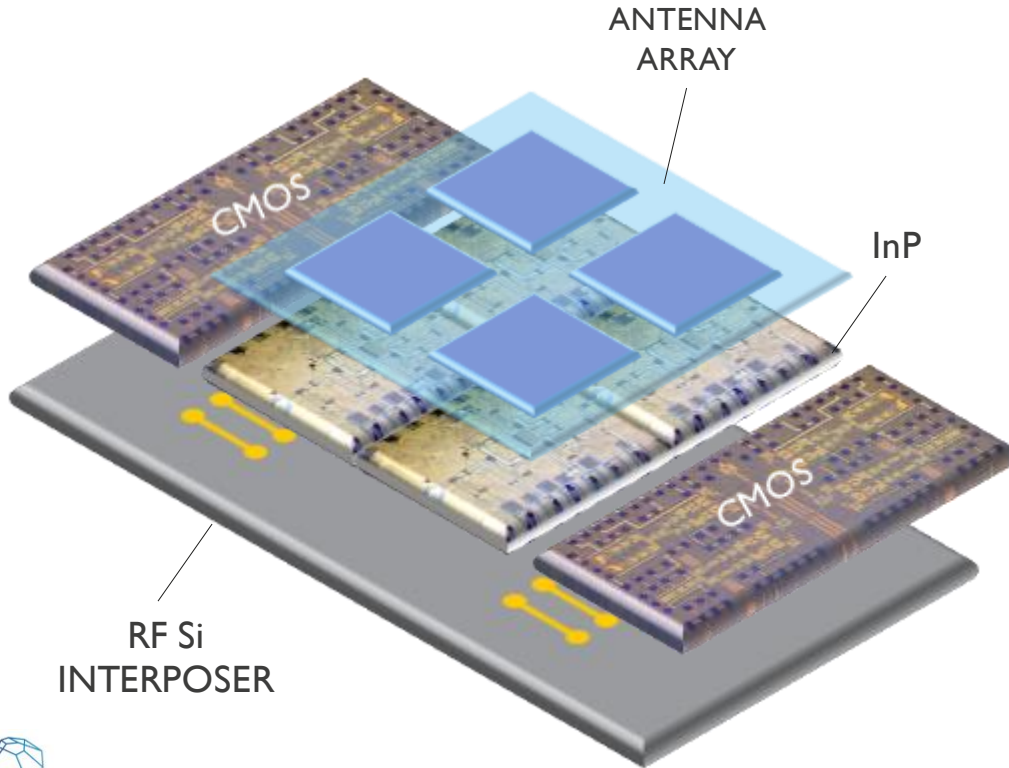
2.5D integration
RF-tailored interposer



Wafer-level 3D integration



RF interposer is a key enabler for heterogeneous integration

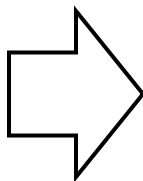
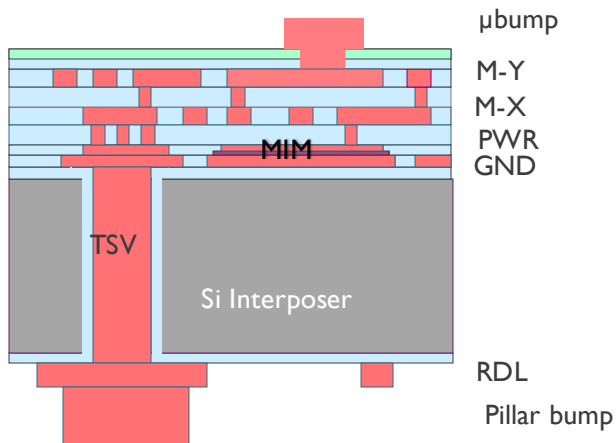


- + Low loss interconnects
- + Better thermal performance
- + Integration of passives
- + Antenna array in package

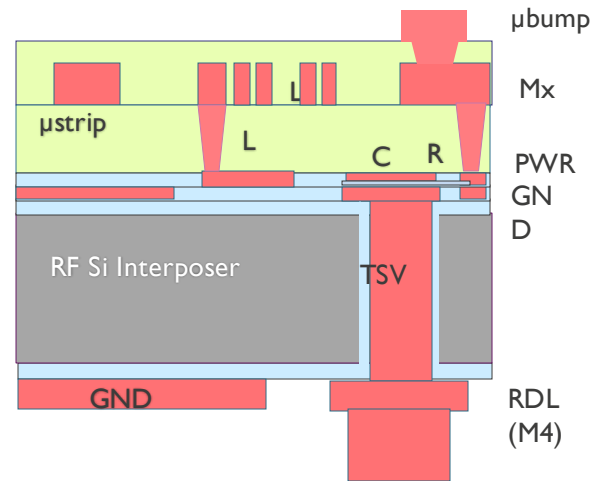
From digital interposer to RF-tailored Si interposer

X. Sun et al., ECTC 2022.

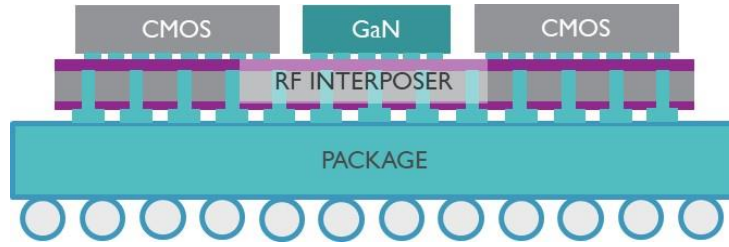
High speed digital interposer



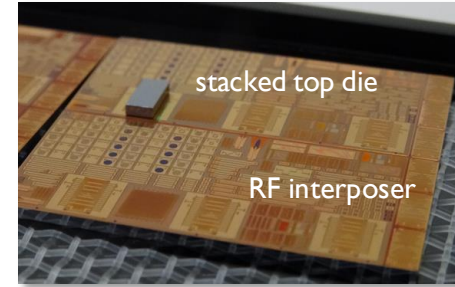
RF Si interposer



RF interposer enables scaled area with low loss

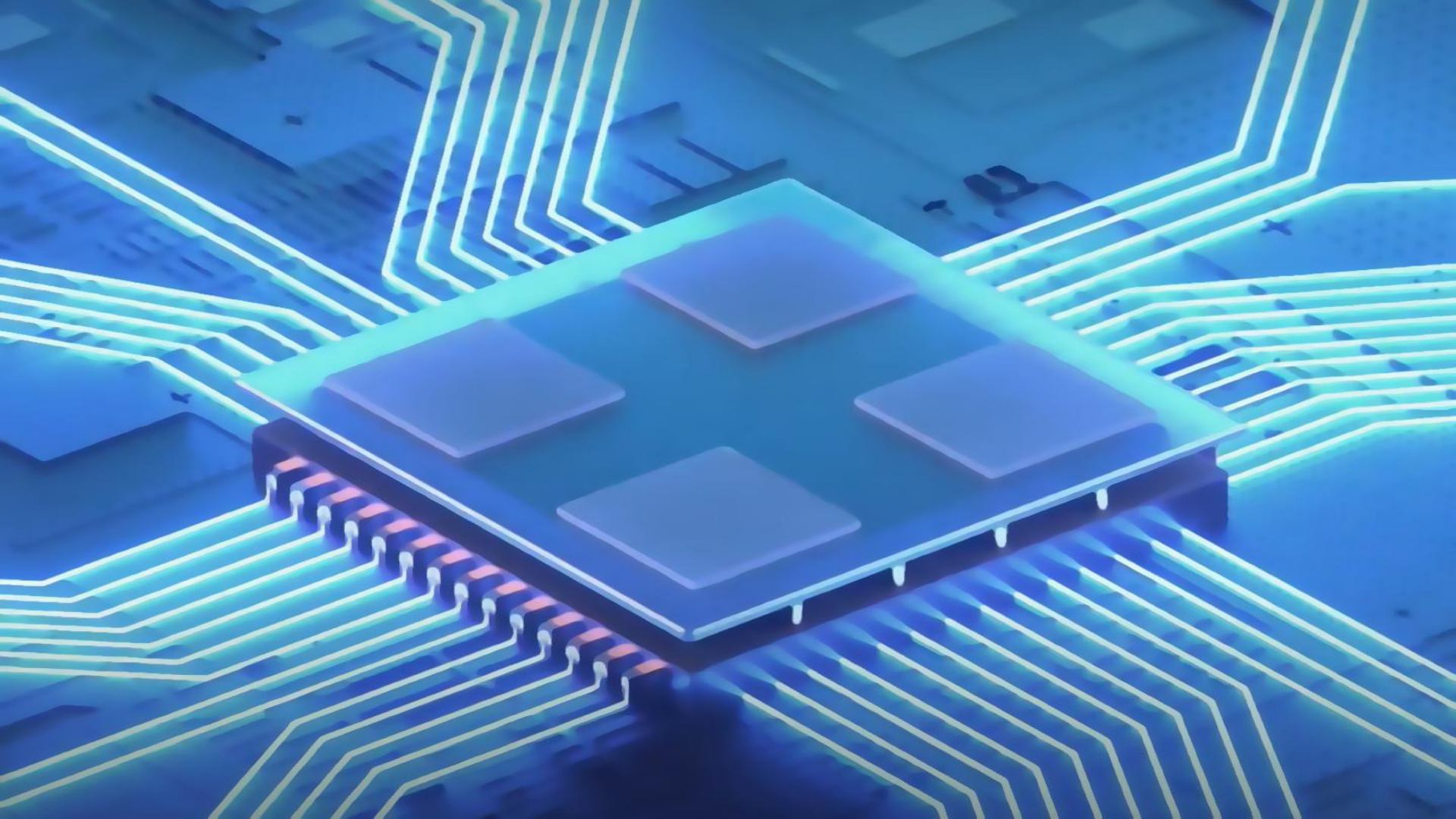


X. Sun et al., ECTC 2022.

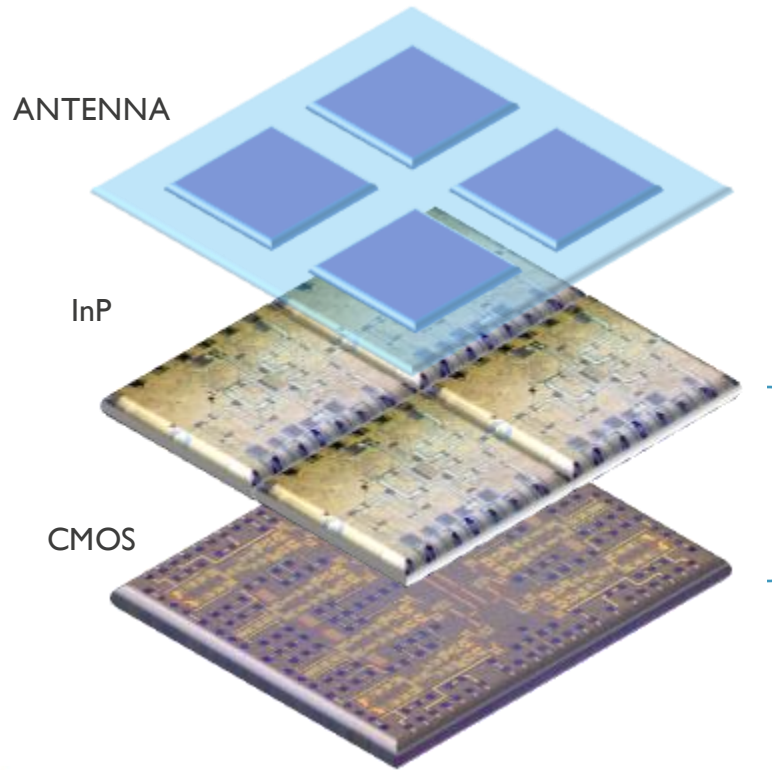


demonstration
with Si die

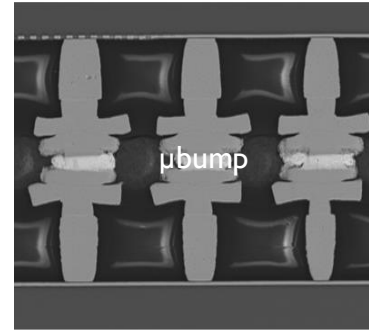
TECHNOLOGY / MATERIAL	HDI PCB	IC Substrate + mSAP	IMEC waferscale RF interposer
ROUTING LAYERS	6 - 8	4 - 8	2 - 4
TRACE / SPACE	50 μm / 50 μm	15 μm / 15 μm	5 μm / 5 μm
LAYER THICKNESS	50 - 250 μm	10 - 30 μm	5 - 20 μm
BUMP PITCH	200 μm	80 - 120 μm	20 - 40 μm
FLIP-CHIP FREQUENCY	170 GHz	300 GHz	500 GHz
FLIP-CHIP AREA	600 x 600 μm^2	300 x 300 μm^2	100 x 100 μm^2
FLIP-CHIP LOSS @ 150 GHz	1 dB	0.5 dB	0.2 dB
LINE LOSS @ 150 GHz	0.2 dB/mm	0.4 dB/mm	0.3 dB/mm



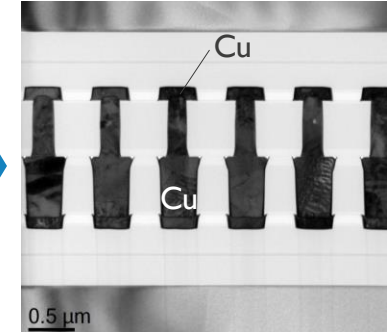
3D integration



Micro-bumping



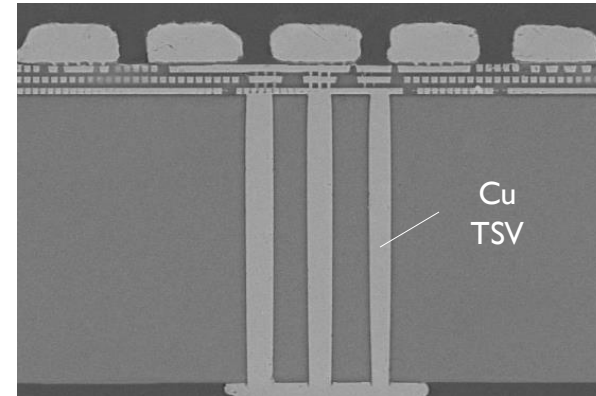
W2W hybrid bonding



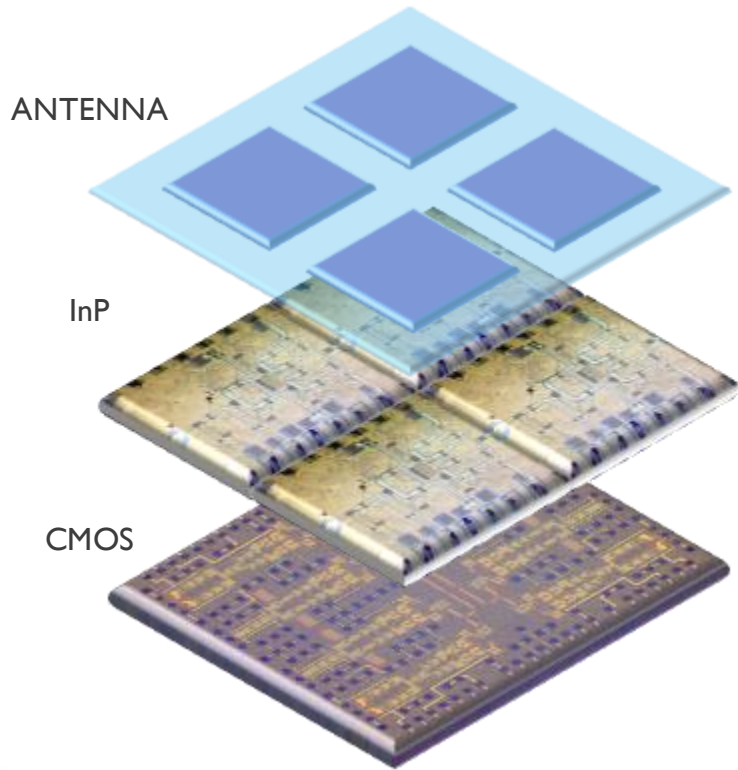
E. Beyne, ITF Japan 2022



TSVs and thermal vias



Towards a D-band Joint Communication & Sensing Demonstrator



Scalable Ultra High data-rate

Up to 40Gb/s



High energy efficiency

< 0.1 nJ/bit



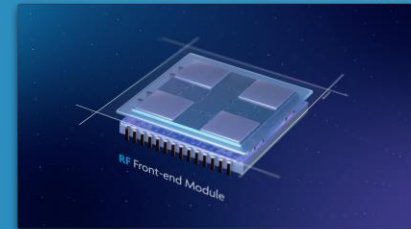
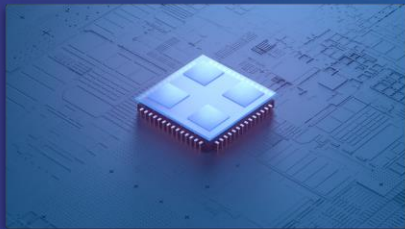
Extreme Sensing resolution

range < 2cm / angular < 5° / speed < 0.1 m/s



Small form factor

< 0.5cm²



The techno-economics of serving ever more traffic at cost drive us to **mmWave** and then **above 100 GHz**.

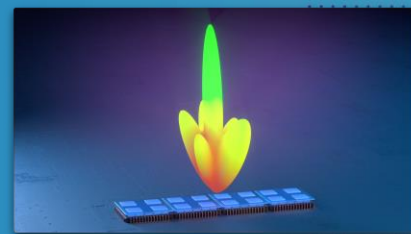
+ **Power and efficiency** limits for mmWave mobile devices can be avoided using **GaN**.

For systems above 100 GHz, **InP** reduces power consumption and size by **50%**.



We are on track to demonstrate these CMOS compatible, cost effective RF platforms **by 2025**.

... and not just for **communications**.





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Thank you

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