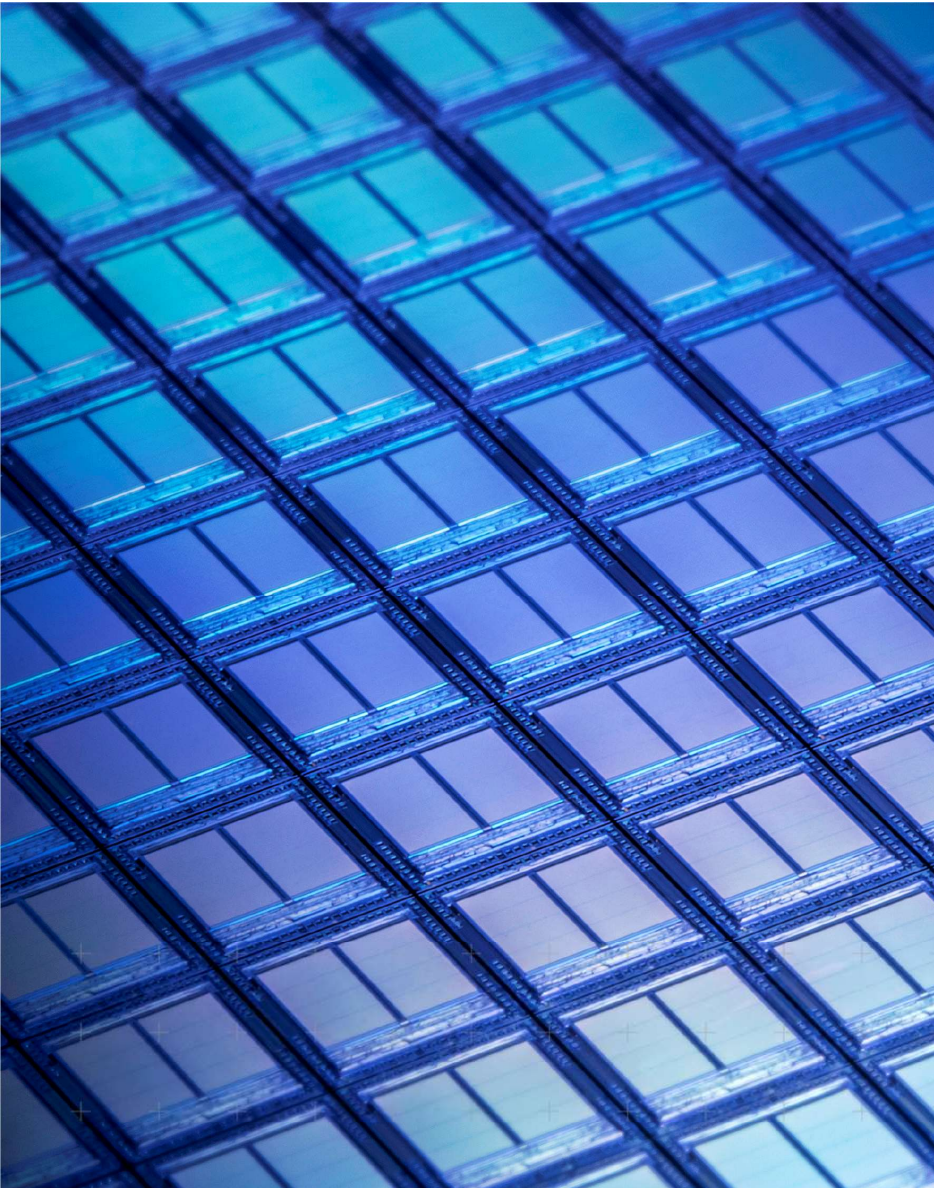




Plasma Etch & Deposition Processes for SiC Devices in Power Applications

Electrification & Power Semiconductors
SEMICON Europa 2022

SEMICON[®]
EUROPA

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16 November, 2022

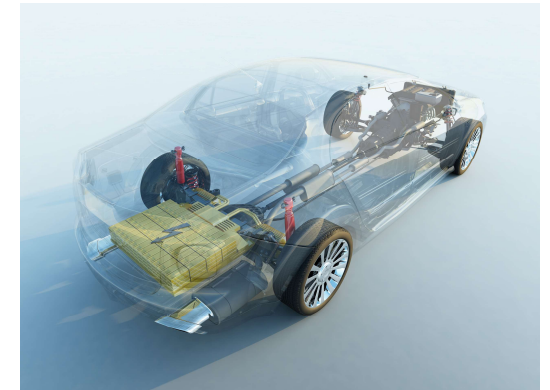
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Wind Turbines



Automotive / EV



Traction



SiC Power Device Markets

All data from

 Except where indicated

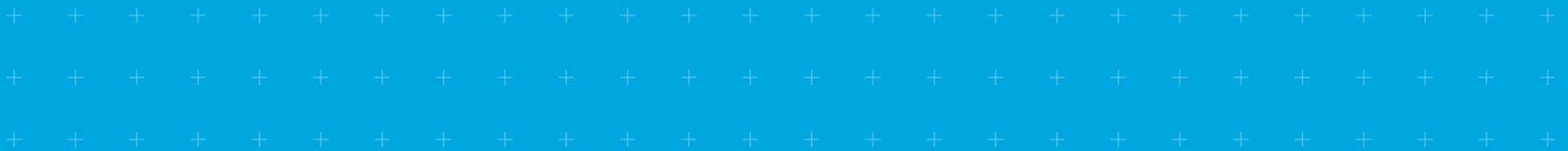
- SiC power devices markets will reach \$6.3B by 2027
- 34% CAGR from 2021 – 2027
- EV SiC power device market alone forecast to grow from
 - \$685M in 2021 to ~\$5B in 2027
- Voltage range 650V (EV, solar inverters) to several kV (rail & wind turbines)
- Wafer size: 4" or 6" → 8"

Property	Si	GaAs	6H-SiC	4H-SiC	GaN	Diamond
Bandgap, E_g (eV)	1.12	1.43	3.03	3.26	3.45	5.45
Dielectric constant, ϵ_r^a	11.9	13.1	9.66	10.1	9	5.5
Electric breakdown field, E_c (kV/cm)	300	400	2,500	2,200	2,000	10,000
Electron mobility, μ_n (cm ² /V·s)	1,500	8,500	500 80	1,000	1,250	2,200
Hole mobility, μ_p (cm ² /V·s)	600	400	101	115	850	850
Thermal conductivity, λ (W/cm·K)	1.5	0.46	4.9	4.9	1.3	22
Saturated electron drift velocity, v_{sat} ($\times 10^7$ cm/s)	1	1	2	2	2.2	2.7

Source: US Dept of Energy Report 'ORNL/TM-2003/257'

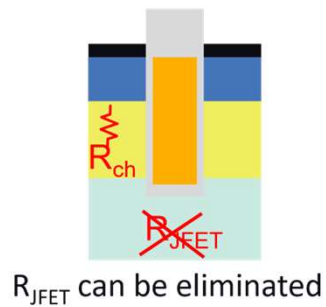
Etch & PVD solutions required to keep up with growing market demands

Etch Applications

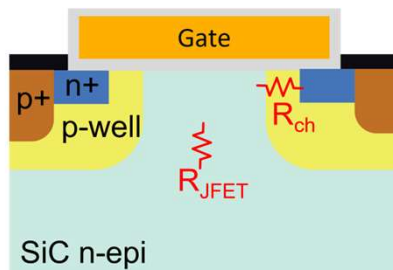


SiC Trench Etch Process Flow

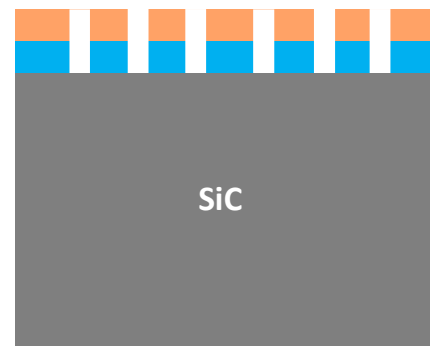
SiC Trench MOSFET



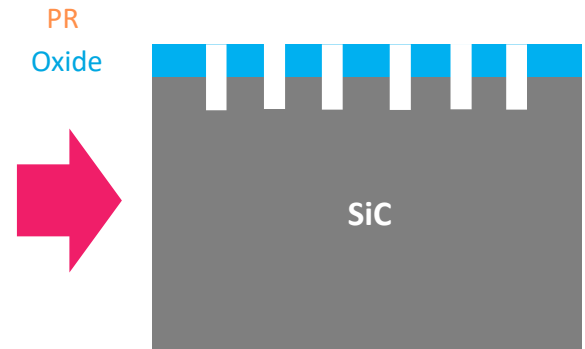
SiC Planar MOSFET



1 Oxide Hard Mask Open

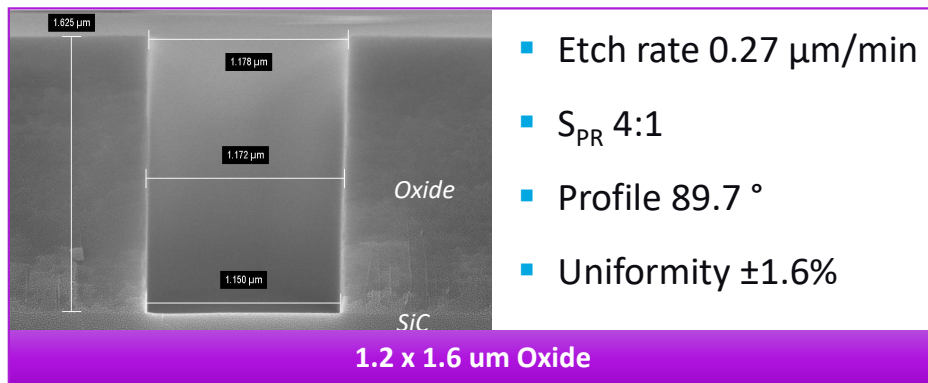
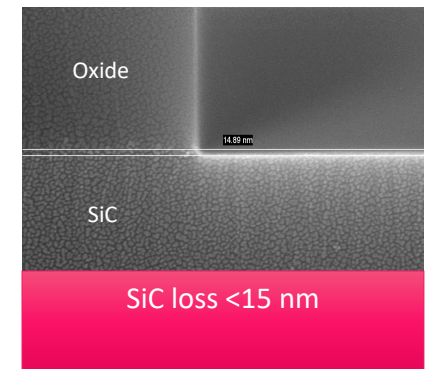
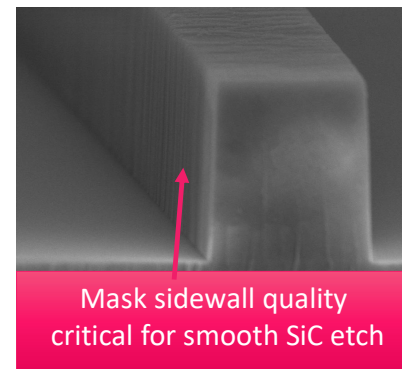
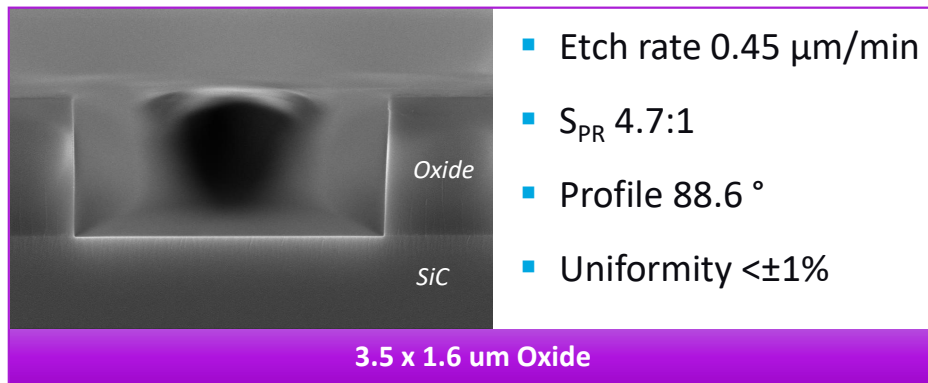


2 Shallow SiC Trench Etch

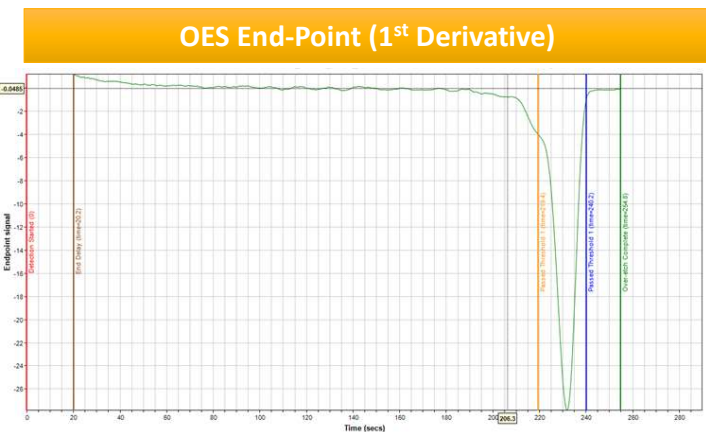


HMO & SiC etch performed
on SPTS Synapse™ module

1. Oxide Hard Mask Open on SiC Wafer

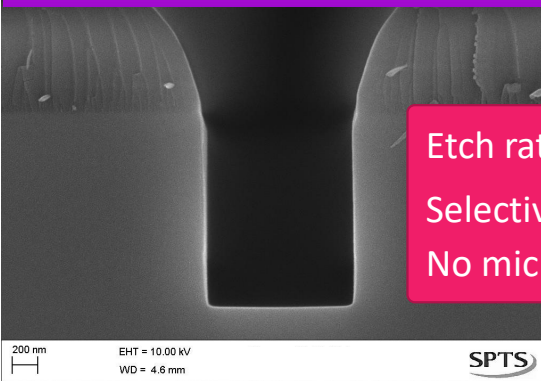


Apparent 'tilt' due to SEM



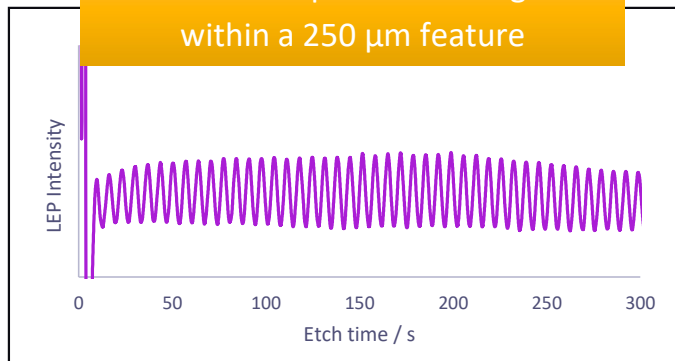
2. SiC Trench Formation

Flat Base



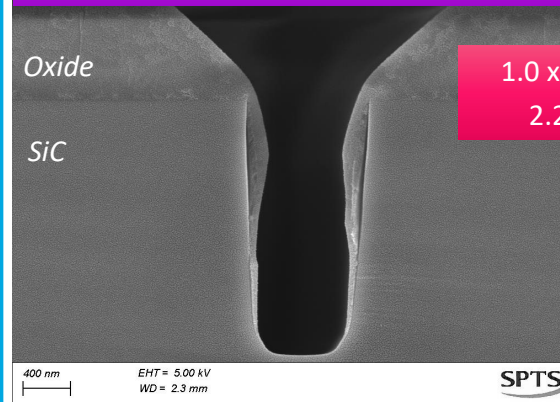
Etch rate 0.3-0.9 $\mu\text{m}/\text{min}$
Selectivity to oxide $\sim 2\text{-}3\text{:}1$
No micro-trenching

LASER depth monitoring
within a 250 μm feature



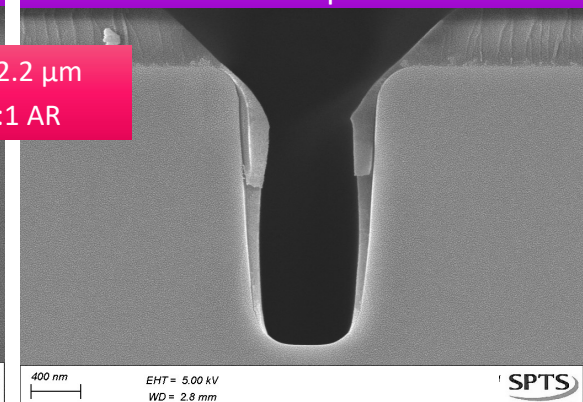
Rounded bases for next-generation devices
Improves gate oxide quality & prevents high electric fields
→ higher operating voltage

Rounded Base



1.0 x 2.2 μm
2.2:1 AR

Rounded Top & Base

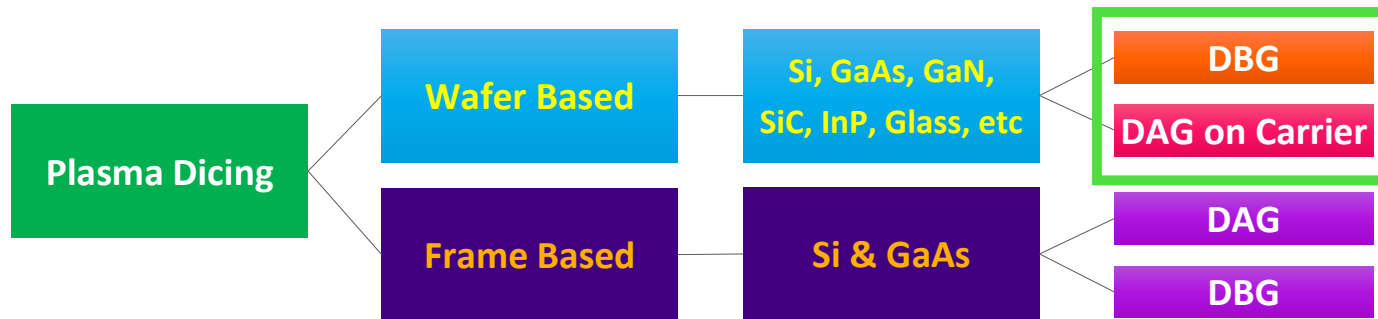


- Novel Etch/passivation chemistry IP in progress...
 - Passivation removed post-etch with HF
- Etch rate 0.33-0.5 $\mu\text{m}/\text{min}$ $S_{\text{Oxide}} > 2\text{:}1$
- 10-16 WPH @ 1x1 μm CD, depending on process required

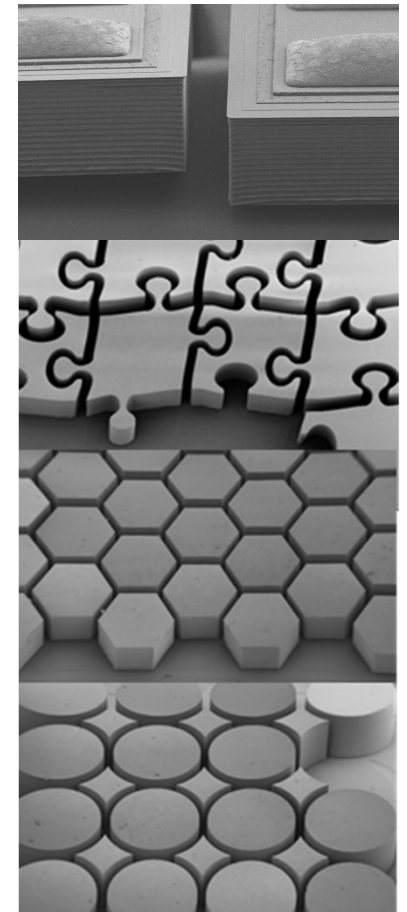
Plasma Dicing



Plasma Dicing Overview



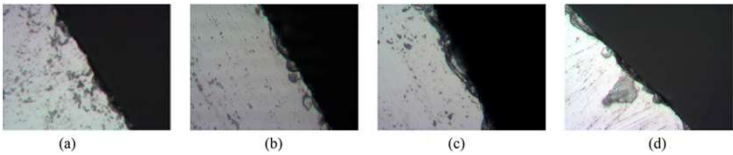
- **SiC Plasma dicing performed on SPTS Synapse™ module**
 - Dice Before Grind (DBG) or Dice After Grind (DAG) on carrier wafer
 - Framed based approach is not a feasible option
- **Integration is key**
 - Patterning, mounting, post-etch...



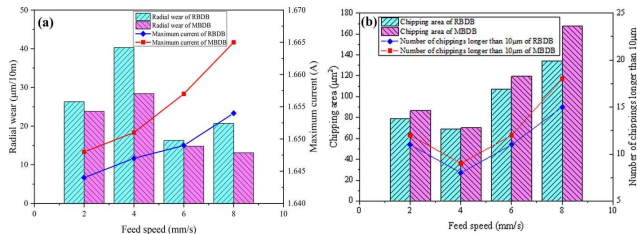
SiC Plasma Dicing Vs Blade Dicing

SiC Blade Dicing

Chipping after blade dicing
50 μm to 200 μm depth



Chipping area increases as
blade feed speed is increased

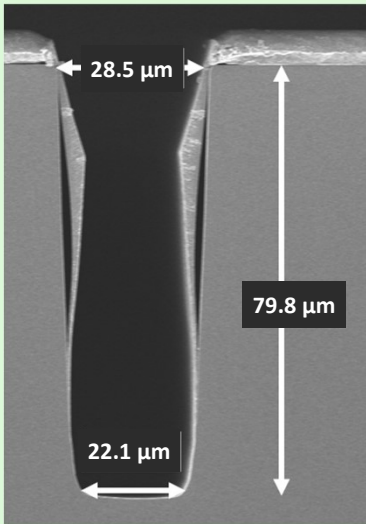


Slower throughput compared to plasma dicing:

Blade Dicing	Plasma Dicing
2 – 3 hours	~40 mins

Die Size >10mm²

SiC Plasma Dicing

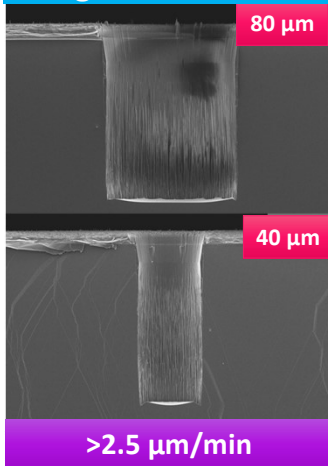


Characteristics	Result
Etch rate (μm/min)	2.1
Uniformity (±%)	5
Profile Angle (°)	~88
Selectivity to Ni	~20:1
T'put (100 μm)	>1 wph

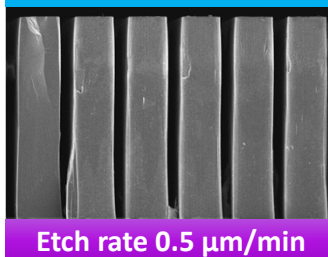
Benefits

- ✓ Higher Die-Break Strength
- ✓ Increased Throughput
- ✓ Increased Yields
- ✓ Lower CoO

High Rate SiC Via



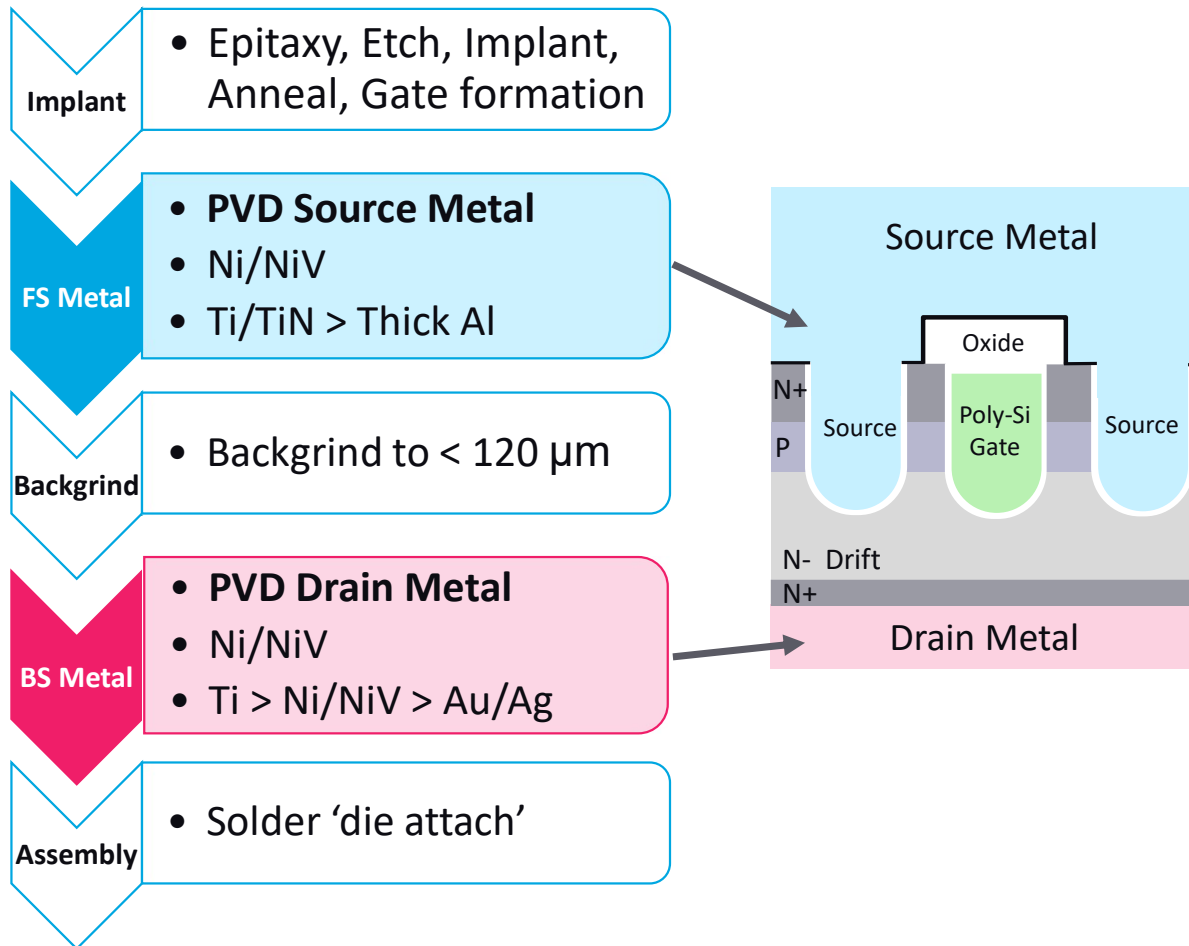
20:1 HAR SiC MEMs



PVD Applications



PVD Applications for SiC Power



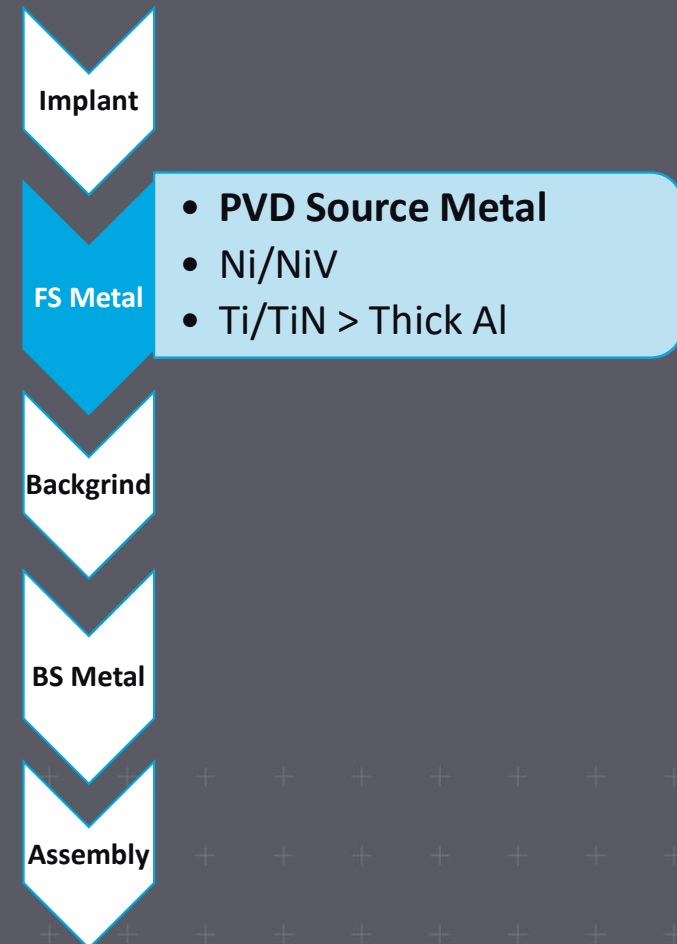
Frontside Metal

- ~350 μm SiC thickness
- **Ni/NiV** – Ohmic contact
- **Ti/TiN** – Barrier
- **Thick Al** – (3-5 μm) gate/source contact

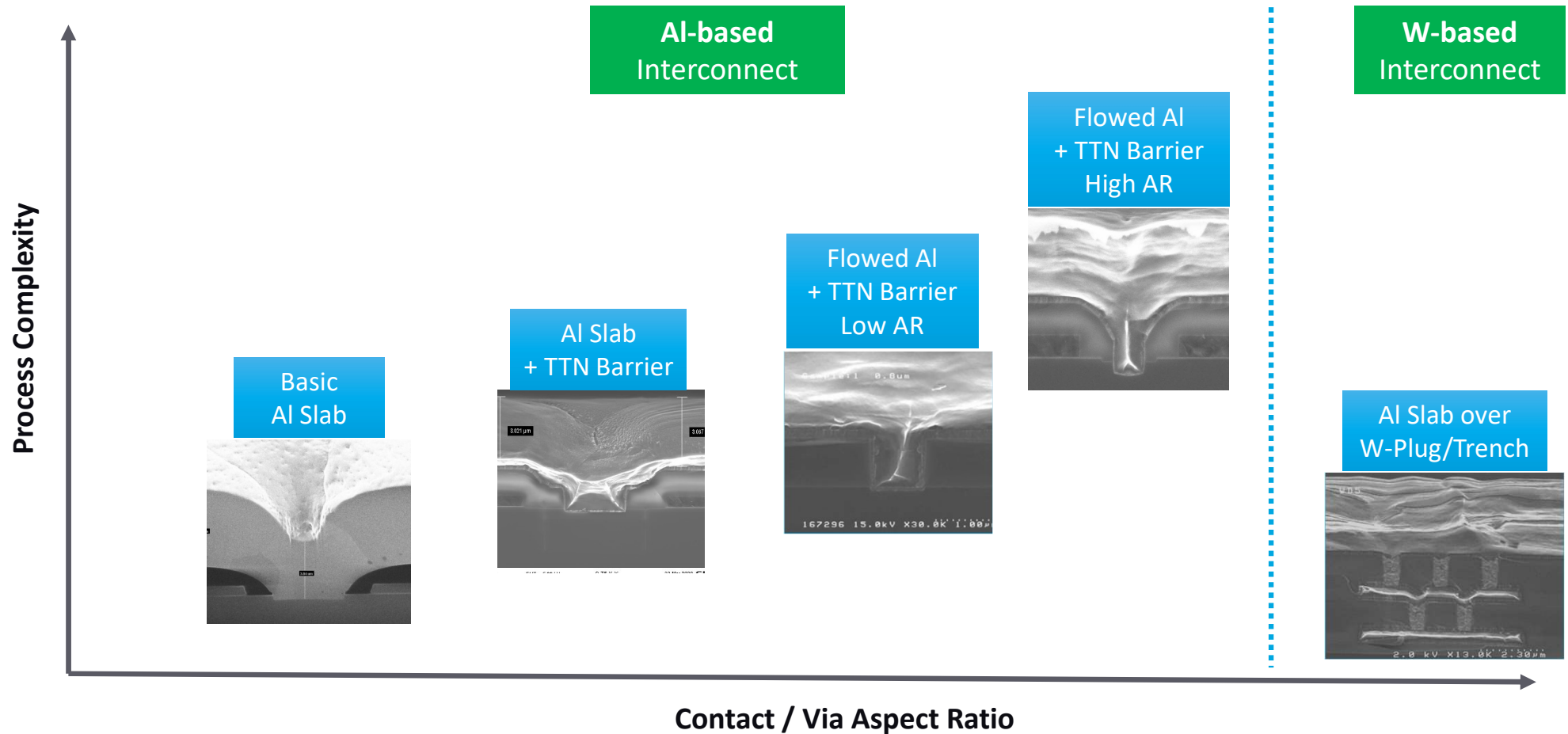
Backside Metal

- Thinned SiC ~ 120 μm
- **Ni/NiV** – Ohmic contact
- **Ti** – Adhesion
- **Ni/NiV** – Inter-metallic, low stress
- **Au/Ag** – Passivation

PVD Frontside Metal



FS Metal – Ti/TiN > Thick Al Metallisation



FS Metal – Thick Al Requirements

Low extrusions

- No contamination
- Controlled deposition temp
- Specialised chamber/shield design

Low CoO

- High throughput
- Long target life
- Shielding = Target life
- No costly ESC, no clamps; faster PM's

Industry Requirement:
Defect Free, High T'put



SPTS Sigma®: 4 µm Al Deposition

Experience up to 20 µm

Reported Issues:
Defects, Low T'put



Other PVD tool result

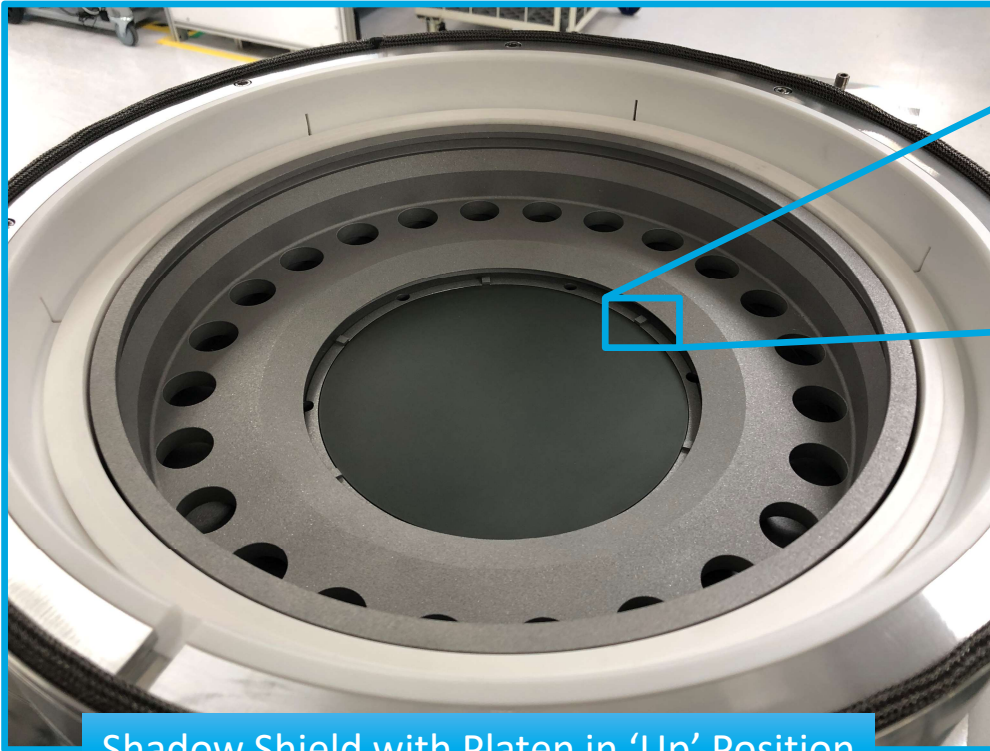
	Al Dep rate	T'put	Defects?
Other PVD Tool	0.6 µm/min	~ 15	Yes
SPTS Sigma®	1.4 µm/min	> 30	No

PVD Backside Metal



- **PVD Drain Metal**
- Ni/NiV
- Ti > Ni/NiV > Au/Ag

Backside Processing – Die Protection, Overspill Prevention



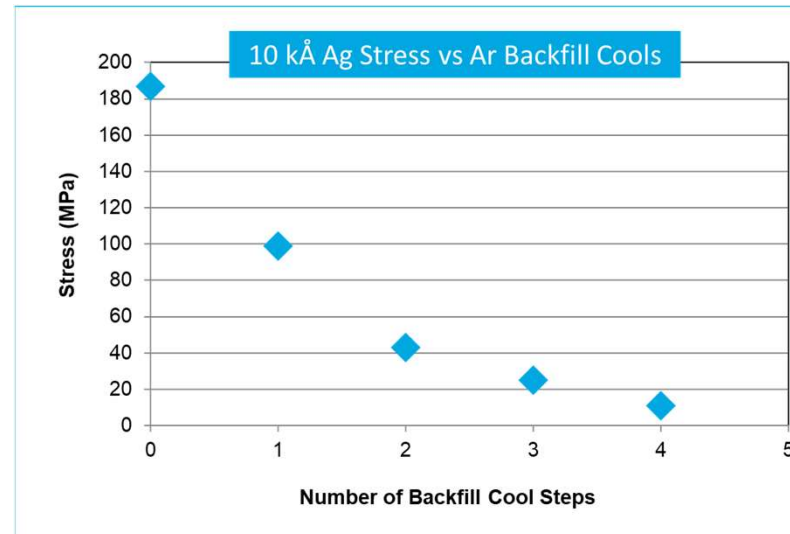
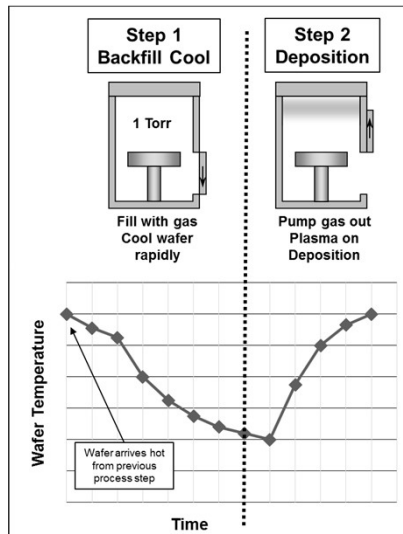
Shadow Shield with Platen in 'Up' Position



Edge Contact Support

- **Shadow Shield** prevents BSM overspill
- **Edge Contact** end effector & lift pins prevent handling damage to active die

Managing SiC Stress, Warpage & Film Adhesion



- SPTS Sigma® uses “Backfill” cools & UCP to manage wafer temperature and subsequent stress/adhesion
- Effective temperature & stress control minimises:
 - Adhesion issues, wafer breakages
 - Localised die stress, yield loss

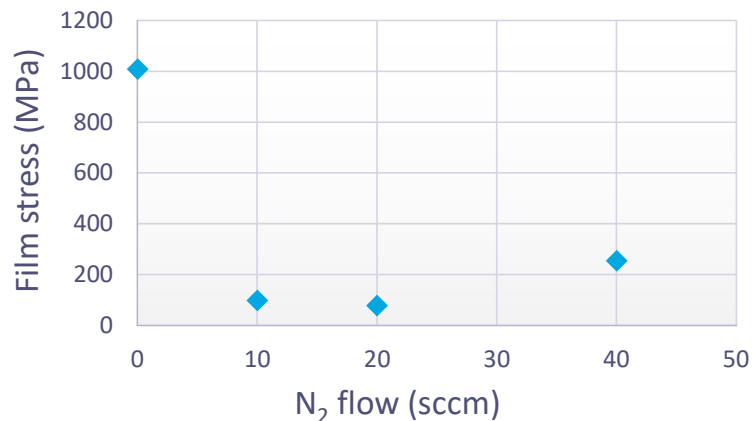
Stress Control: Ni & NiV

- Higher solder reflow temperatures require much thicker NiV
- KLA's SPTS PVD systems offer advanced stress control techniques:

N₂ Addition for NiV

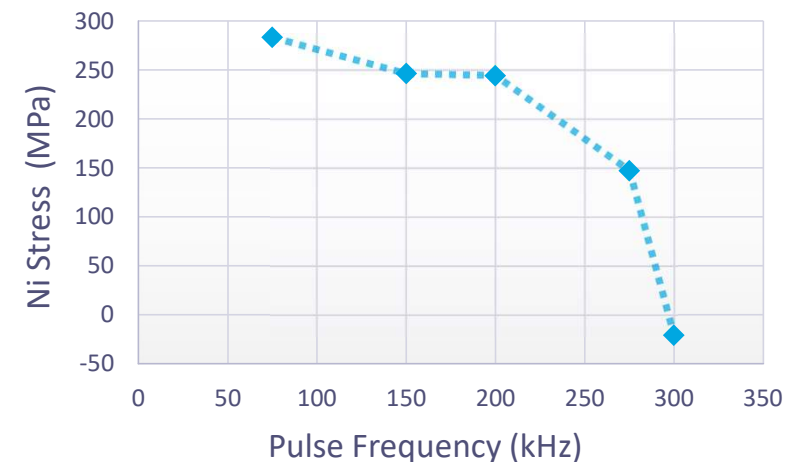
N₂ physically incorporated into NiV lattice

Not reacting - Forces lattice out, into compression



N₂ addition reduces stress by a factor of 10

Pulsed DC for Ni/NiV



↑ pulse *f* makes layer more compressive

Summary

- SiC power device market growing rapidly
 - Etch and PVD solutions provided by KLA
- SiC power MOSFET trench formation on Synapse™
 - Hard mask open with smooth sidewalls
 - Trench etch with rounded top & base
- Plasma dicing solution for SiC on carrier wafers
- Frontside & backside PVD solutions on Sigma™
 - Thick Al deposition with lowest CoO and lowest extrusions
 - 'Edge Contact' handling prevents damage to SiC active face
 - Multiple parameters to manage stress/adhesion

Thank you

