

Complex, Small, Cheap: How Packaging is Going to Power the Digital Age

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Agenda

1. Overview on Chiplet Packaging
2. Chiplet Packaging Opportunities & Challenges
3. JCET Group Chiplet Packaging Platform & Solutions

Semiconductor Market Applications Are Experiencing

New Applications

Individual Experience

- Metaverse, AR/VR
- Cloud feeling
- Autonomous driving
- Artificial intelligence

Collective Enhancement

- Ubiquitous computing
- Smart cities
- Smart finance, crypto
- Vehicle to anything
- ...

New Requirements

Complex System Architectures

- Multi-core architectures
- High-bandwidth memories
- Extensive use of non-logic IPs

Uncompromised Performance

- High data-rate (Gbps)
- Bandwidth (GHz)
- Low-latency (us)
- Power efficiency (pJ/bit)
- Routing density (wires/mm/layer)
- IO density (pads/mm²)

New Barriers

Larger System-on-Chip (SoC)

- Fab reticle < 800mm²
- Low yield, Edge die waste
- Long development time
- No one-node fit all

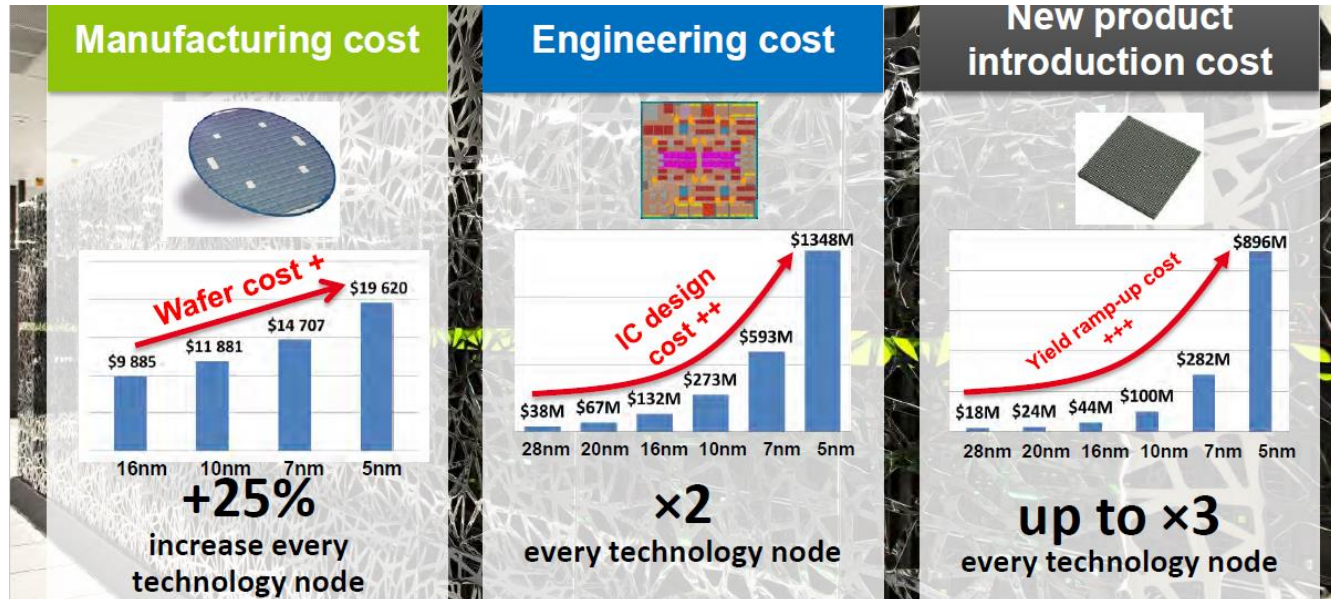
Advanced Node Scaling

- High development cost
- High wafer cost
- Unfit transistor cost model
- Diminishing return in scaling non-logic cores

New technology barriers in More-than-Moore's-Law Era warrant a new Chiplet-packaging ecosystem

Chiplets Motivation : Cost Trend with Si Node

- Si node technology in IC scaling is becoming too expensive.
- Associated yield can be problematic, and further affecting effective cost



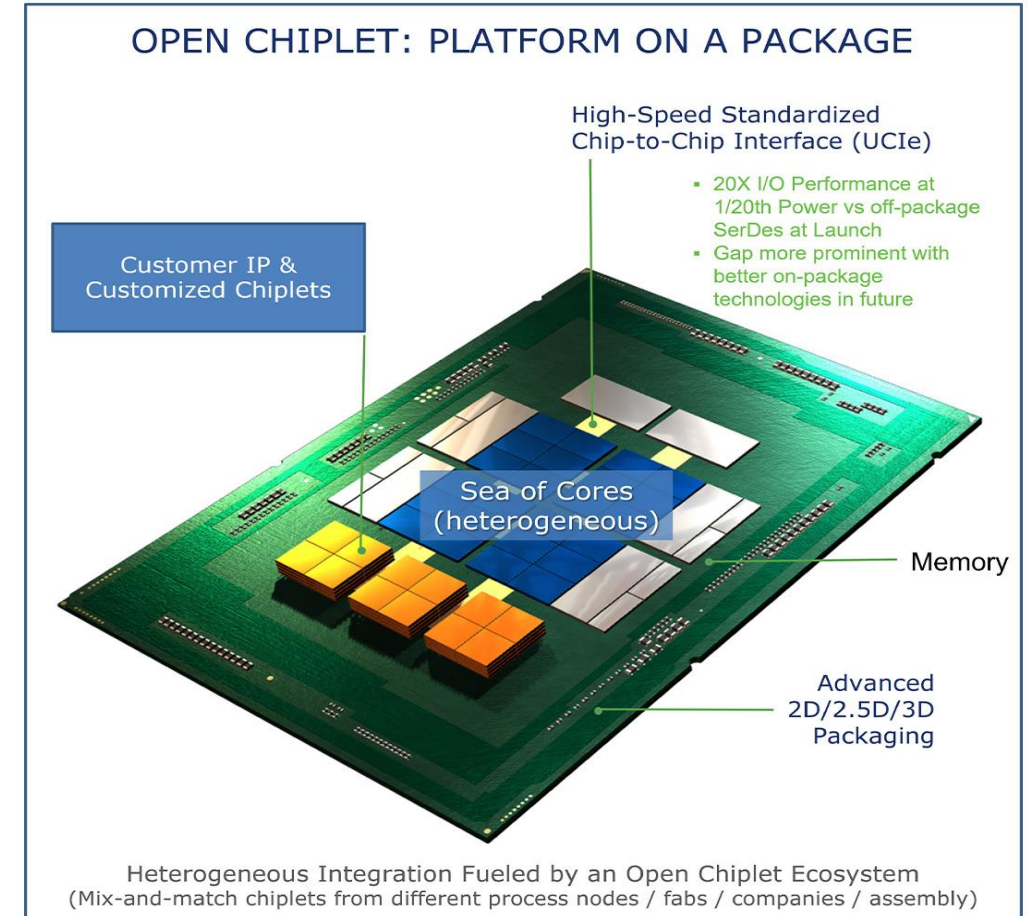
Source: Leti



Source: HIR

Top Challenges of Heterogeneous Packaging

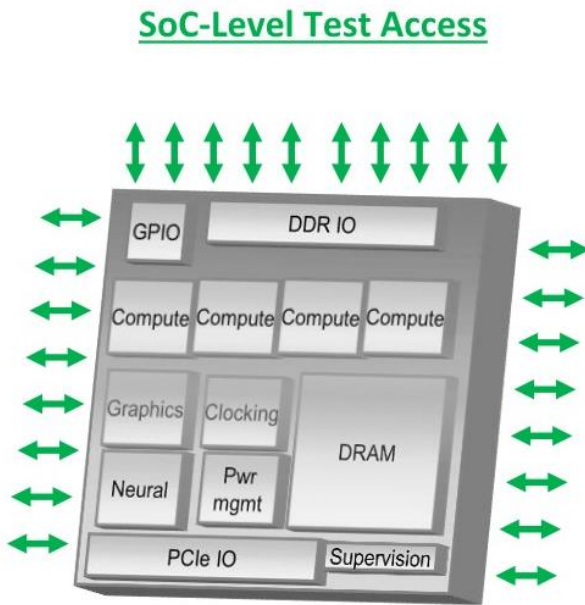
- **Design & Test** challenges in packaging assembly, interconnection, thermal management...
- **Collaboration** challenges among IDMs, Foundries, OSATs, Mat. & Equ. Providers, IP Providers, OEMs...
- **Standardization** challenges due to IP barriers, many different standard bodies/interest groups such as:
 - eXtremely ShoRt distance (XSR)
 - Ultra-ShoRt distance (USR)
 - Bunch-of-Wires (BoW)
 - Advanced Interface Bus (AIB 2.0)
 - Open Domain-Specific Architecture (ODSA)
 - Compute eXpress Link (CXL)
 - IEEE Heterogeneous Integration Roadmap (HIR)



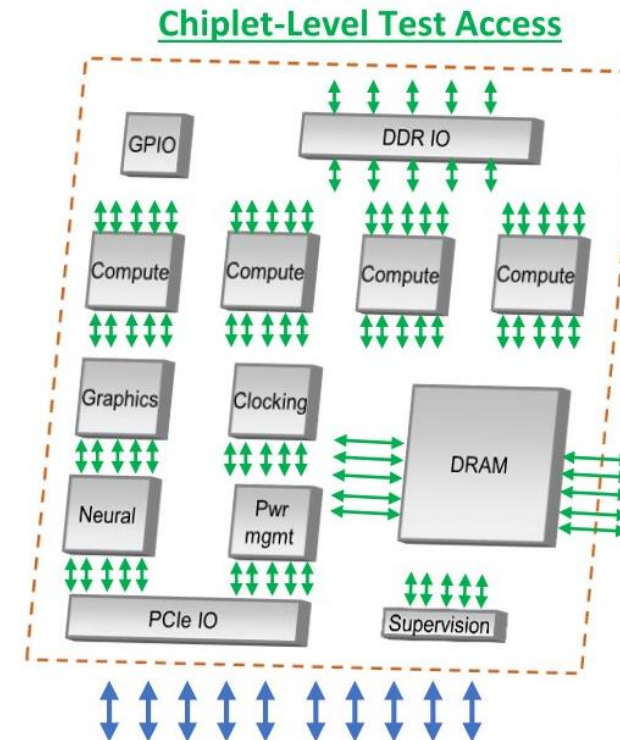
Source: UCIe

Top Challenges of Heterogeneous Packaging – Design & Test

- **Going way beyond functional requirements:** A practical chiplet package design must be verified thoroughly in terms of electromagnetic, thermal, signal/power (integrity), warpage, and other mechanical stresses. This is driving a significant upgrade to the entire EDA workflow.
- **Built-in Self-Test (BiST)** has been essential to SoCs. The same necessity is required for Chiplets.
- **Optimal Packaging Design :** Interconnections between functional chips should be optimized for best performance

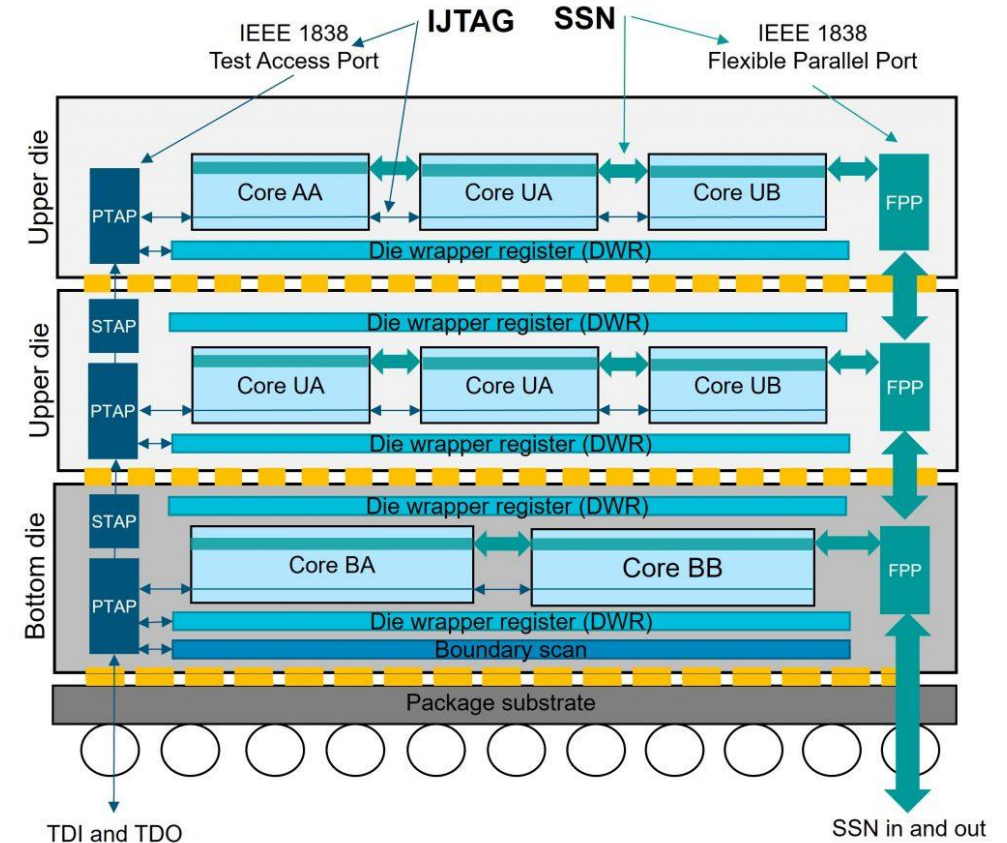


Source: IEEE EPS



Top Challenges of Heterogeneous Packaging – Device Maker Considerations

- **IP and Technology Partitioning** methods will be quite different, from one design to another.
- **Modular, Reusable IP Blocks** need to be compatible with existing and emerging industry standards.
- **Known-Good-Die (KGD)** test qualification becomes a challenge given the new Chiplet ecosystem.
- **Design for Test(DFT) Integration** on the Chiplet level is challenging due to the demand for novel DFT architectures.



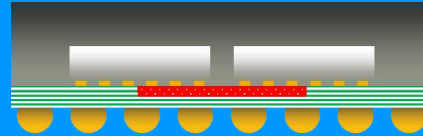
DFT Architecture for 3D Chiplet Packaging (Source: Siemens EDA)

Heterogeneous Packaging Solutions

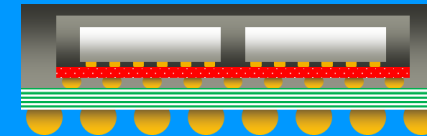
OSAT Model

RDL first interposer
OSAT capable
Mid-high applications

UHD RDL Bridge



UHD Fan-Out 2.5D



Lower cost compared to Silicon interposer with TSVs
Medium-to-high bump density and I/O count – e.g. JCET XDFOI™

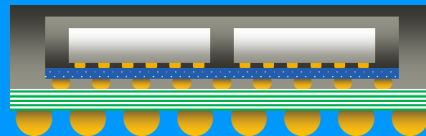
μ -bump pitch 20-55 μ m, L/S ~2 μ m
RDL size < 2000mm²

Hybrid bonding
without TSVs
C2W F2F/F2B

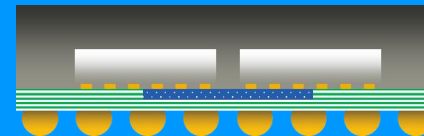
OSAT + Foundry Model

TSV interposer
Si Bridge
Foundry capable
high applications
Assembly & Test
OSAT capable

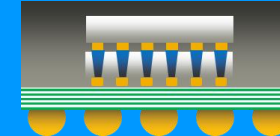
TSV Interposer



Silicon Bridge



3D Stack

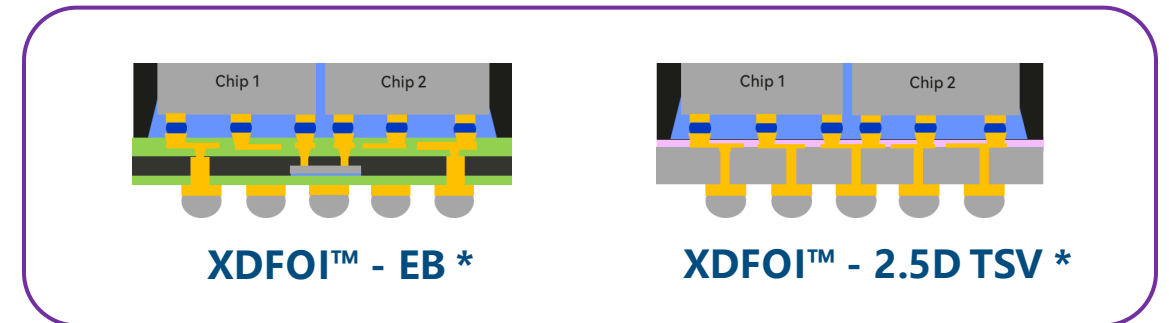
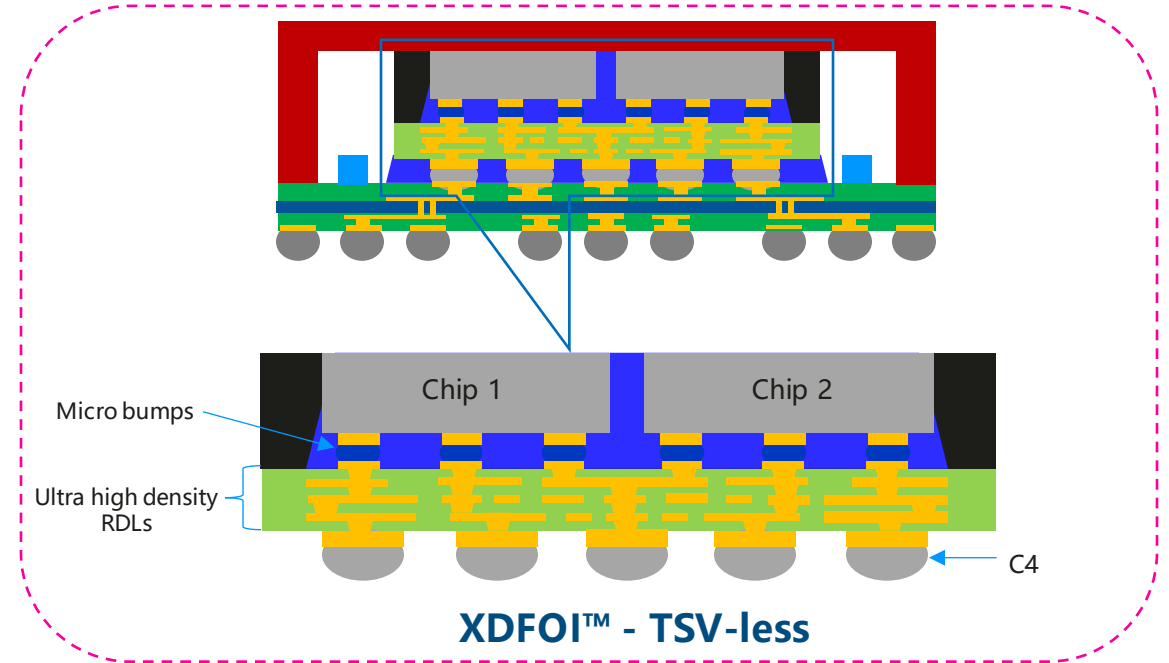
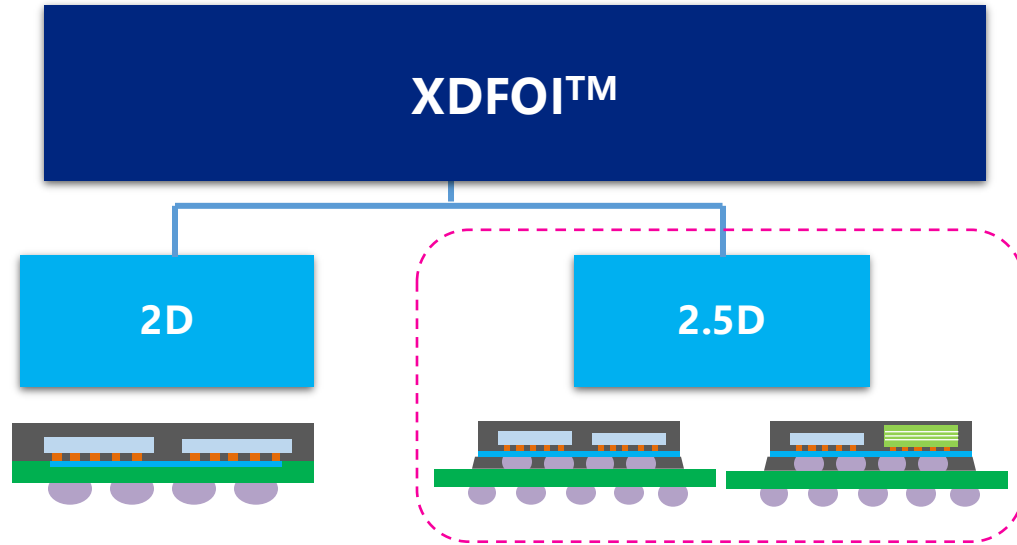


Very high bump density and I/O count

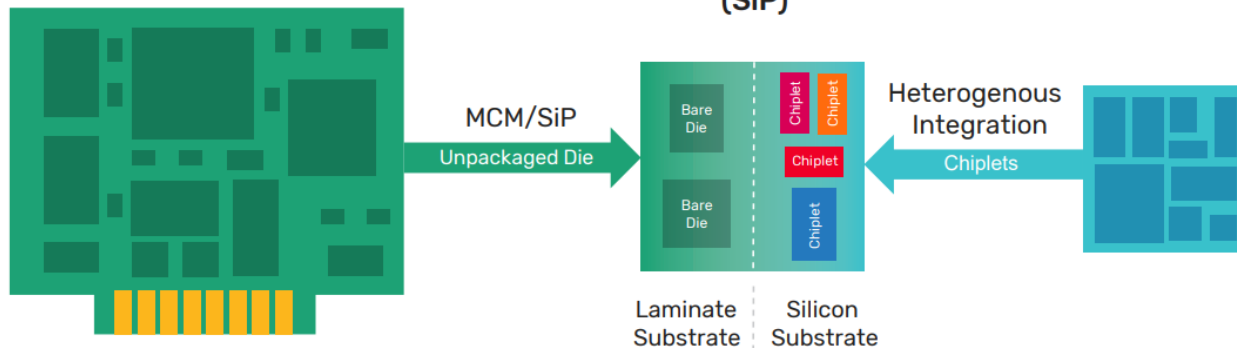
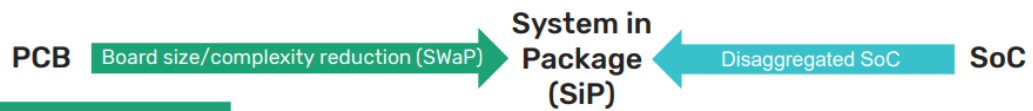
μ -bump pitch a few μ m -55 μ m (~300 ios/mm²)
L/S < 1 μ m

Hybrid bonding
(~12kios/mm²) with TSVs

JCET XDFOI™ Platform



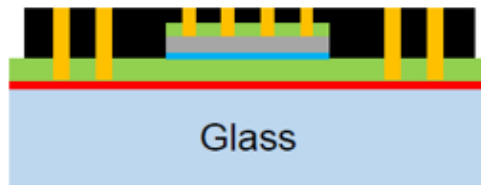
* In Development



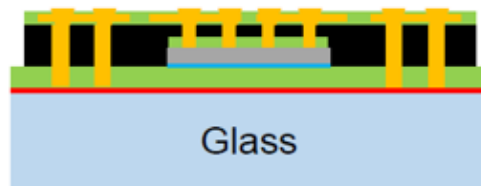
Technology Solutions for XDFOI- EB



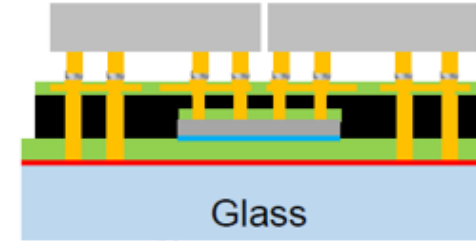
① Release Layer & PI & Cu post



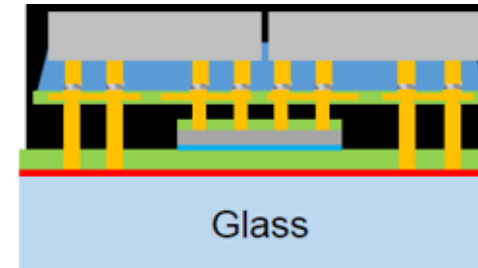
② Die attach & molding & Cu Reveal



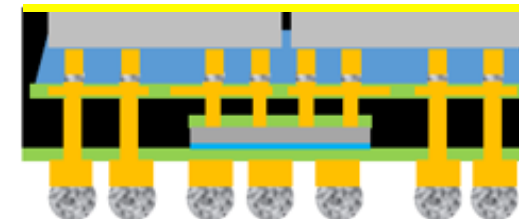
③ RDL



④ Flip chip on wafer



⑤ Underfill & molding

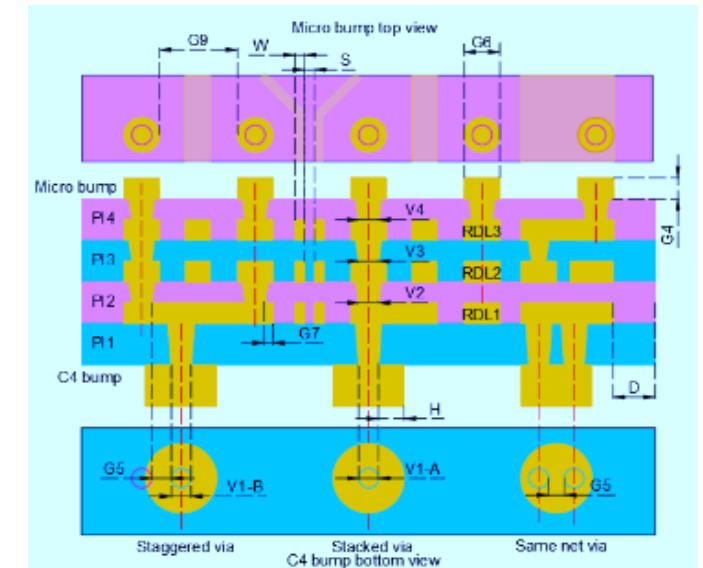
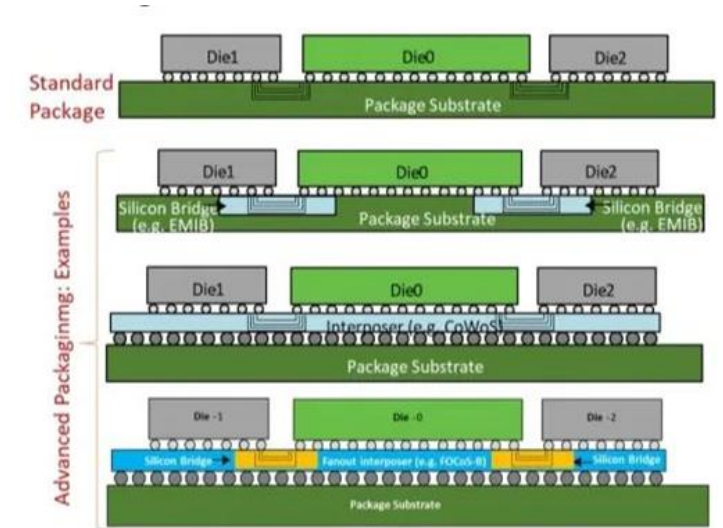
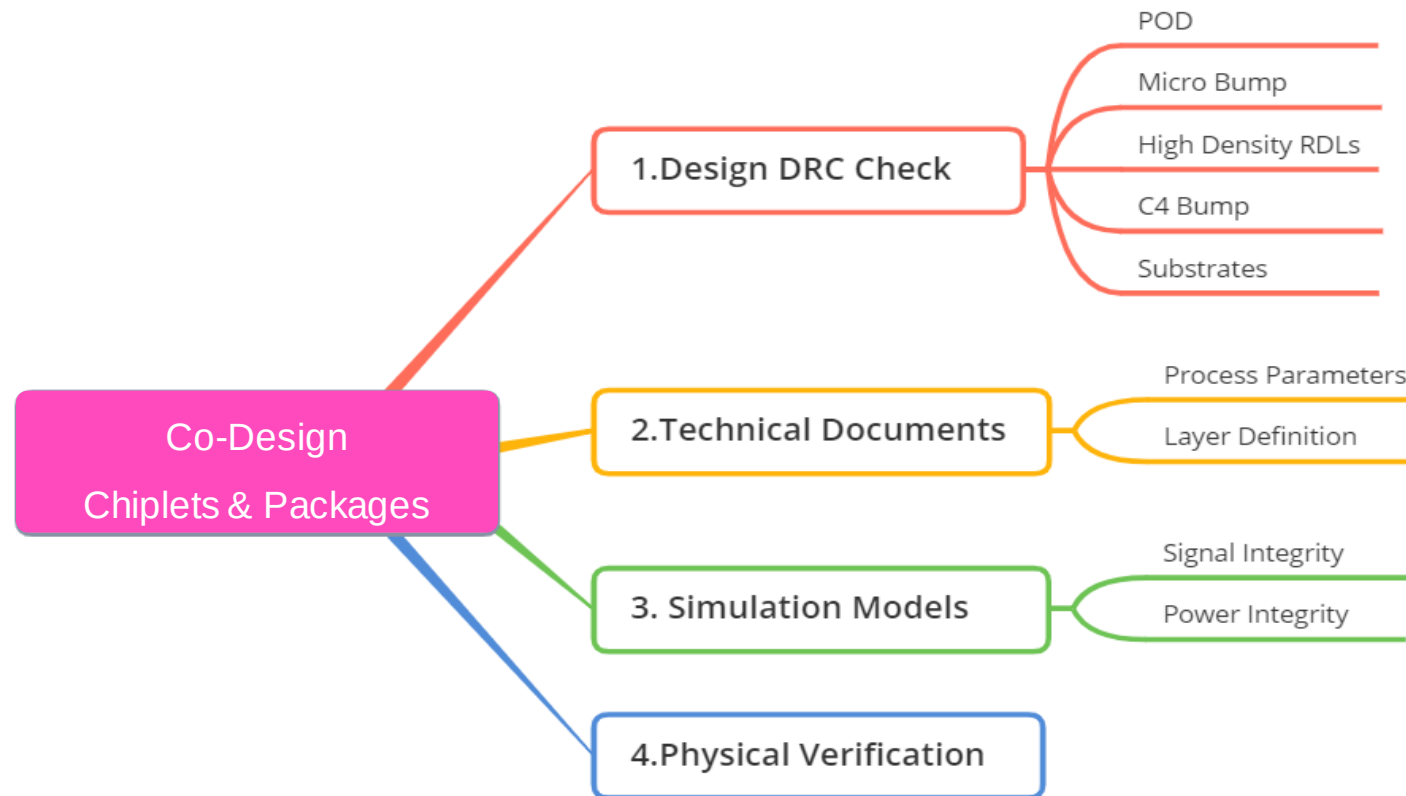


⑥ Carrier release & C4 & BSM

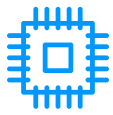
- ❑ Bridge die can be embedded where the high density interconnections are needed.

Heterogeneous Packaging Co-Design Capabilities

- JCET has a professional design service center with package to system-level electrical performance, mechanical, thermal simulation, and 3DIC collaborative design capabilities, empowering XDFOI™ design and simulations.



Summary



Cost and Time-to-Market drive the needs to replace larger SoCs by functional chiplets blocks, i.e., heterogeneously (different Si nodes) integrated.

Chiplets idea does not apply to all applications, but a limited set of advanced compute applications.



Semiconductor industry is collectively supporting various types of chiplet packages, e.g. FC SiP or PoP, High-Density FO, 2.5D, 3D, etc.



Standardization of Die-to-Die (D2D) interconnect protocols enables the semiconductor industry to quickly adopt chiplet technology.



JCET XDFOI™, a novel cost-effective platform for implementing nimble, scalable Heterogeneous Integration, is ready for prime time.



Thank You!

Li Zheng
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