

Improving 4H-SiC MOSFETs by Gate Engineering

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Silicon Carbide has great properties for power electronic MOSFETs:

- Bulk mobility $\sim 900 \text{ cm}^2/\text{V.s}$
- Wide band gap ($\sim 3\text{eV}$) compared to Si ($\sim 1\text{eV}$)
 - Higher $E_{\text{breakdown}}$
 - thinner drift region in power MOSFET
 - lower R_{ON}
- Native oxide
 - Surface passivation
 - Metal oxide semiconductor (MOS) gated channel

BUT

- Poor MOSFET gate stack
 - channel (field effect) mobility ($< 50 \text{ cm}^2/\text{V.s}$)
 - Maximum operating temperature limited to $< 200\text{C}$

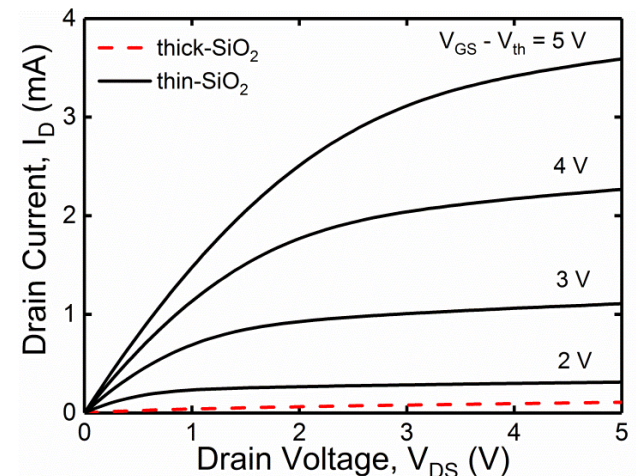
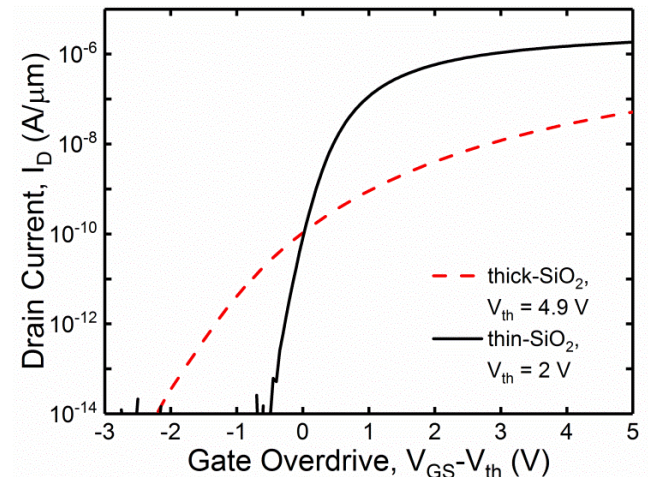
Key Messages

In this work, we demonstrate high performance enhancement mode 4H-SiC MOSFETs:

- High mobility:
 - $\mu_{FE} = 154 \text{ cm}^2/\text{V.s}$; $\mu_{eff} = 265 \text{ cm}^2/\text{V.s}$
- Steep subthreshold slope < 130 mV/dec
- Good temperature stability 25 - 300 °C
- ON/OFF current ratio > 10^6 up to 300 °C
- Low D_{it} $6 \times 10^{11} - 5 \times 10^{10} \text{ cm}^{-2}\text{eV}^{-1}$

Achieved by 0.7 nm $\text{SiO}_2 + \text{Al}_2\text{O}_3$ gate stack

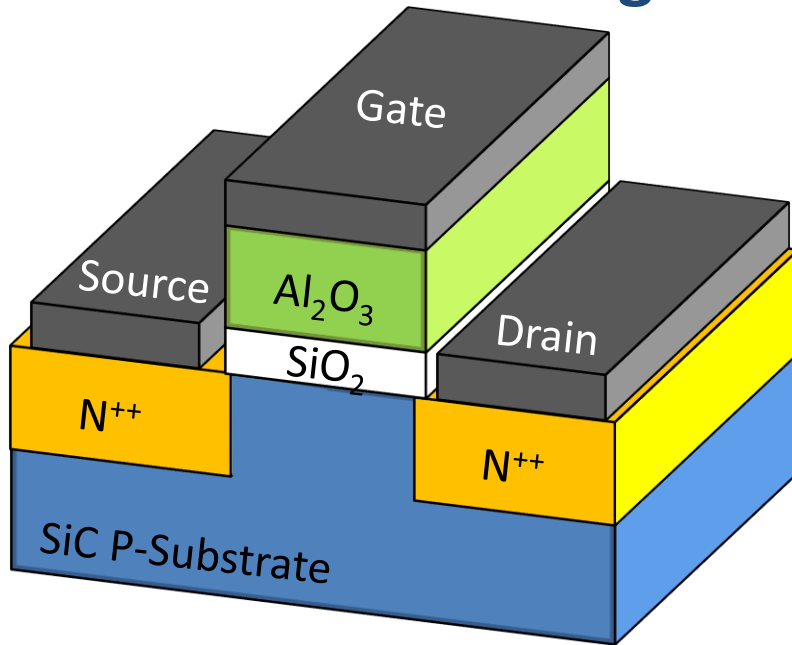
- Less SiC oxidation → less residual C
- Coulomb scattering reduced
- → Phonon-limited mobility is high
- Achieved SiC universal mobility ~50% of Si



Outline

- Background
- 4H-SiC MOS capacitor
- 4H-SiC MOSFET
- Mobility
- Key messages

Background: MOSFET

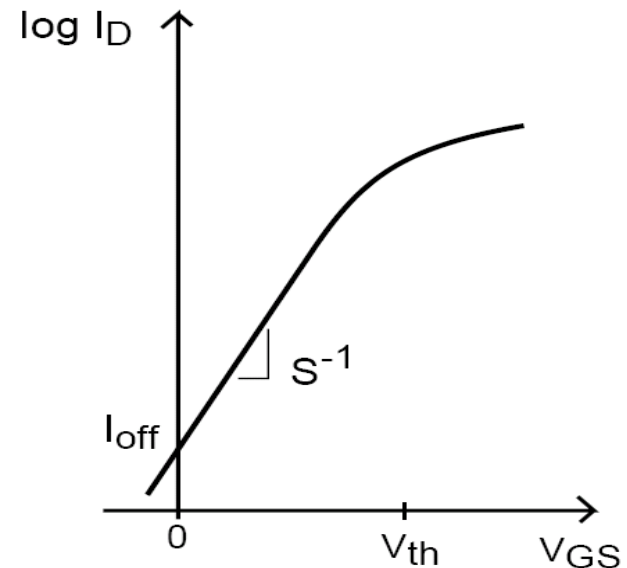
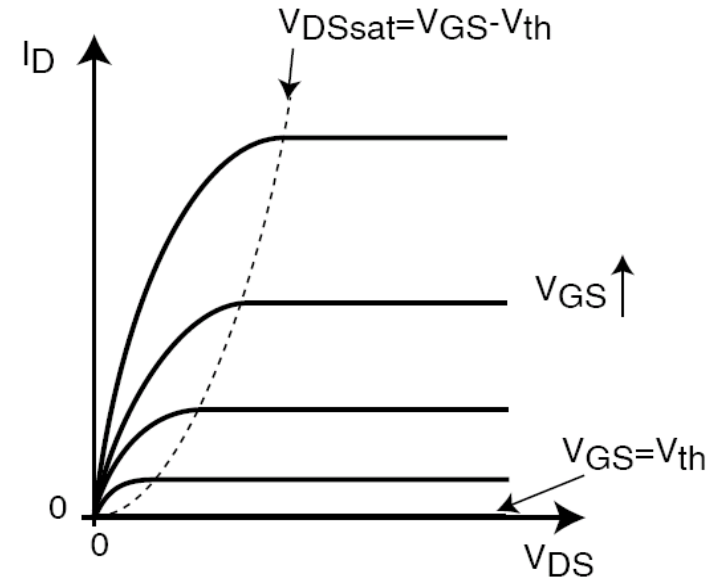


- Current flows through inversion layer
– Si/SiO₂ interface controls mobility.
- Subthreshold current:

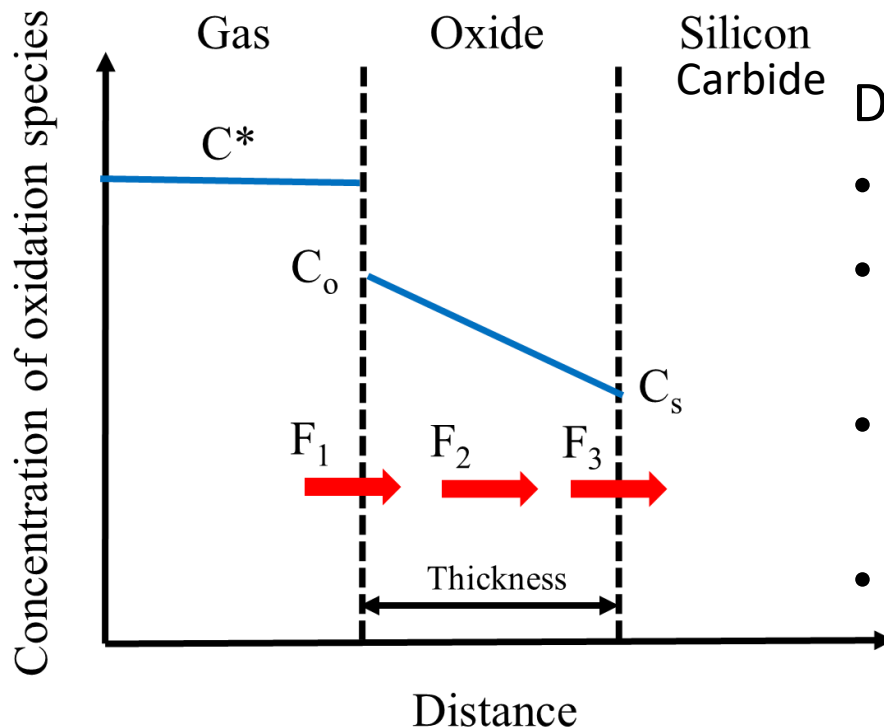
$$I_D \propto \exp \frac{q(V_{GS} - V_t)}{nkT}$$

- Gives subthreshold slope (S):

$$S = \frac{nkT}{q} \ln 10 = 60 \text{ mV/dec at } 300 \text{ K}$$



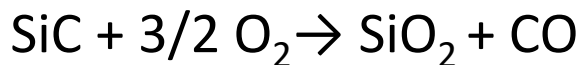
Background: SiC oxidation



Deal-Grove Model (1965)

- oxidant arrives at oxide surface;
- transported across oxide film to semiconductor;
- Arrives at semiconductor surface and reacts to form new SiO_2 .
- But for SiC there is residual C

- Some residual C may out-diffuse through the oxide film



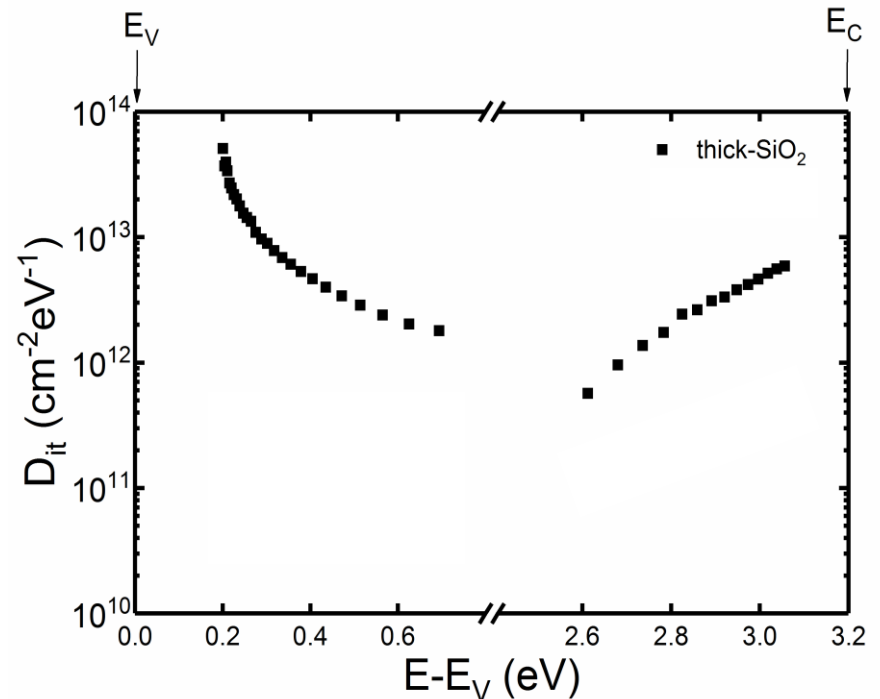
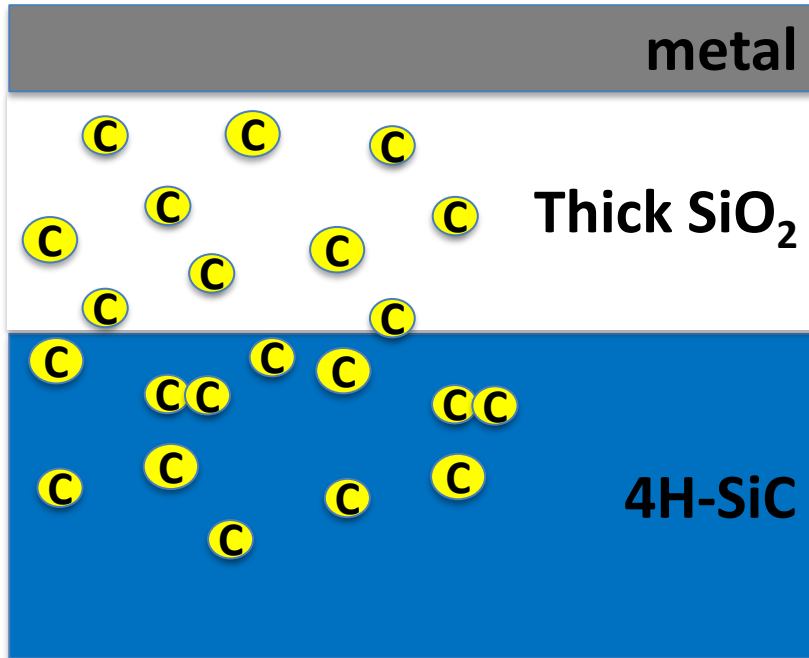
- Some residual C may remain,
 - near interface traps (NITs) in SiO_2 , C related defects in SiC



Outline

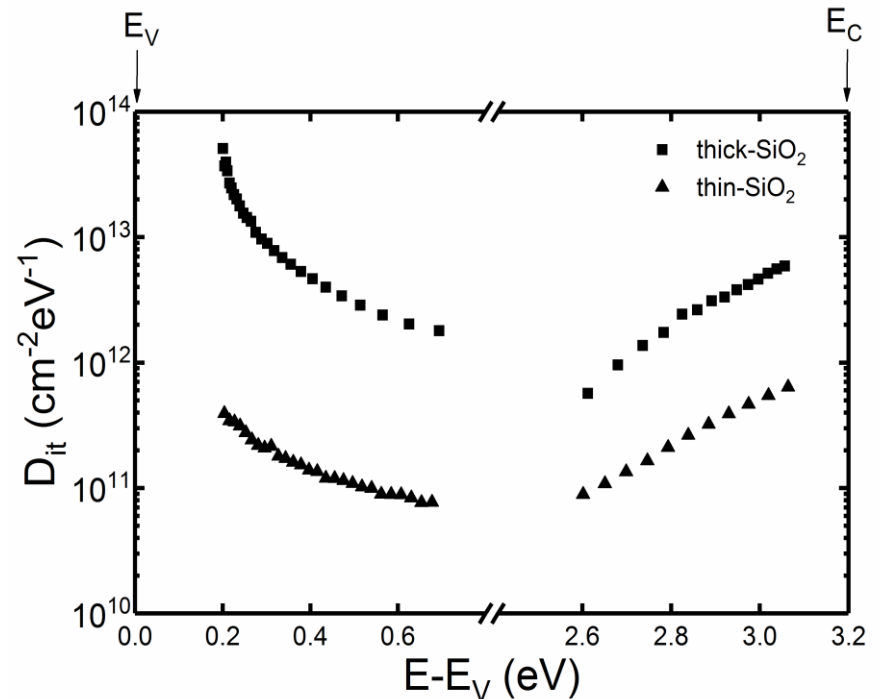
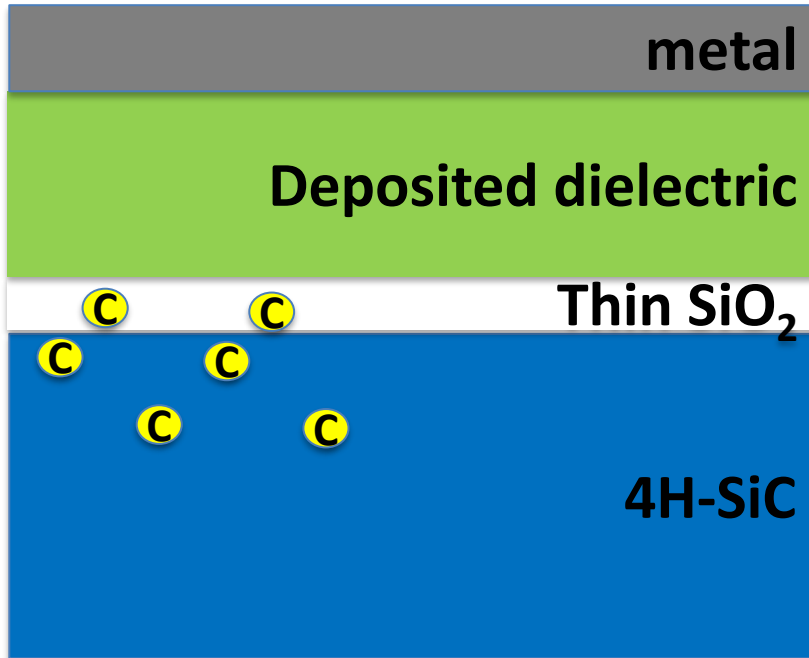
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- 4H-SiC MOSFET
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4H-SiC MOS Capacitor



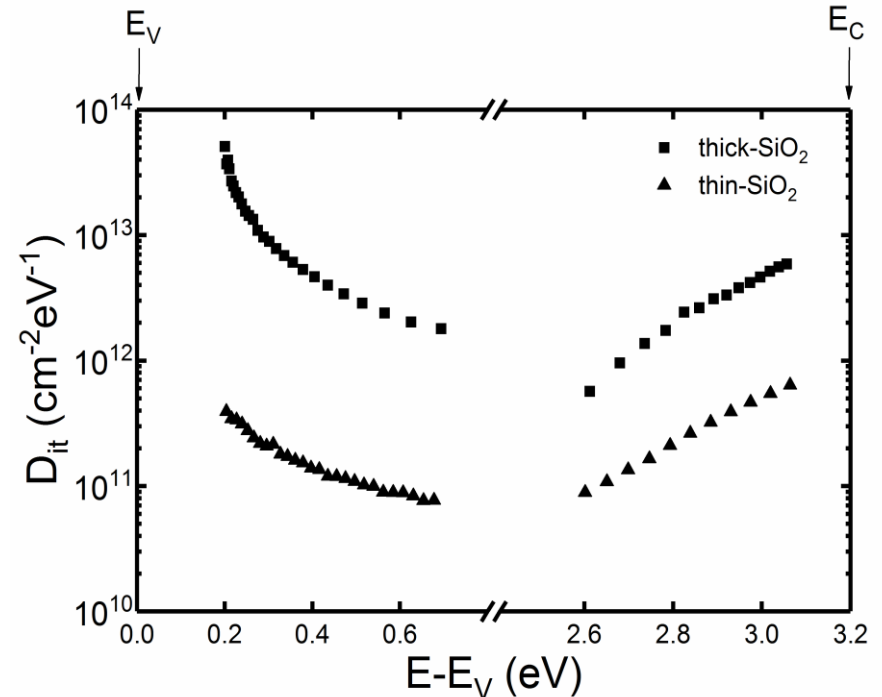
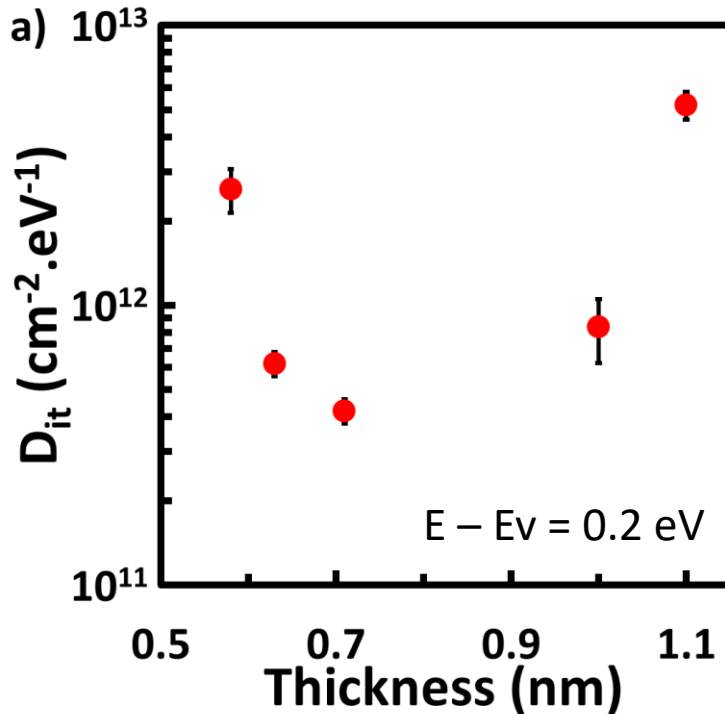
- Conventional MOS gate stack formed by high thermal budget oxidation $\rightarrow$ thick SiO_2
 - 180 min @ 1150 $^{\circ}\text{C}$ $\rightarrow$ 29 nm SiO_2
- High residual C near SiO_2/SiC interface
 - Near interface traps (NITs) in SiO_2
 - Interstitial, complex clusters of C in SiC, e.g. $(\text{C}_i)_2$

4H-SiC MOS Capacitor



- Here, MOS gate stack formed by low thermal budget oxidation → thin SiO₂
 - 3 min @ 600 °C → 0.7 nm SiO₂
 - Deposit (ALD) Al₂O₃ to achieve 29 nm effective oxide thickness
- low residual C near SiO₂/SiC interface
 - D_{it} 100x smaller than thick SiO₂

4H-SiC MOS Capacitor

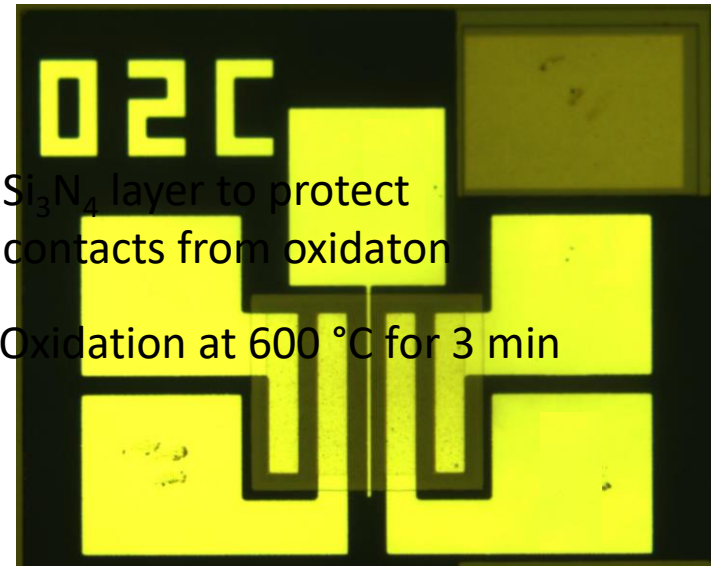
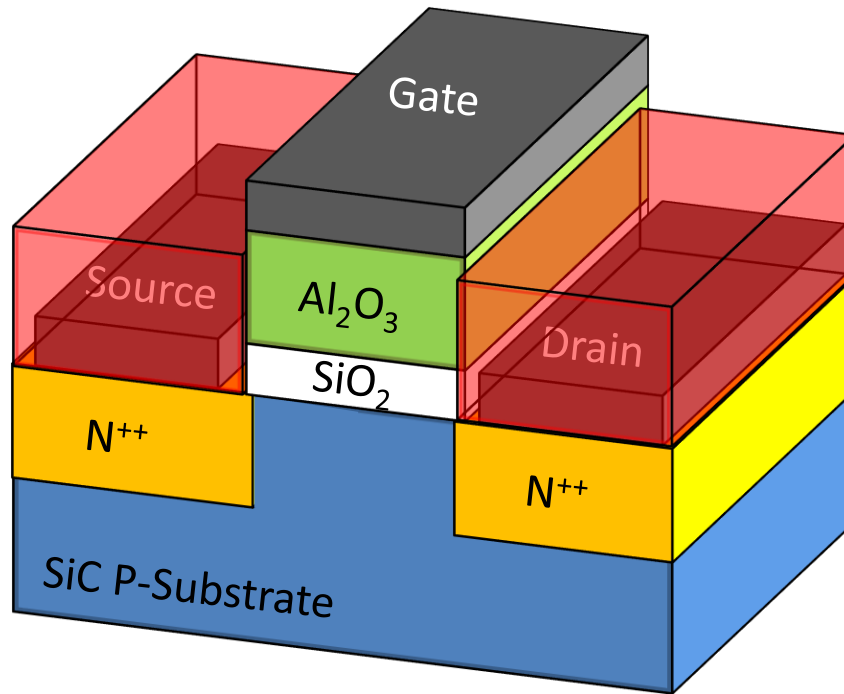


- D_{it} passes through a minimum corresponding to 0.7 nm SiO₂ layer
- minimum D_{it} occurs for a thermal budget of 600 °C for 3 min
- corresponds with 0.7-nm growth of SiO₂
- MOS capacitors have the same gate stack as MOSFETs
- For thin SiO₂
 $D_{it} = 6 \times 10^{11} - 5 \times 10^{10} \text{ cm}^{-2}.\text{eV}^{-1}$

Outline

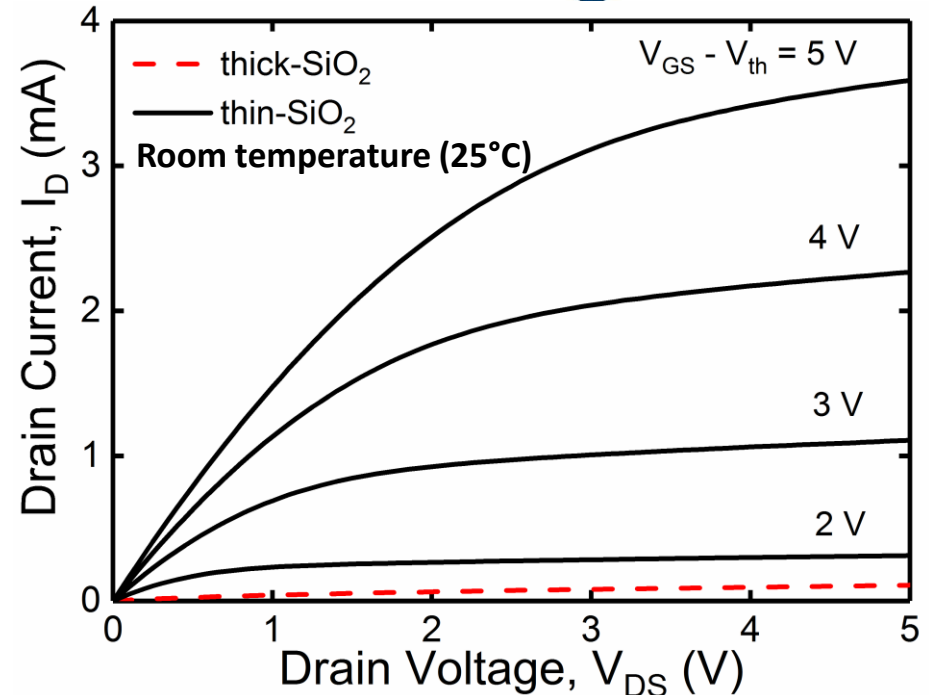
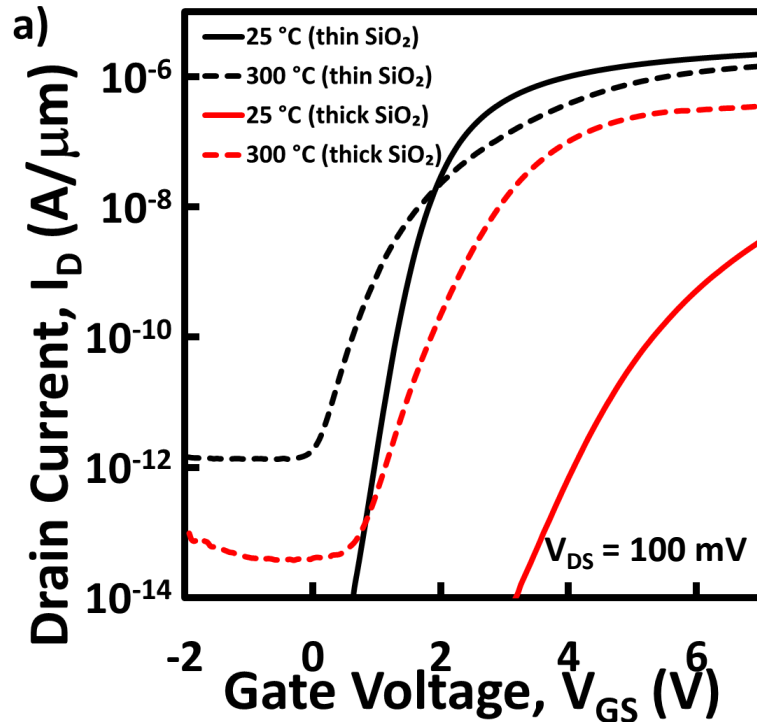
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4H-SiC MOSFET



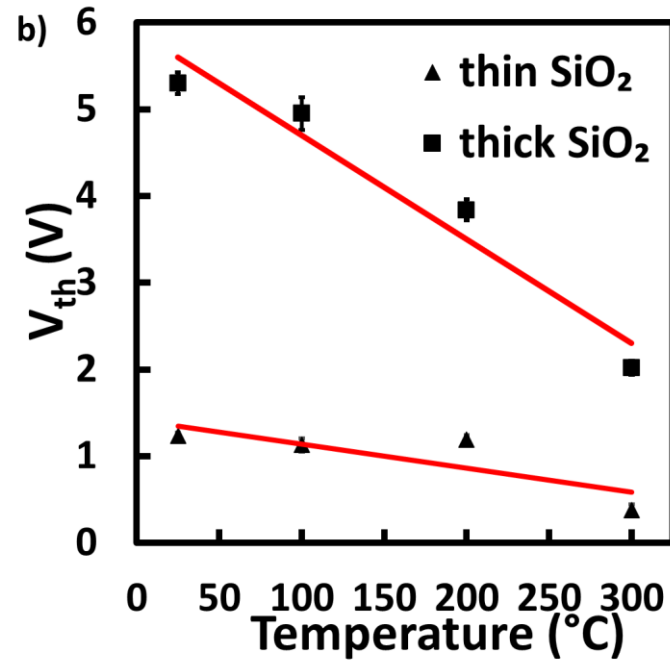
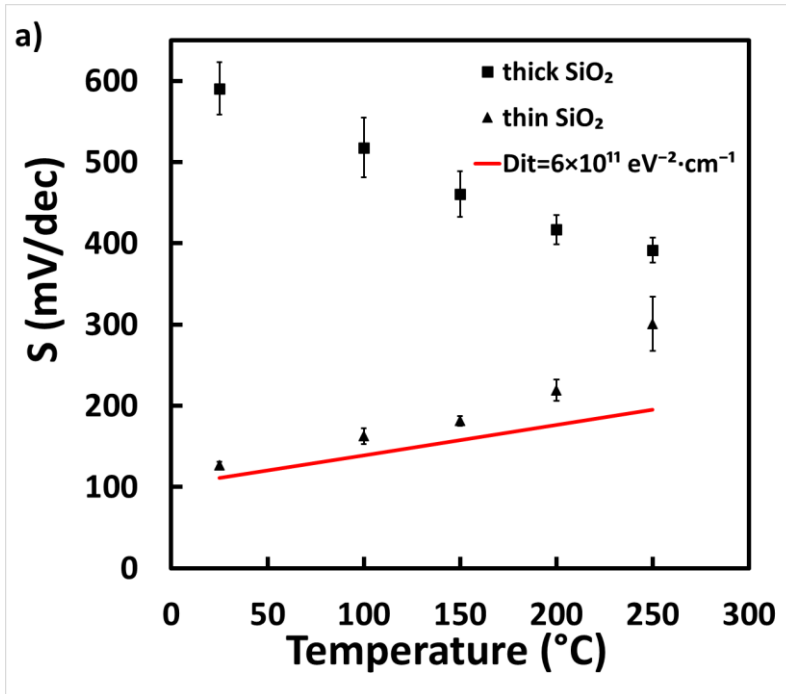
- 4H-SiC: Si-face, n^+ (sub)/ p^+ (10^{17} cm^{-3} , $5 \mu\text{m}$)/ p^- ($5.3 \times 10^{15} \text{ cm}^{-3}$, $1 \mu\text{m}$)
- Source/Drain:
Implantation N $4.7 \times 10^{19} \text{ cm}^{-3}$, 100 nm .
S/D Contacts: Ti (5 nm) + Ni (90 nm). @ 1000°C for 3 min in Vacuum
- Channel length (L) $2 \mu\text{m}$ x width (W) $100 \mu\text{m}$
- Effective Oxide Thickness = 29 nm (0.7 nm SiO_2 + 40 nm Al_2O_3)
- Control MOSFETs fabricated with 29 nm SiO_2 . @ 1150°C for 180 min

Experimental: I-V data



- I_D - V_{GS} measured at room 25°C and 300°C
- For thin SiO₂ MOSFET:
 - $I_{off} = 1.8 \times 10^{-12}$ A/ μ m at 300°C
 - $SS < 130$ mV/dec
 - Much higher I_{on} compared to thick SiO₂ control
 - All devices enhancement mode

Experimental: I-V (T) data



- subthreshold slope (S) is the inverse gradient of $\text{Log } I_D$ versus V_{GS}

$$S = n \frac{kT}{q} \ln(10), \quad n = \frac{C_{ox} + C_{dep} + C_{it}}{C_{ox}} \approx 1.88 \text{ for thin } \text{SiO}_2$$

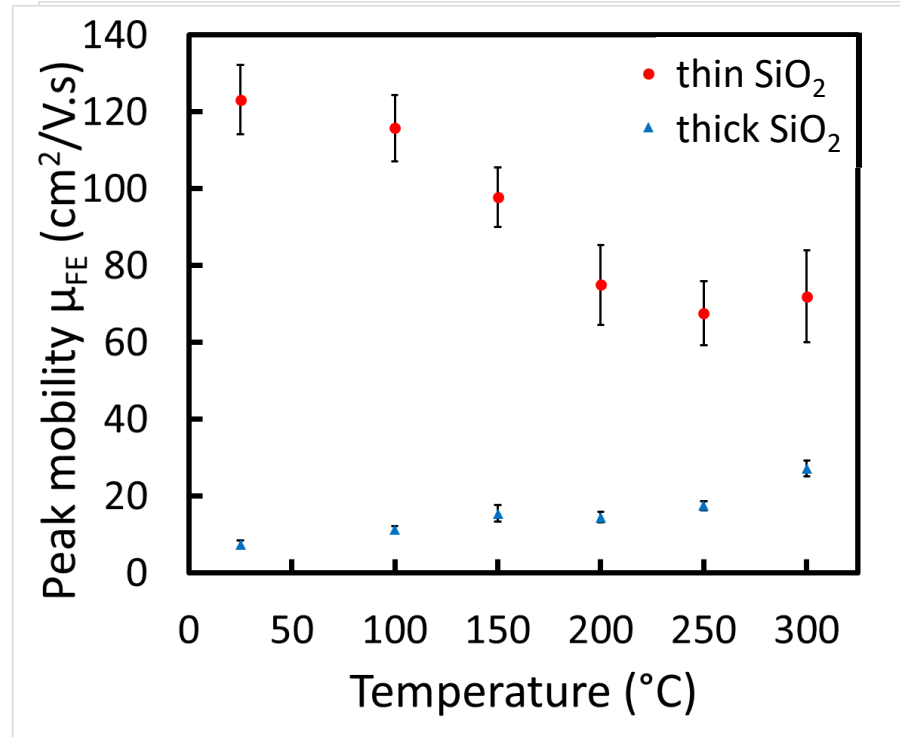
$$\approx 67 \text{ for thick } \text{SiO}_2$$
- Good fit with $D_{it} \Leftrightarrow$ large reduction in defect density
- V_{th} slope is significantly steeper for the thick- SiO_2 devices (-11.8 mV/K) compared with the thin- SiO_2 devices (-4.6 mV/K and comparable with Si devices)

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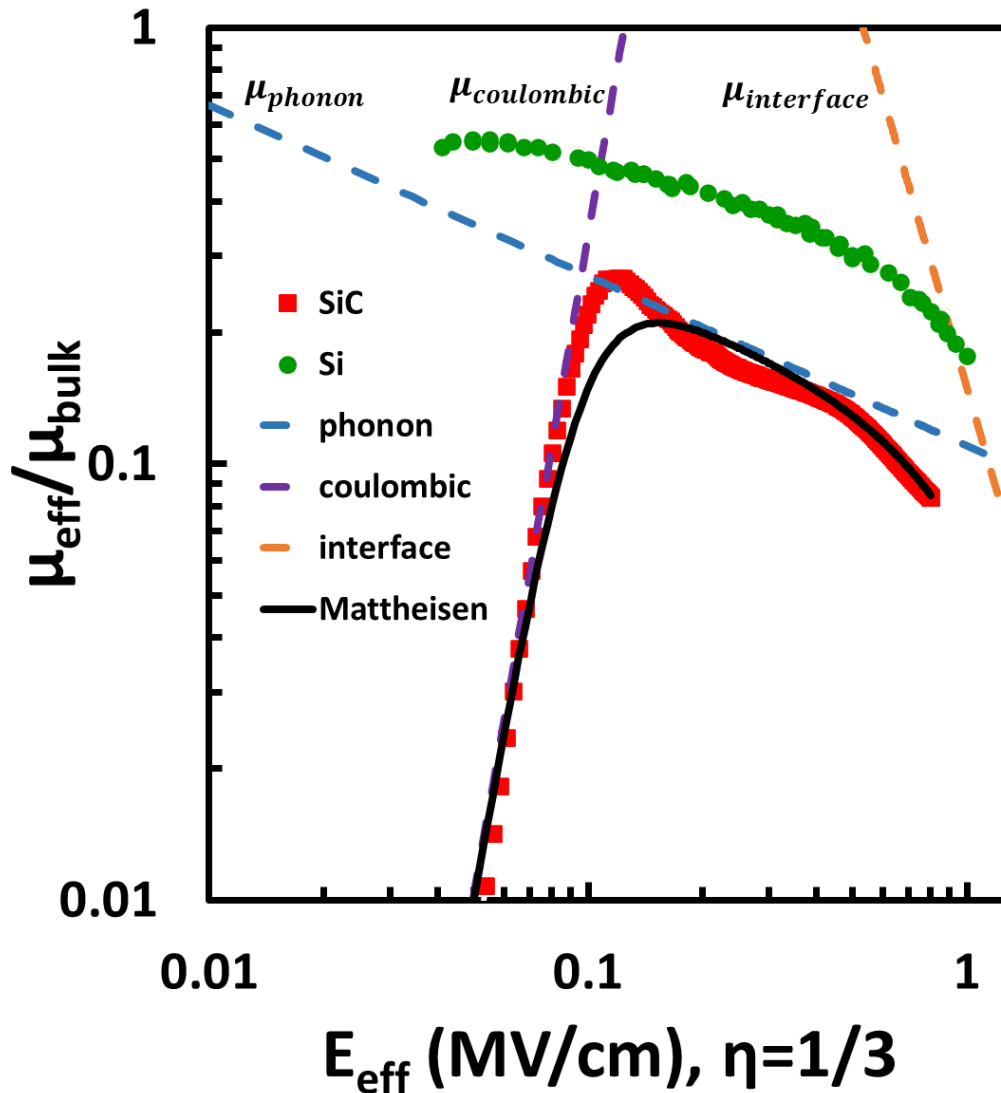
Experimental: mobility $\mu_{FE}(T)$

- μ_{FE} reduces by 40% at $T=300^{\circ}\text{C}$
 - sustains high mobility
- $\mu_{FE} \downarrow$ as $T \uparrow$ for thin SiO_2
 - phonon scattering
 - greater lattice vibration as $T \uparrow$
- $\mu_{FE} \uparrow$ as $T \uparrow$ for thick SiO_2
 - coulombic scattering
 - interaction time reduces as $T \uparrow$



- The temperature dependence of mobility for the thin- SiO_2 MOSFETs shows that it is dominated by phonon scattering
 - fewer C related defects reduces coulombic scattering
 - gives rise to its high mobility .

Experimental: SiC versus Si mobility



- Si, SiC bulk mobilities are similar:
Si $\mu_{\text{bulk}} = 1450 \text{ cm}^2/\text{Vs}$
4H-SiC $\mu_{\text{bulk}} = 900 \text{ cm}^2/\text{Vs}$
- Universal mobility plot reveals:

- SiC devices ~50% of Si devices
- contributions to scattering:

$$\frac{1}{\mu} = \frac{1}{\mu_{\text{coulombic}}} + \frac{1}{\mu_{\text{phonon}}} + \frac{1}{\mu_{\text{interface}}}$$

- Fitting to the data gives:

$\mu = Ae^B$	$\eta=1/3$		$\eta=1/2$	
	A	B	A	B
coulombic	3×10^7	5	5×10^5	3.4
phonon	99	-0.39	117	-0.39
interface	135	-3	360	-2

$$E_{\text{eff}} = \frac{q}{\epsilon_0 \epsilon_{\text{SiC}}} (N_{\text{depl}} + \eta N_s)$$

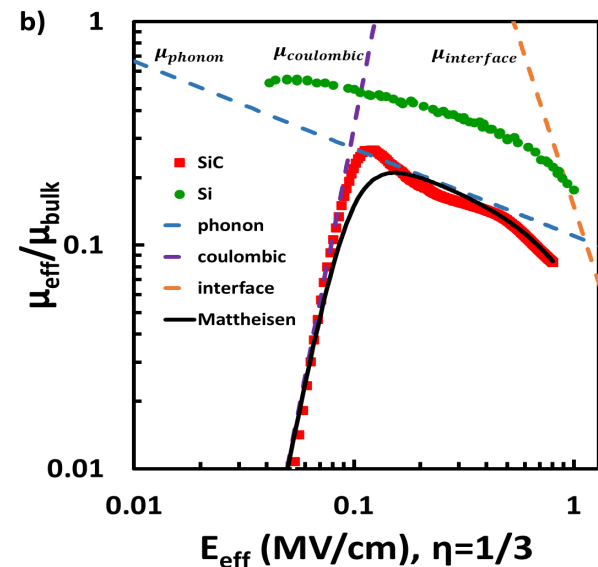
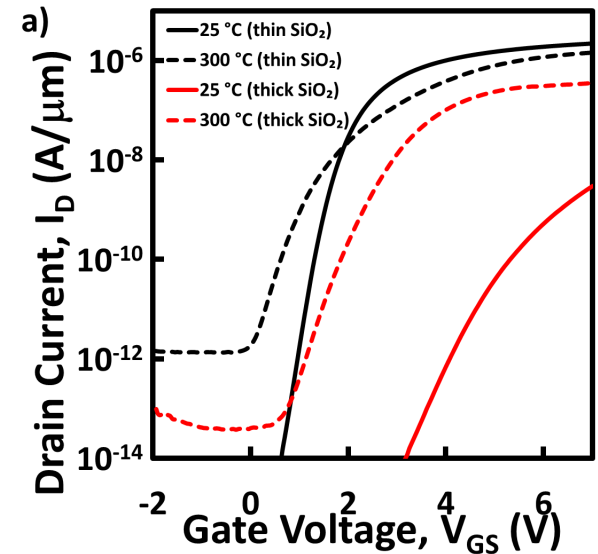
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Thanks for your attention!

Further reading:

- J. Urresti *et al*, “Design and Analysis of High Mobility Enhancement-Mode 4H-SiC MOSFETs Using a Thin-SiO₂/Al₂O₃ Gate-Stack”
IEEE Trans. Electron Devices, vol. 66(4) pp. 1710-1716, 2019
- F. Arith et al, “Increased mobility in enhancement mode 4H-SiC MOSFET using a thin SiO₂/ Al₂O₃ gate stack,”
IEEE Electron Device Lett., vol. 39 (4) pp. 564–567, 2018