



ASE GROUP

Integrated Photonics Packaging: Solutions for Silicon Photonics Applications

2022 Semicon Europe Integrated Photonics Symposium

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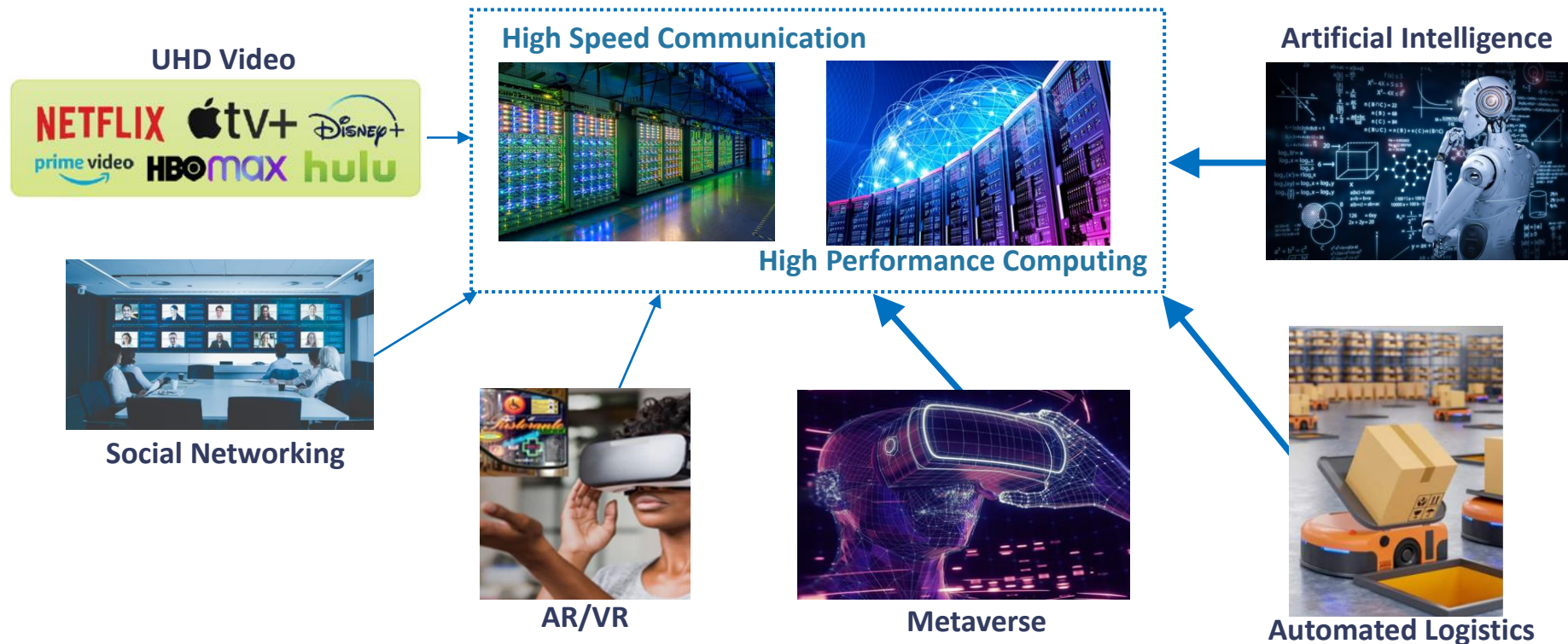


Outline

- Introduction / Motivation
- ASE Photonics Toolbox
- Advanced Packaging for Co-Packaged Optics
- Fiber Optical Coupling
- Optical Test Solution
- Sensor & Edge Applications
- Conclusions

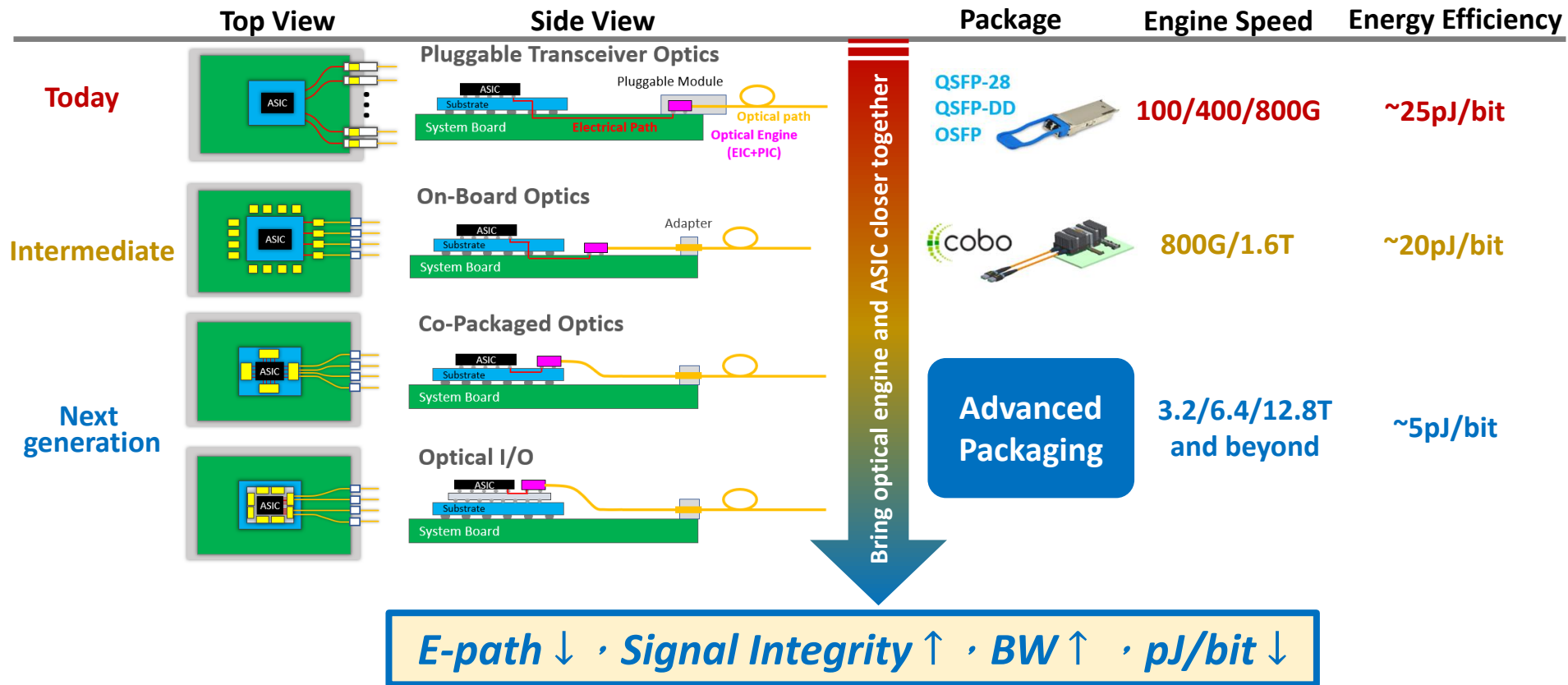


Motivation



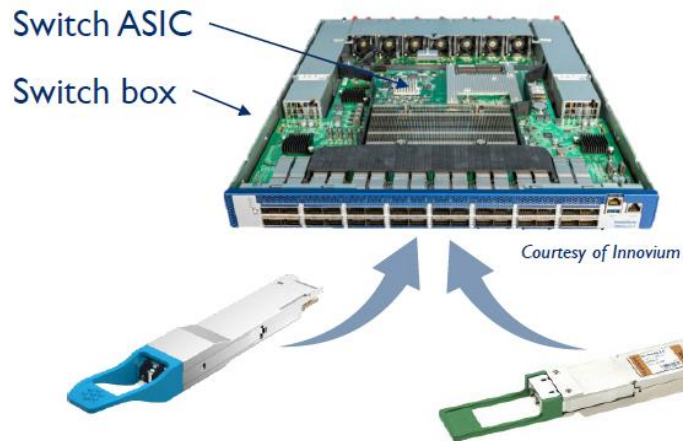
*extracted from Yole 2022

Fiber Optics Evolution in the Data Center



Pluggable Optics vs. Co-Package Optics (Yole 2022 report)

Faceplate-pluggable (FPP) or Pluggable

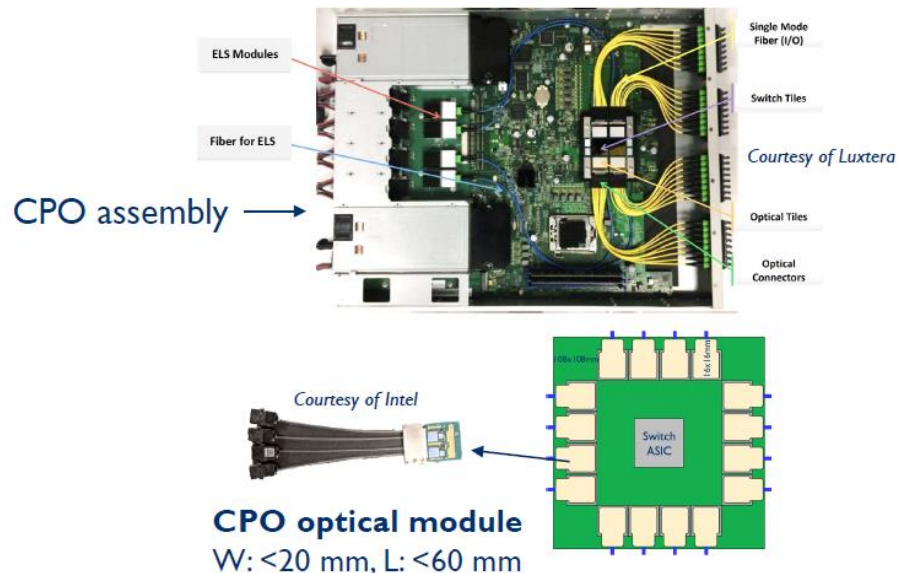


QSFP-DD W: 18.35 mm, L: 89.4 mm and T: 8.5 mm

OSFP W: 22.58 mm, L: 107.8 mm and T: 13.0 mm

- **Pluggable module transceivers** are external to the network and are installed and function similarly to other computer peripherals or may function as standalone devices.

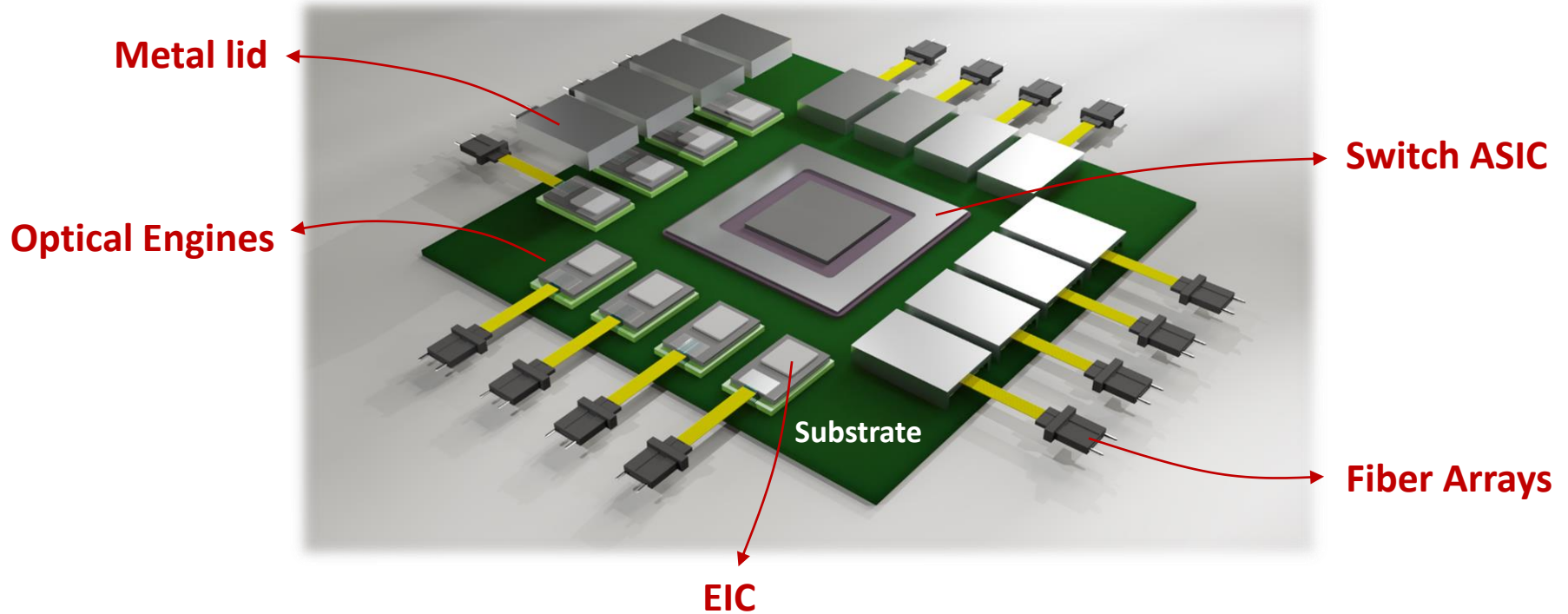
Co-Packaged Optics (CPO)



- **CPO transceivers (optical tiles or engines)** are small and are inserted onto a system board or wired directly onto a circuit board.

Conceptual Drawing of Co-Packaged Optics

Co-packaged optics



Co-Packaging Optics Challenges

Ultra-high D2D Bandwidth

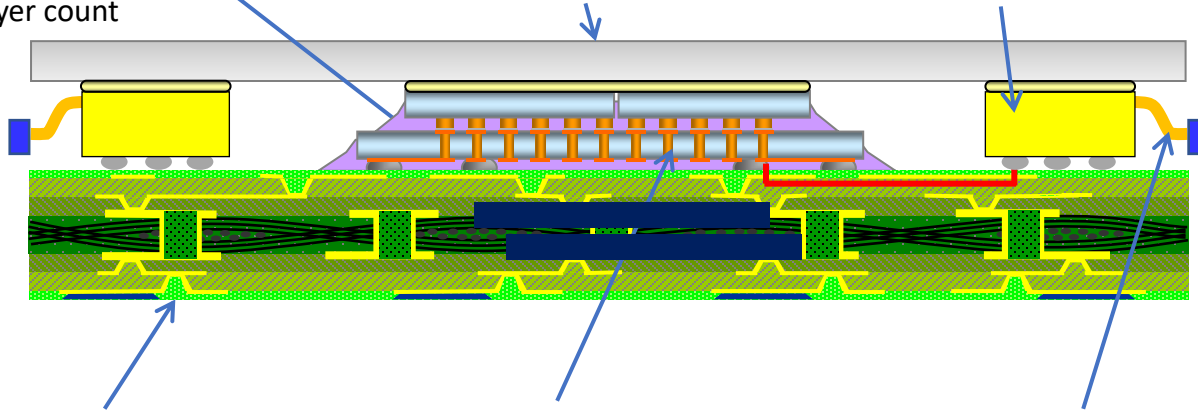
- Interconnect pitch
- RDL L/S
- Layer count

High Power Solution

- Lid
- TIM1

Optical engine

- Engine size/ Data rate
- PKG structure



Super Large Package

- Package Warpage
- L2 Reliability

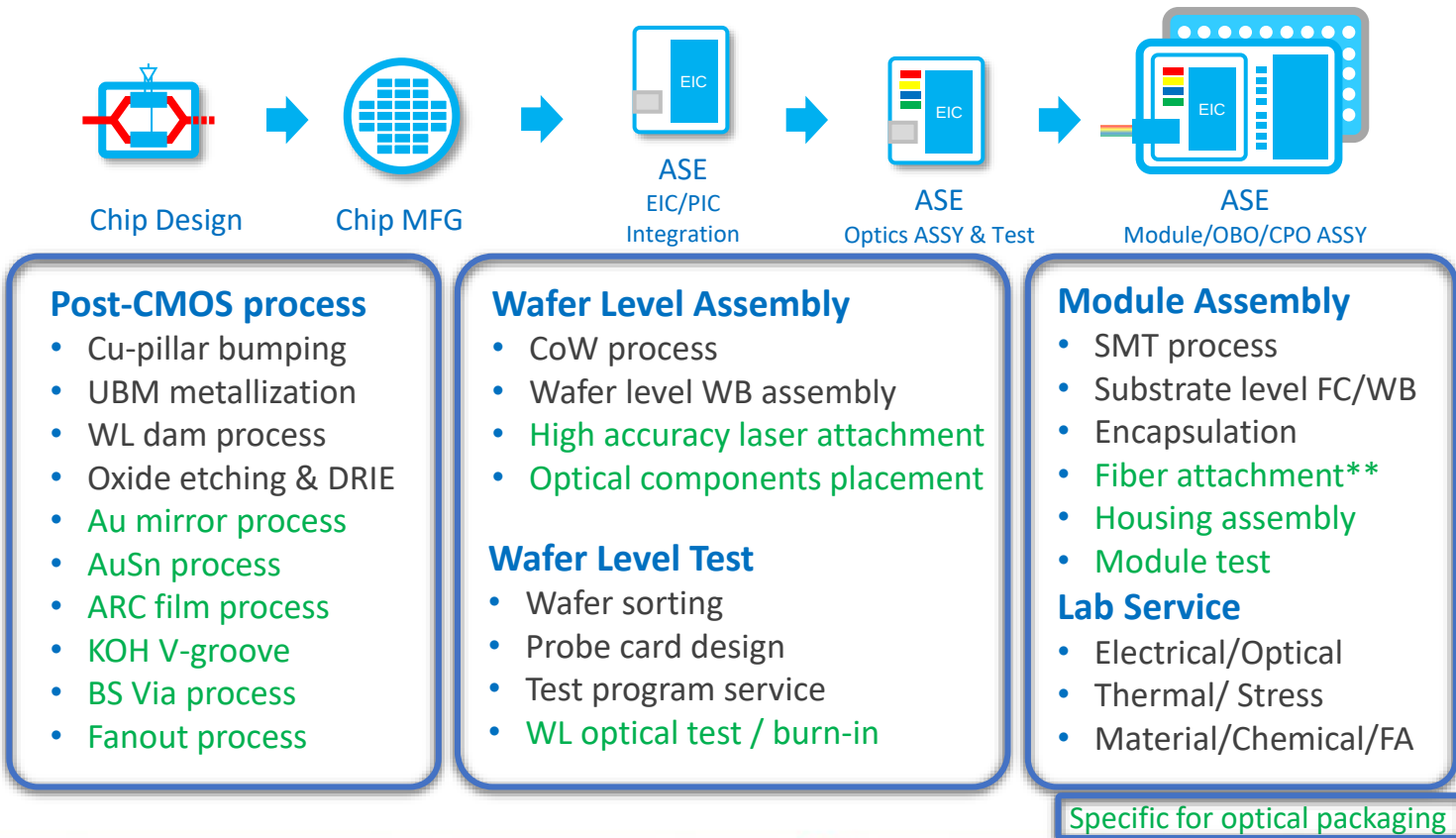
Large Fan-Out / Interposer Size

- Warpage
- Package Reliability

Fiber Attach

- Fiber connector workability
- Warpage/ Thermal stability

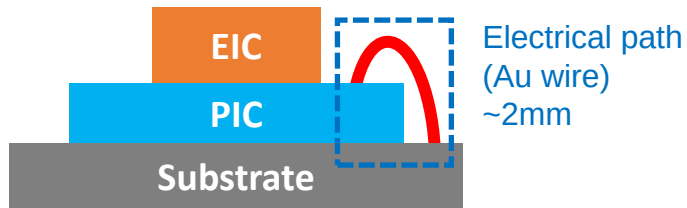
ASE Toolbox : Consolidate supply chain for cost reduction



Advanced Packaging for Optical Engine

- Package structure comparison

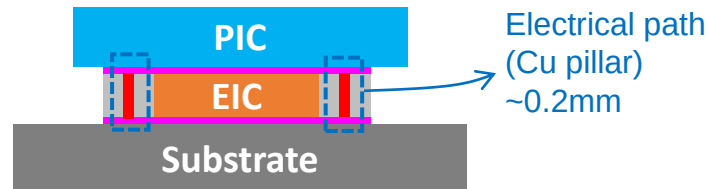
CoW & WB interconnect



Features:

- EIC stacked on PIC. F2F integration
- Larger form factor
- Au wire as interconnect
- Electrical path ~2mm
- Impedance not controlled

Fan-Out Package On Package (FOPOP)

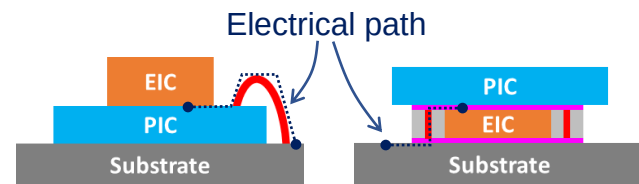
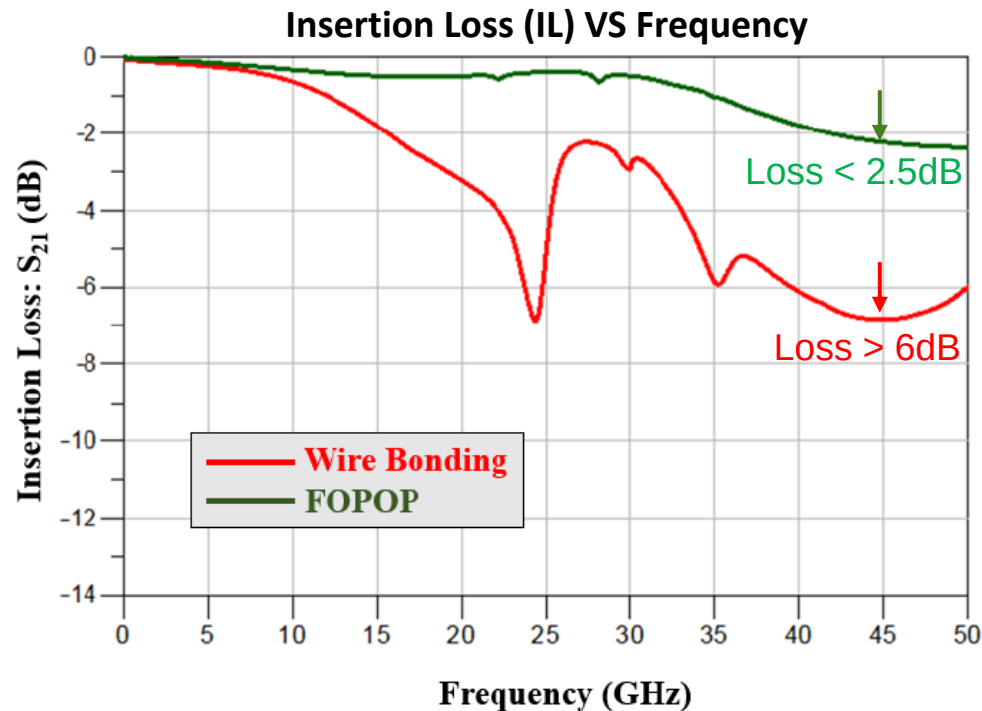


Features:

- PIC stacked on EIC fanout PKG. F2F integration
- Smaller form factor
- Cu pillar as interconnect
- Electrical path ~0.2mm
- Impedance controlled

Package Comparison – Electrical Performance

- S21 insertion loss simulation comparison

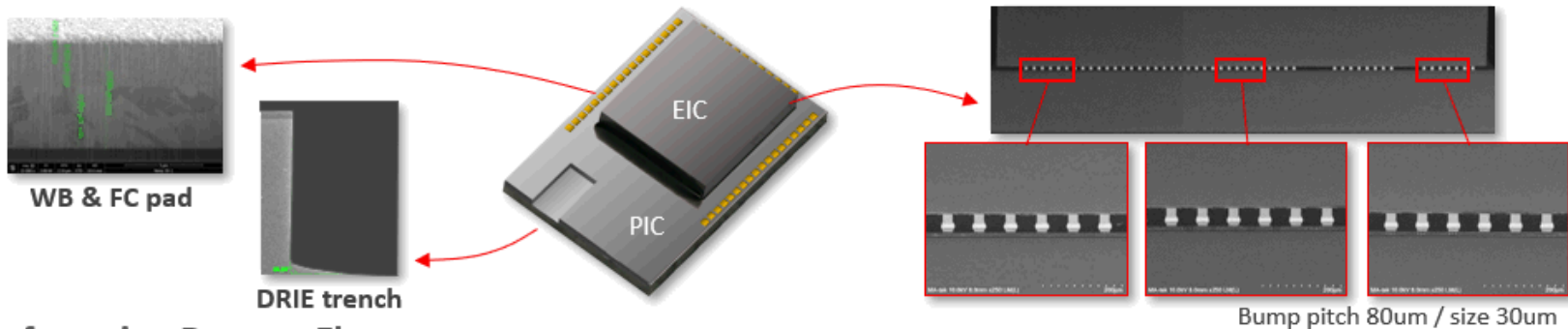


Package	CoW w/ WB	FOPOP
Simulation results	- Resonance due to bonding wire inductance - IL ~ 6dB @50GHz	- Smooth frequency response - IL < 3dB @50GHz - Better signal integrity

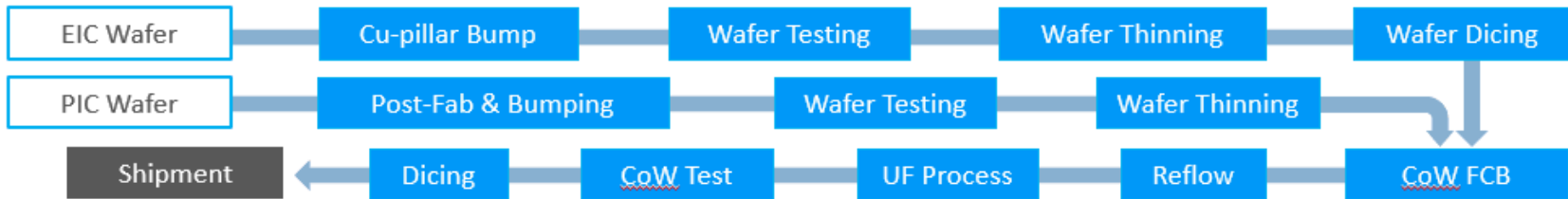
Process Flow – Die on Wafer

CoC Structure & Bumping Process

- Cu/Ni/SnAg Cu-pillar bump & Cu/Ni/Au UBM capability



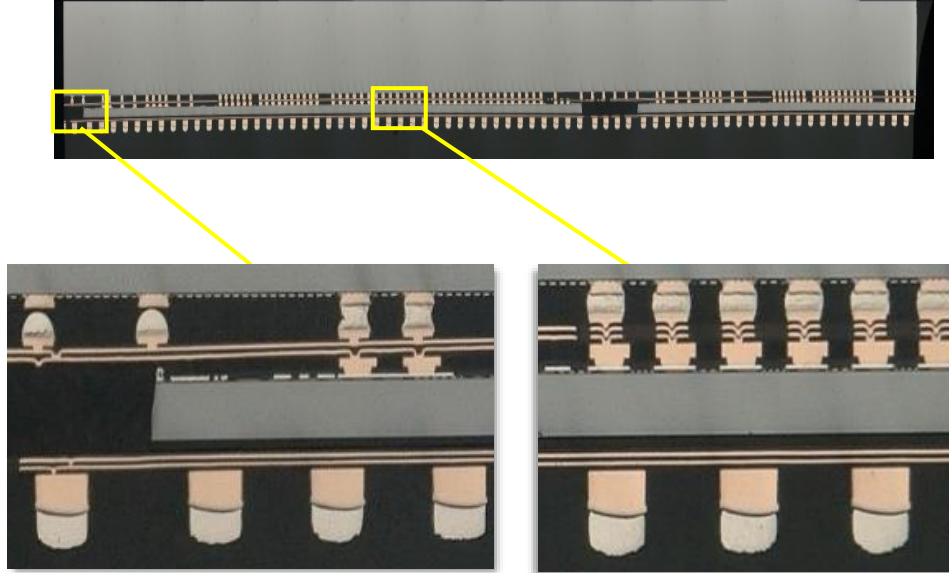
Manufacturing Process Flow



Reliability

- TCT1000/HTST1000/THT1000/HAST96 Qual Pass

Test Vehicle - Fanout-POP for EIC (VIPack™ Pillar VI)

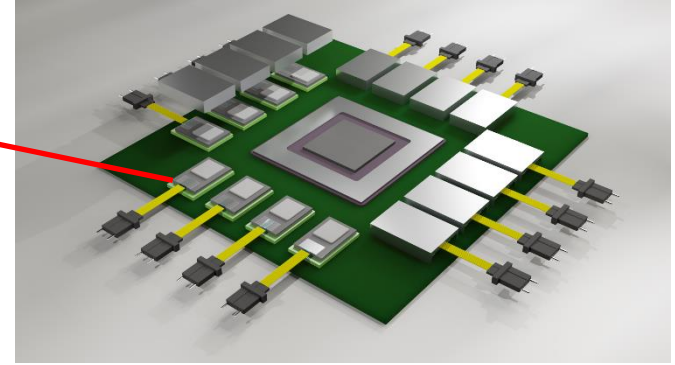
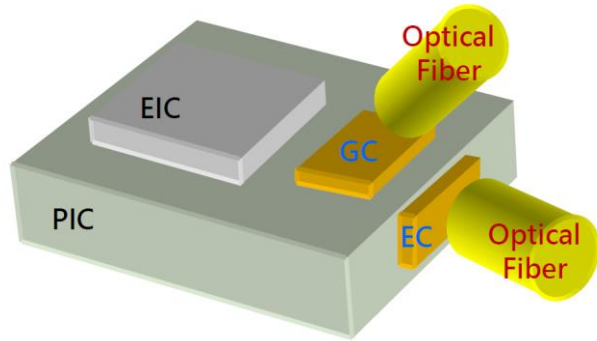


Fiber to PIC Optical Coupling

Coupling between PIC & Fiber

- Efficiency is reduced by **mode mismatch**
 - Large dimension gap
 - Geometry difference

Particular coupling design for PIC

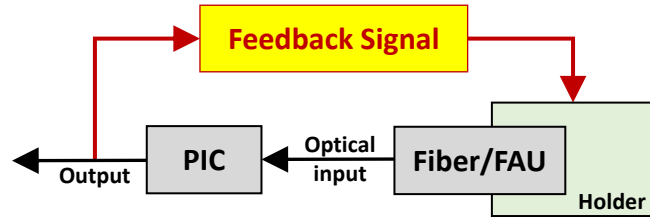


Coupler Design	Grating Coupler (GC)	Edge Coupler (EC)
Coupling Direction	Vertical	Lateral
Bandwidth	Narrower	Broader
Polarization Dependence	Stronger	Weaker
Remarks	<u>Convenient to fulfill wafer-level testing</u> due to coupling direction	Promising for <u>high bandwidth applications</u>

Fiber to PIC Optical Coupling

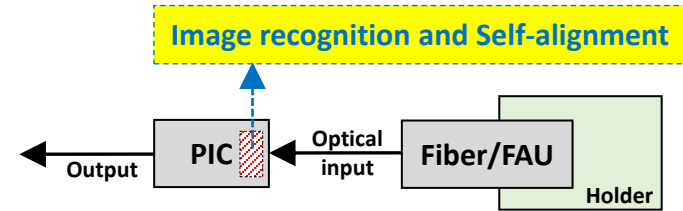
- Fiber alignment comparison

Active Alignment



- Mechanism:**
Holder will not stop actuation until the feedback achieves the threshold
- Time consumption:** Higher
- Convenient to fulfill real-time monitoring of coupling data**

Passive Alignment



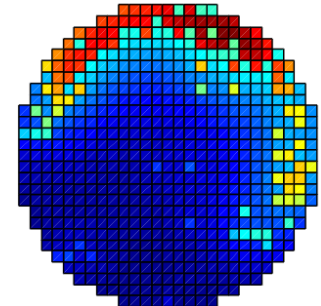
- Mechanism:**
Image recognition at beginning and self-alignment design
- Time consumption:** Lower
- Promising choice for high volume production**

Optical Test Solution for PIC

- **PIC KGD wafer maps by wafer level optical test solution**

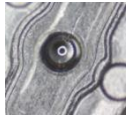
Wafer Sorting Types

Types	Electrical Testing	Optical Testing	Optoelectronic Testing
Input/Output	Electrical/Electrical	Optical/Optical	Optical/Electrical OR Electrical/Optical
DUT	Electronic components	Passive optical components	Passive/Active optical components



KGD Wafer Map

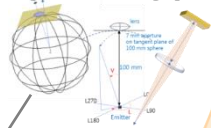
- **O/O & O/E test are required for PIC wafers**
- **Known good optical engine is critical to enable high CPO assembly yield**



Window

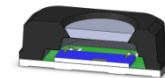
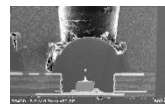
- Barrel Lens
- Glass
- Film
- WLO
- DOE/MLA
- Lens Lid

Eye Safety(IEC)



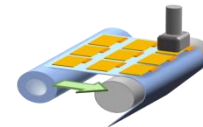
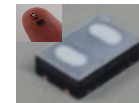
Clear Molding

- Transfer
- Liquid-Transfer
- Compression
- Double Molding

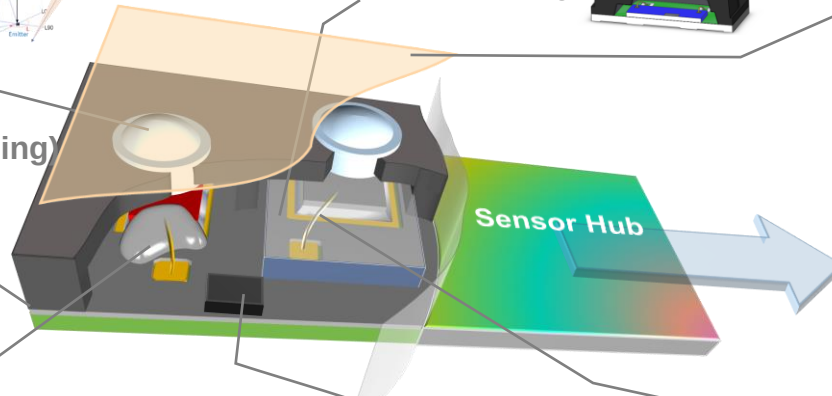


Protective Film

- PTFE/ePTFE
- PI



Semi-Hermetic Hermetic(Seam Welding)

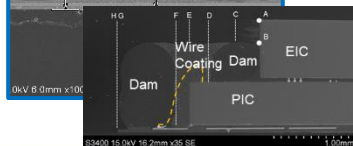
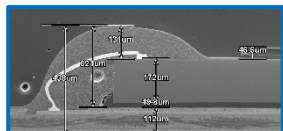


Spectroscopy
Bio
LiDAR
MOEMS
etc.

Lab On Chip

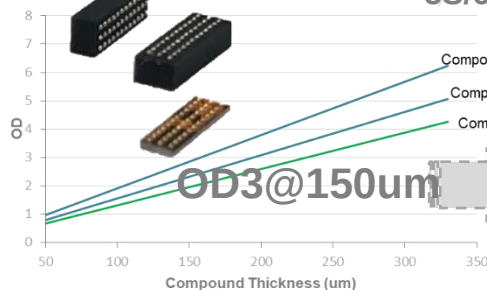
Wire Coating

- Dome Coat
- Stripe Coat
- Dam & Fill



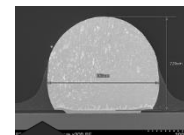
Optical Density@940nm

5S/6S Protection

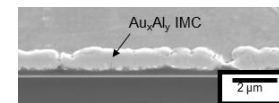


OD3@150um

OD5@2um



LTW(Low Temp WireBonding)



Leverage our LTW technology, achieving **6,000,000kg CO₂** emission reduction/year which is equivalent to plant **15000 trees/year**

Summary

- Co-packaged optics is promising for next gen fiber optics solution
- Advanced packaging solution are required to enable high performance/integration & small form factor optical engines
- Passive alignment of fiber optical coupling is *promising* for high volume production
- Wafer level optical test is key building block for PIC KGD delivery
- Known good optical engines required to enable high CPO assembly yield
- Extend optical capabilities to new markets for sensing & range finding such as LiDAR, healthcare, and others ...

Thank You

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