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CONNECTS

Heterogeneous Integration for
Connectivity and Sustainability

**3D-RDL & TPV-based Advanced Wafer-Level packaging
Pilot Line for RF applications**

Ayad GHANNAM, CEO - 3DiS Technologies

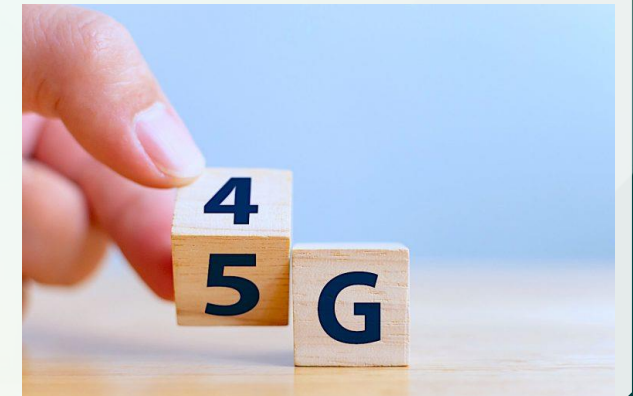
ghannam@3dis-tech.com

RF Frontend, driver of innovation in advanced packaging

Highly integrated and high-performance RF Front-ends relied on advances in silicon technologies

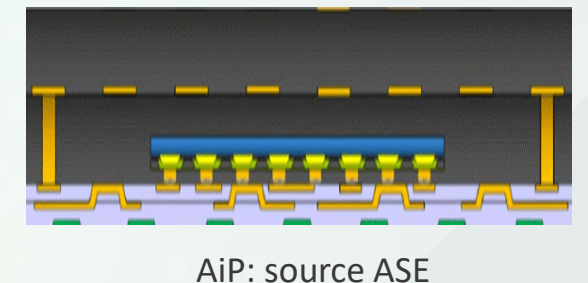
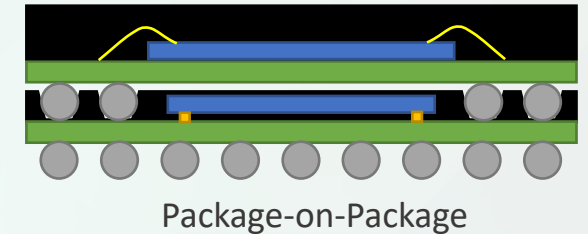
Moore's law benefits approaching their boundaries → Advanced system packaging technology is the answer

- RF front-ends require System-in-Package “SiP” technology
 - Enables 3D integration : more RF bands in small surfaces (smartphone)
 - Improves performance
 - Reduces time-to-market
- 5G/6G are here: Drive innovation in advanced packaging to integrate RF front-end building blocs and antennas in one package



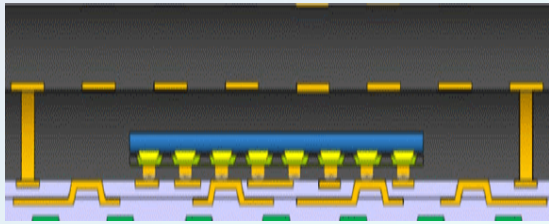
RF Frontend, driver of innovation in advanced packaging

- 5G/6G Frontend SiPs require back-side interconnects or double sided redistribution layers “RDL” for:
 - PoP integration
 - Antenna integration on package “AiP”
 - Creating RF feeds for interfacing with antenna array
- Bringing signal to package backside requires thru-package-vias “TPV” that are either:
 - Laser formed and filled with solder
 - Placed inside the package in form of PCB bar (eWLB)
 - Electroplated using HAR copper pillars or thru-package-vias “TPV”, then grinded after molding (Foundries, OSATs, etc.)
- Current multi-layer RDL & TPV technologies has either high number of processing steps & time, are limited RDL layer count & in aspect-ratio, or not compatible with back-side RDL

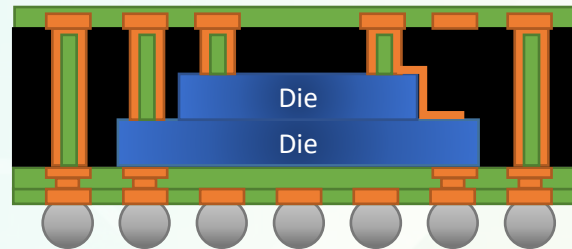


3D-RDL & HDc-TPV platforms: enabler of 3D WLP for RF applications

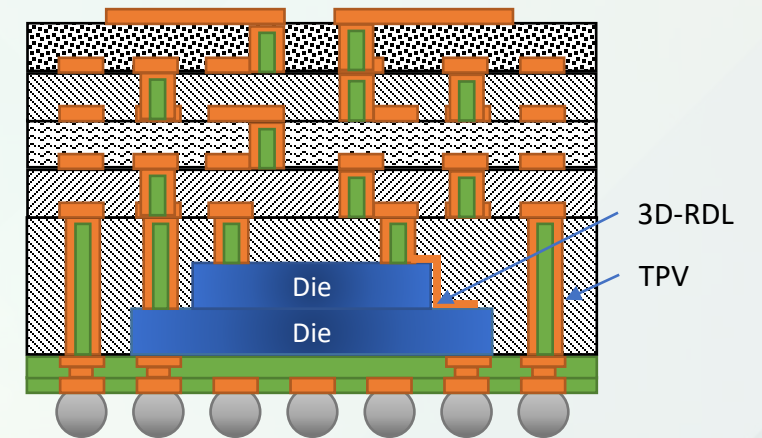
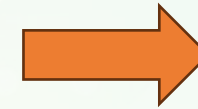
Advancing beyond State-of-the-Art for high-performance advanced wafer-level packaging of RF & mmWave applications



Current State-of-the-Art (2.5D)



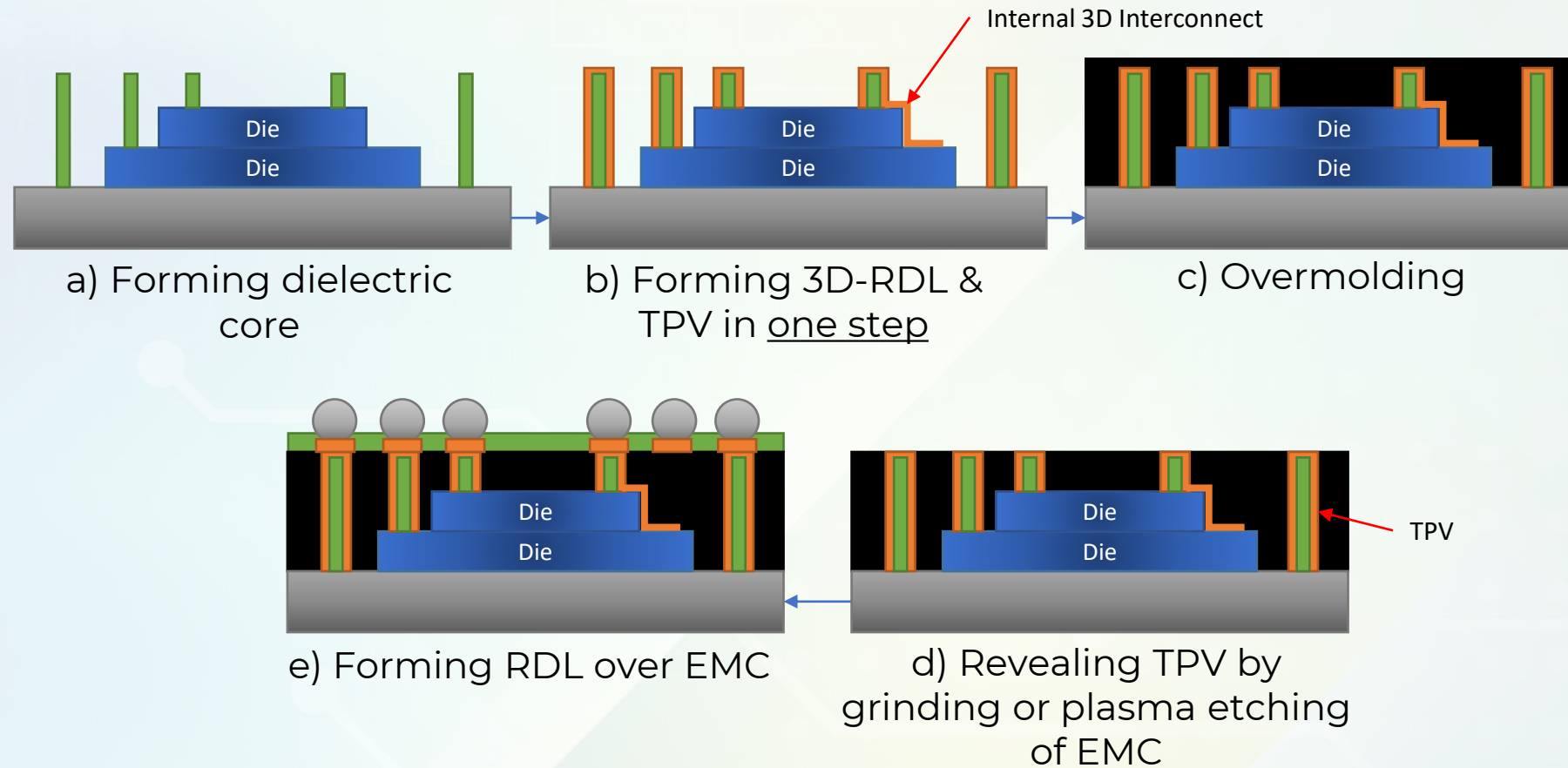
Current State-of-the-Art (3DiS)



Beyond State-of-the-Art (3DiS)

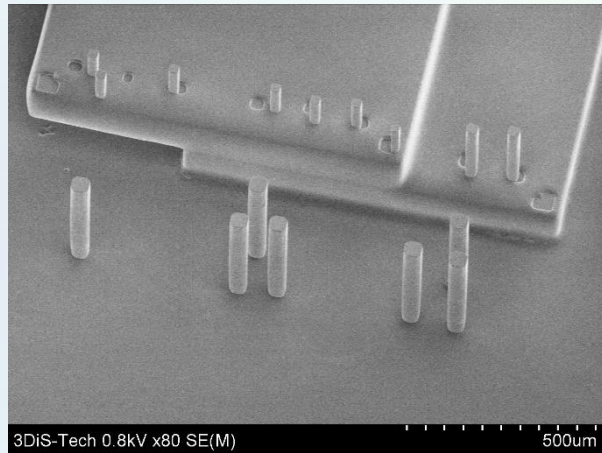
High-Aspect-Ratio dielectric-core TPV “HDc-TPV”

Developed low-cost solution to form HDc-TPV and intra-die connection using 3D-RDL

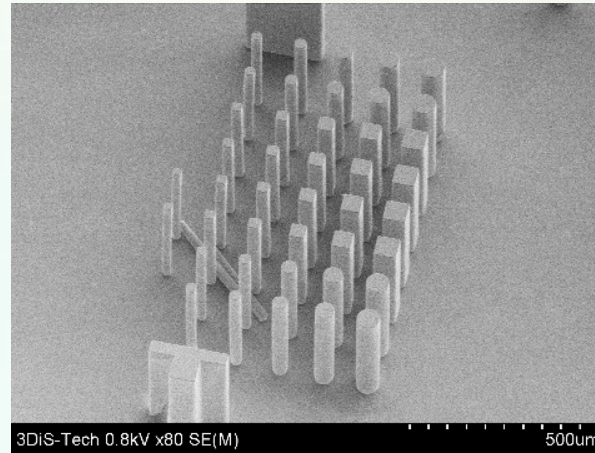


High-Aspect-Ratio dielectric-core TPV “HDc-TPV”

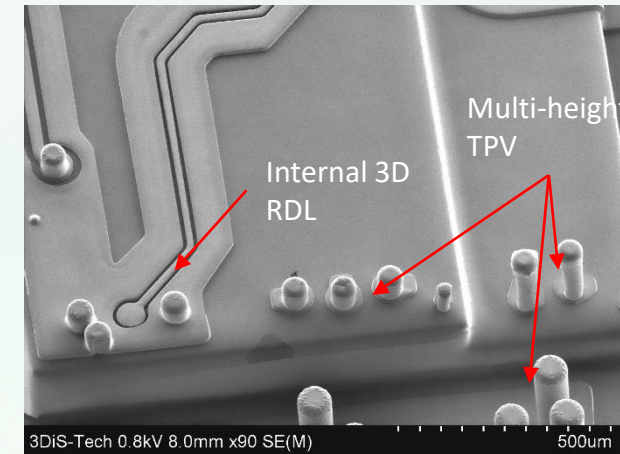
Developed low-cost solution to form HDc-TPV and intra-die connection using 3D-RDL



Dielectric-core pillar



HAR of 10:1 (260um tall)



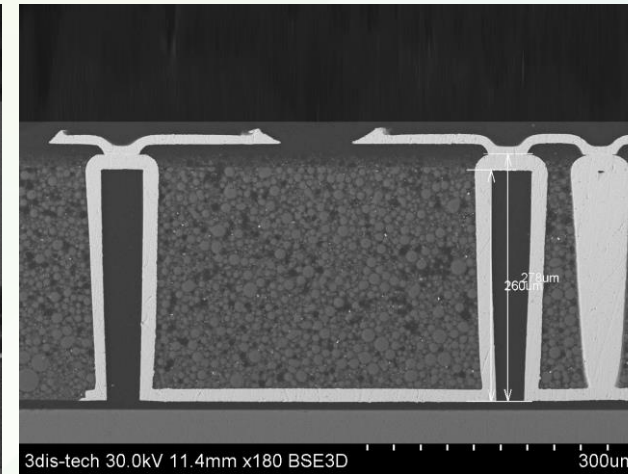
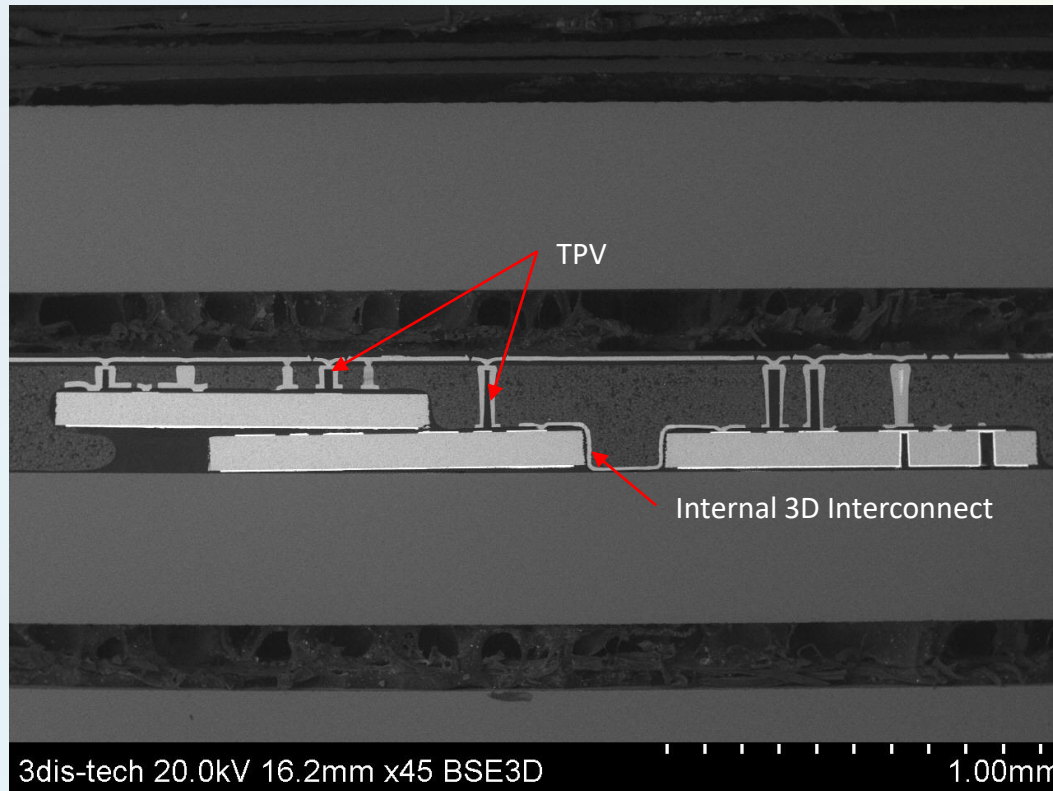
3D-RDL to form interconnects & TPV

- Advantages:
 - Multi-height-independent technology to form TPV
 - HAR for dense & tall TPV
 - Creates 3D internal interconnects / 3D-RDL simultaneously

3D-RDL & HDc-TPV platforms: example RF application

Package having HDc TPV with 3D-RDL on 3D stacked RF system (cross-section)

Previous State-of-the-Art (3DiS)

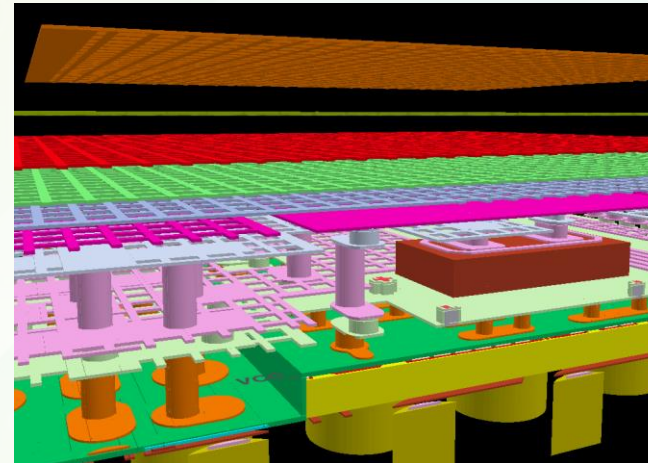
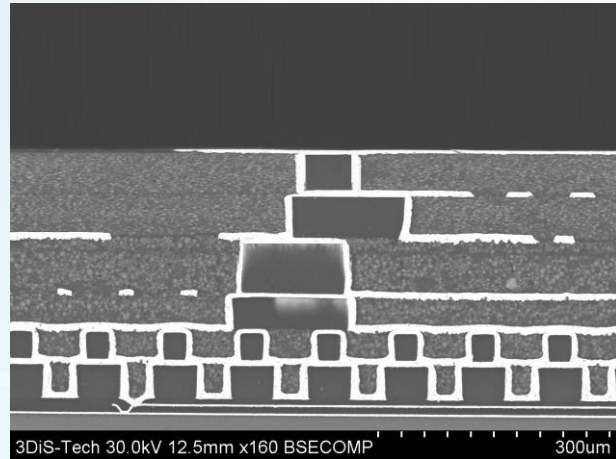


- TPV Height : 270um
- TPV Diameter : 45um
- AR : 6:1

- 3D integration inside the package with **one 3D RDL layer** → cost effective, 3 masks only
- Good 3D copper filling
- Low surface roughness → low RF losses

3D-RDL & HDc-TPV platforms: 3D WLP for mmWave applications

Package having **9+** 3D-RDL with HDc TPV layers (cross-section) ! World first!
Beyond State-of-the-Art (3DiS)



MultiTech in multi layer stack with RF shield

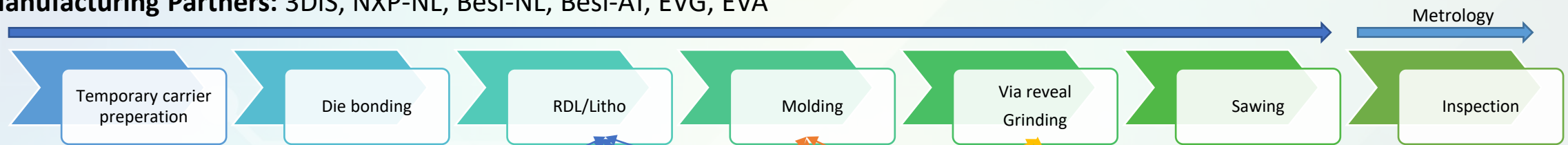
- **Low-loss mmWave** transitions inside the package
- No thermal interface between die and backside RDL
- Technology is been demonstrated on a **large mmWave** package (12+ 3D-RDLs w/TPVs)

3D-RDL & HDc-TPV-based Advanced 3D Packaging Pilot Line

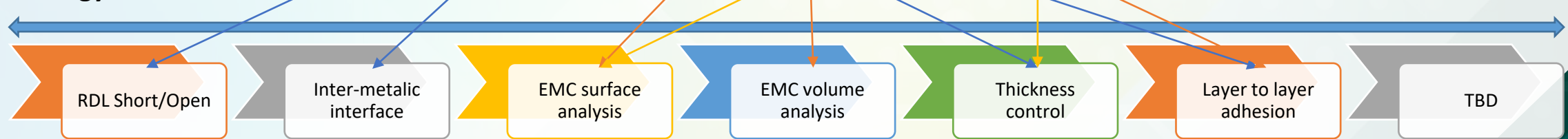
Pilot Line definition & interaction between partners



Manufacturing Partners: 3DiS, NXP-NL, Besi-NL, Besi-AT, EVG, EVA



Metrology Partners: TNO, FBH, DX, HD, AMIL, ICOS, NOVA, BRT, NFI, UPB



Summary

- RF-Frontends are enabler of innovation in advanced 3D packaging
 - Require short, high-performance RF interconnects
 - Need Package-on-Package for smaller footprint
 - Require integrating Antenna-on-Package
- System-in-package technology provides good answer to RF requirements, but needs thru-package-vias and double side RDL. Current TPV solutions are either
 - Not compatible with back-side RDL
 - Have high count of process steps with increased complexity/count for different height TPV
- 3D-RDL Technology coupled to HDc-TPV platform
 - Substrate-less QFN-like and 3D SiP packages
 - Allows bringing contact to package backside using low count of process steps
 - Enables 3D integration inside the package with short 3D interconnections between building blocs
 - Enables hi-performance, 10+ 3D-RDL, 3D FO-WLP for AiP applications
- Developed solutions bring innovation to advanced 3D packaging of RF & mmWave applications

Acknowledgment



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Thank you for your attention!

Dr. Ayad GHANNAM
Founder/CEO

3DiS Technologies
478 rue de la Découverte - CS 67624
31676 Labège FRANCE
E-Mail: aghannam@3dis.tech