

SEMI Europe 2023

QUALITY OF **SmartSiC™** FOR SIC IN AUTOMOTIVE BUSINESS

Emmanuel SABONNADIÈRE, SVP Automotive & Industrial

Munich - November 16th, 2023

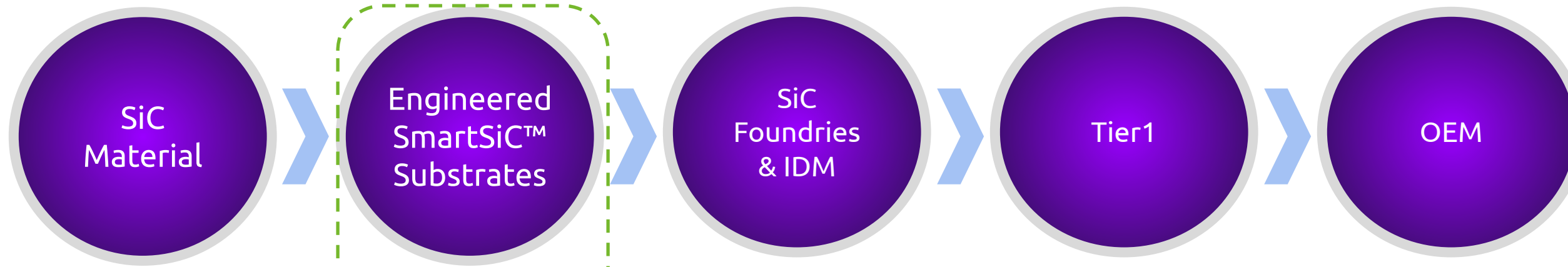
01

Soitec & SmartSiC update

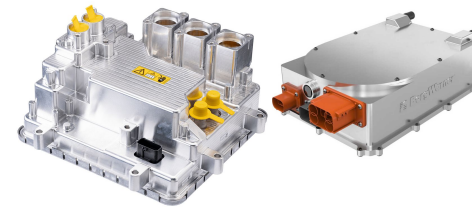
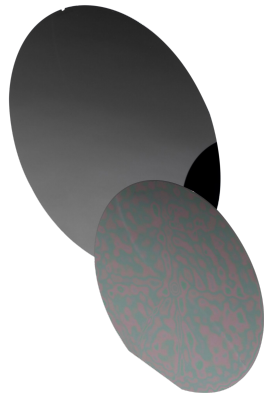
An essential material for the
success of the EV revolution

SmartSiC™, KEY FOR NEW SiC-BASED POWER ELECTRONICS

SOITEC IS A PURE-PLAYER ENGINEERED SUBSTRATE SUPPLIER

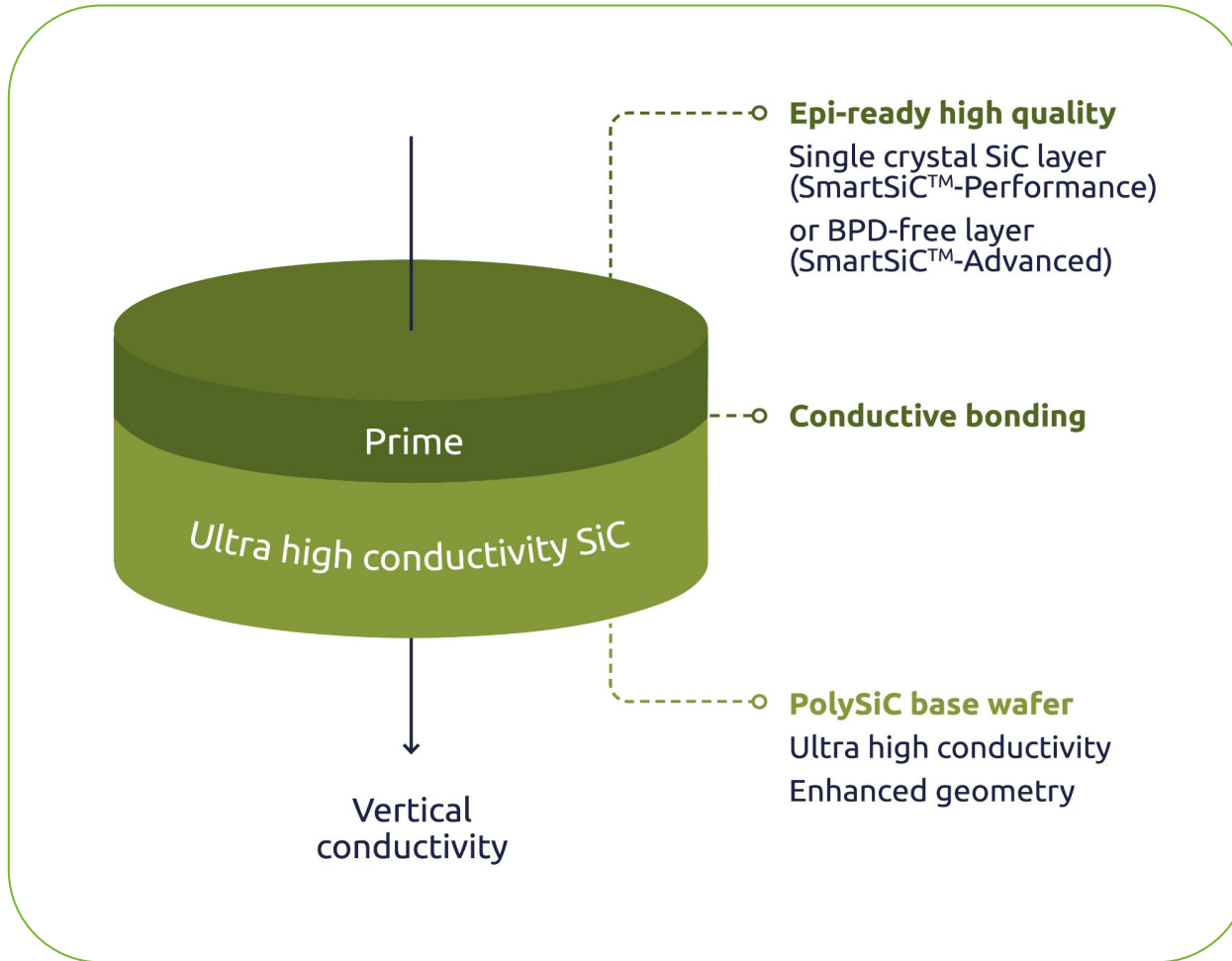


soitec



SmartSiC™ ENGINEERED SUBSTRATE

UNRIVALED VALUE PROPOSITION TO ENABLE SiC ACCELERATION



UNRIVALED VALUE PROPOSITION

>10x

Single crystal SiC
wafer
re-usability

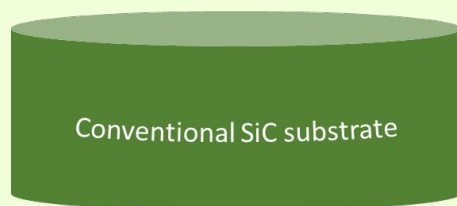
~8x

Poly Crystal SiC
wafer
higher conductivity

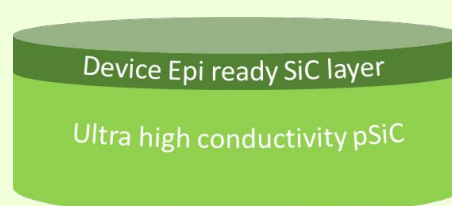
SmartSiC™, THE ENABLER FOR IMPROVED DEVICE PERFORMANCE

FIELD RESULTS BACKING VALUE PROPOSITION

LOWER SUBSTRATE $R_{ON} \cdot A$



180μm



Standard SiC substrate

SmartSiC™ substrate

mSiC
20mΩ.cm

Substrate

pSiC
2.5mΩ.cm Interface
10μΩ.cm²

100 μΩ.cm²

BS metal contact

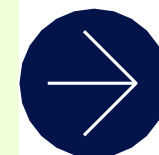
5μΩ.cm²

460μΩ.cm²

Total $R_{Subs} \cdot A$

60μΩ.cm²

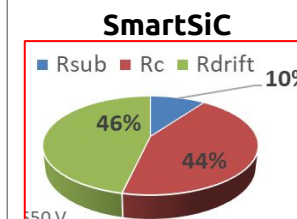
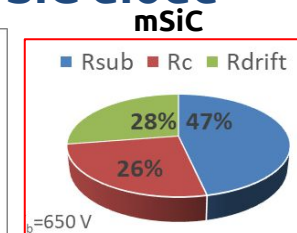
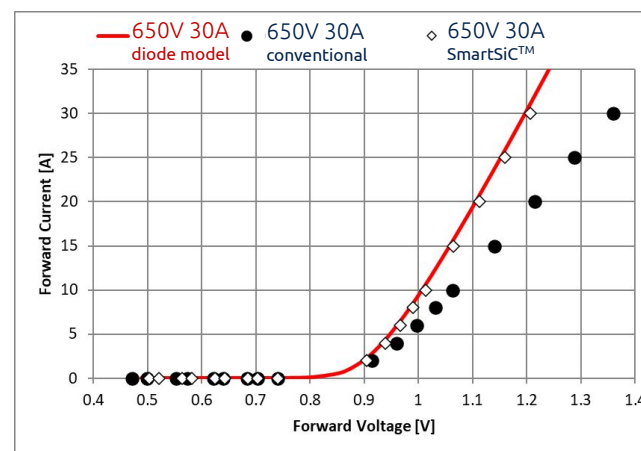
SmartSiC™ reduces the substrate contribution by 8x



VALUE PROPOSITION

- High increase of number of producible wafers
- Maximize substrate value
- Higher manufacturing yield
- Device feature size reduction / R_{DSon} improvement
- Copy & paste of MOSFET process flow
- Acceleration of the path to 200mm transition

Experimental data on 650V SiC diode

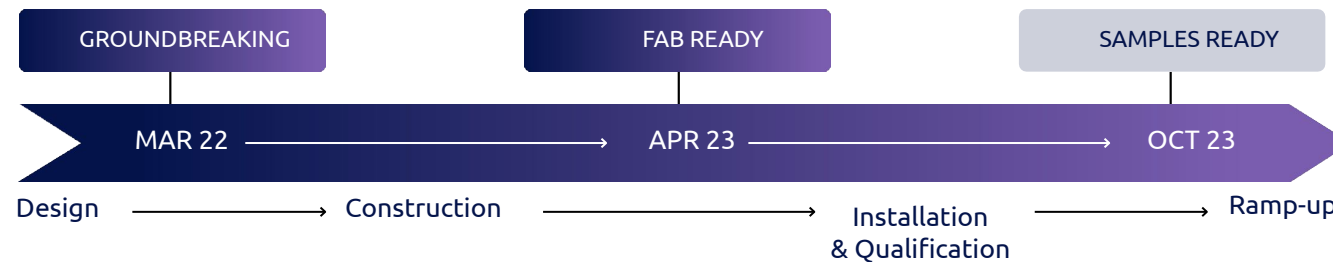


V_f gain at rated current (30A): 150mV over 1.35 => 11% gain
 ΔR @ RT = 30mOhm*mm²

Courtesy of STMicroelectronics, ICSCRM 2023

SmartSiC™ HVM FACTORY

NEW CLEANROOM FOR SmartSiC™ 500kwpy 150/200mm CAPACITY



02

Demonstrated Quality

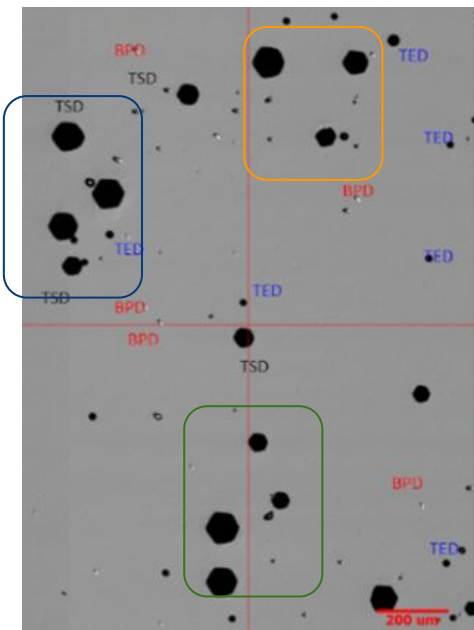
Steps of maturity of the
technology

SmartSiC™, NO CRYSTAL DEFECTS ADDED

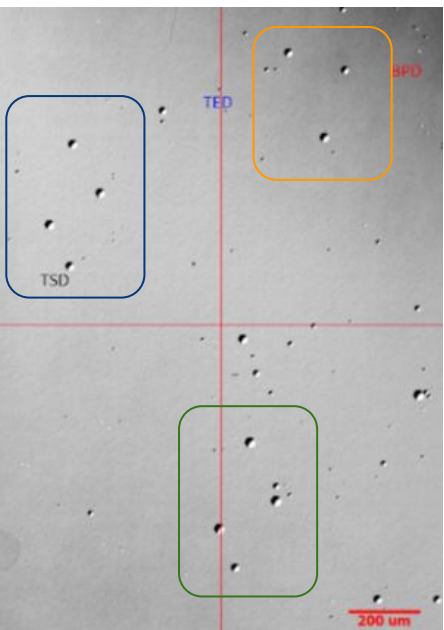
EQUAL OR BETTER QUALITY THAN mSiC

KOH etching and Sica inspection on Bulk 4H-SiC versus SmartSiC™

Bulk 4H-SiC post KOH etching & Na₂O₂
+ Sica inspection



SmartSiC™ post KOH etching
+ Sica inspection



Site to site
comparison

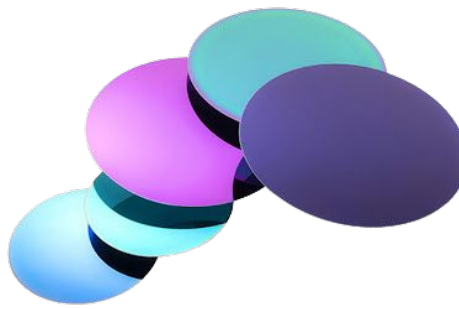
KOH etching support provided by
Japanese Fine Ceramics Center

+ SmartSiC

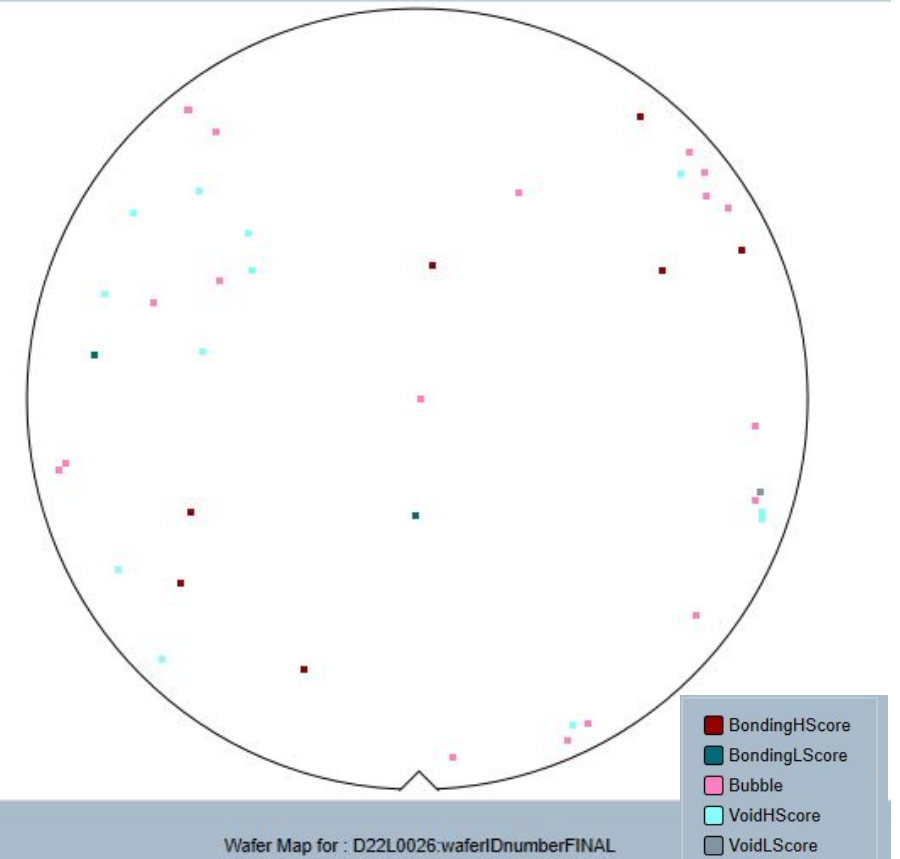
Substrate	mSiC bulk "Donor"	Gen1.2	Gen2.2
TxD density (/cm ²)	~ 4000	~ 4000	~ 4000
BPD density (/cm ²)	~ 500	~ 500	~ 0

+ Epi + SmartSiC

SmartSiC™, AN SOI LOOK... BUT IN SILICON CARBIDE

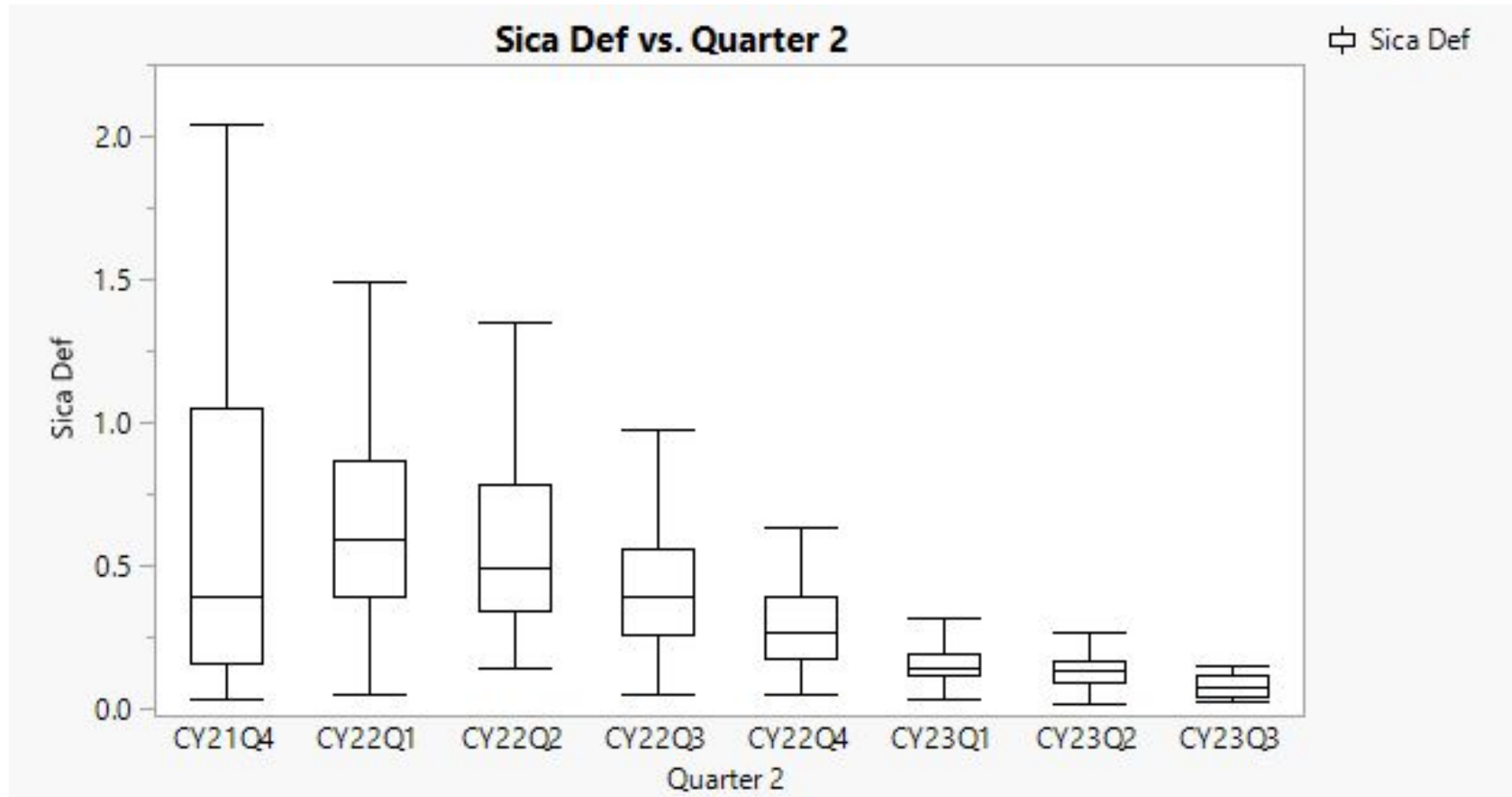


Wafer Map by Defect Class



SmartSiC™, FAST LEARNING CYCLE - 1/2

READY FOR HVM

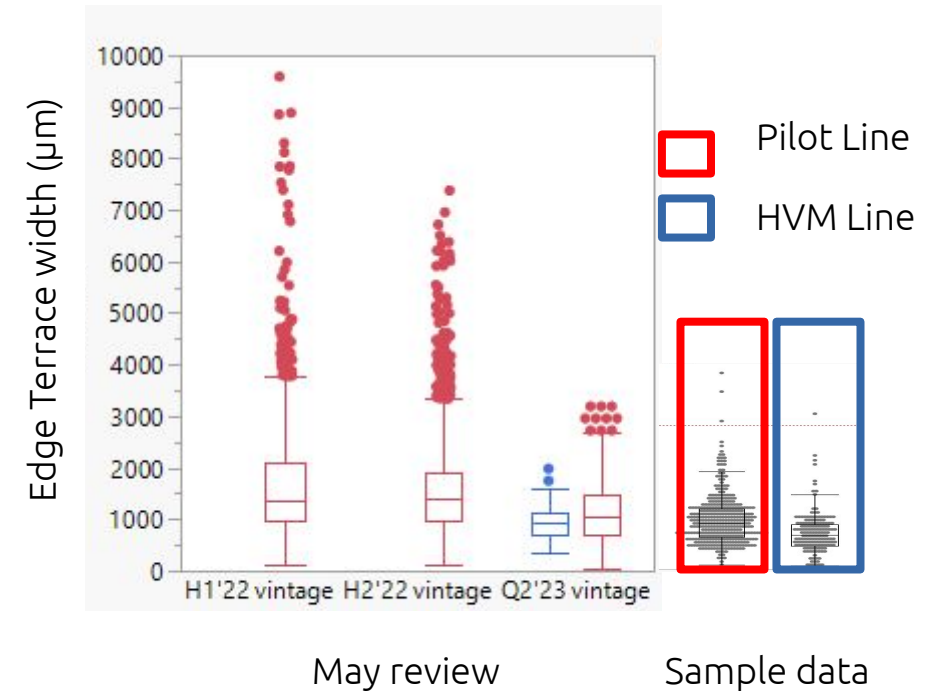


SmartSiC™, FAST LEARNING CYCLE - 2/2

READY FOR HVM

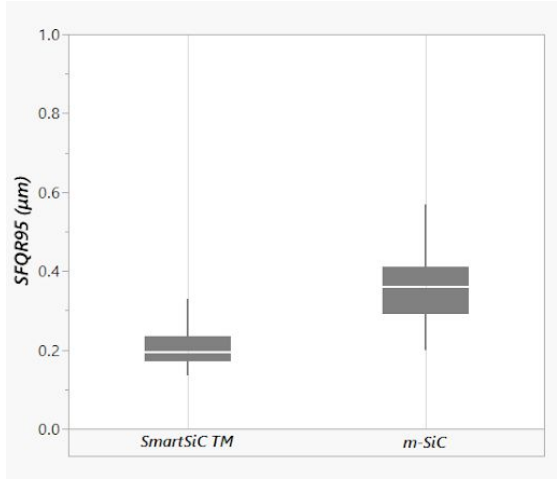
Edge Terrace Under CIP

- Edge Terrace width related to
 - Edge shape from donor & handle wafer
 - Bonding & splitting process
- Edge exclusion width reduction target Q1CY24
 - New pSiC preparation
 - < 3mm edge terrace compatible with EE specification

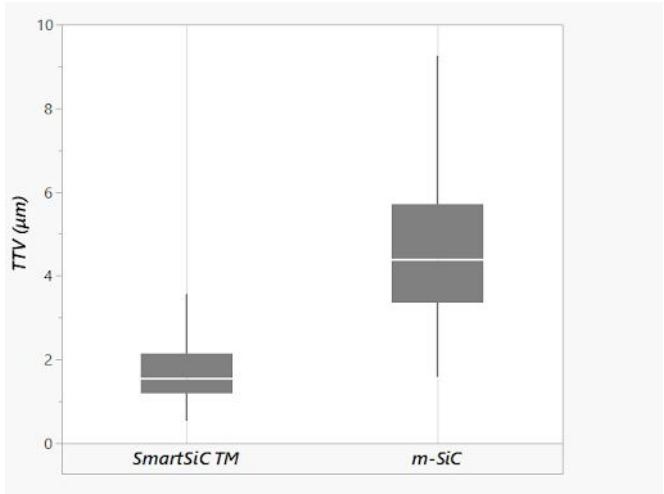
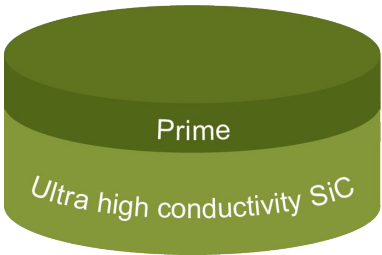


SmartSiC™, A ROBUST TECHNOLOGY

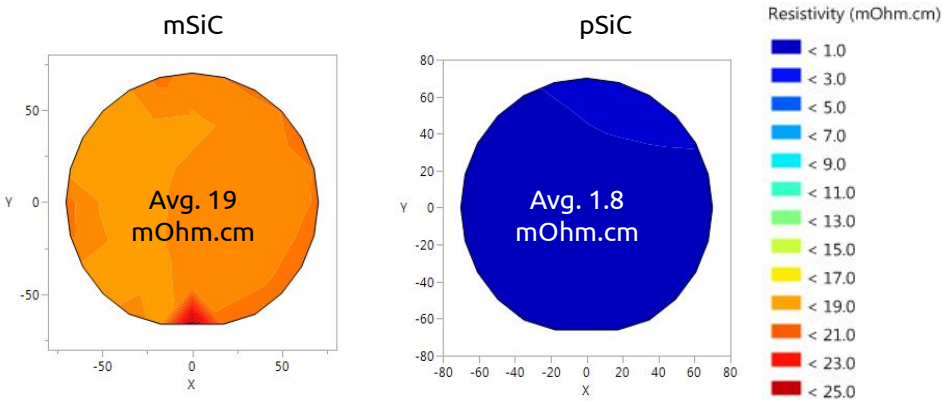
CONTROLLED AND STABLE KEY PARAMETERS



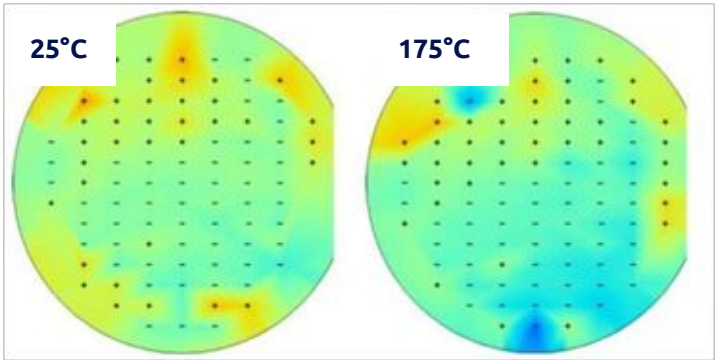
IMPROVED SFQR - PSiC HANDLE



IMPROVED TTV - PSiC HANDLE



VERY LOW AND UNIFORM RESISTIVITY - PSiC HANDLE

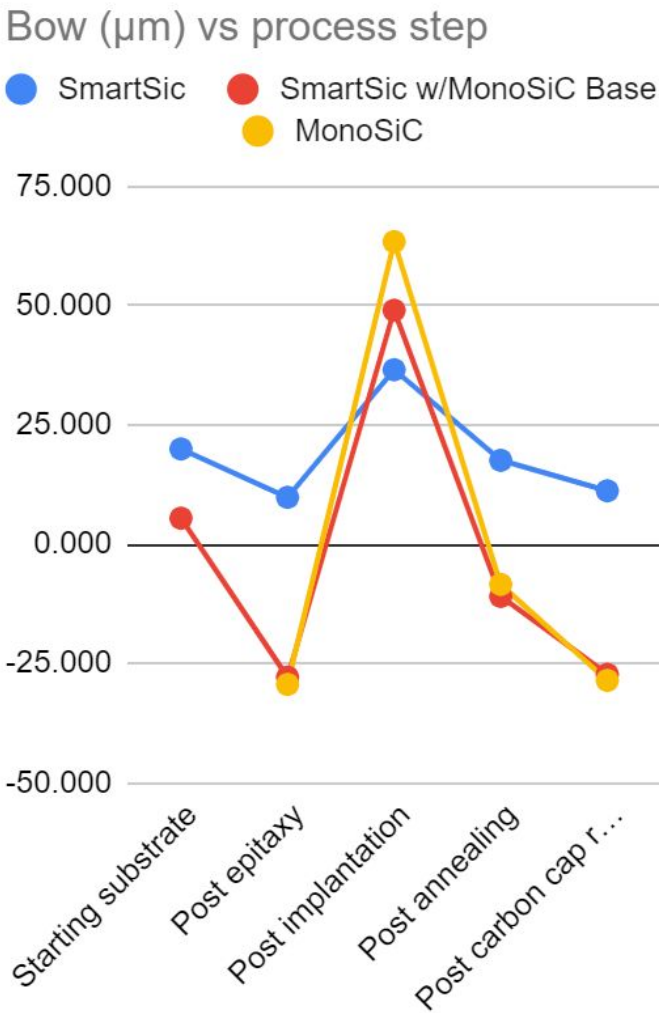
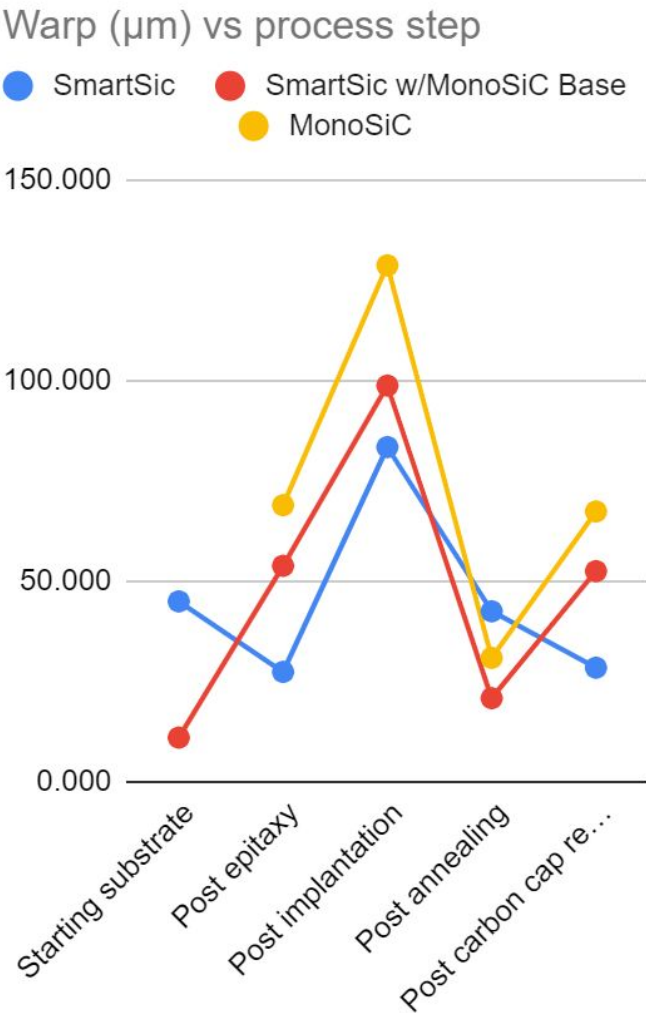
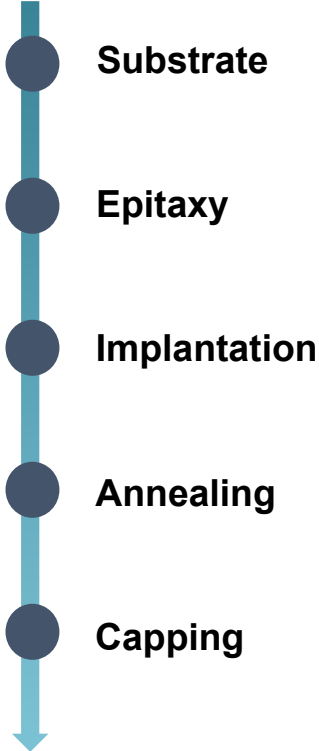


BONDING INTERFACE [mOhm.cm²]

SmartSiC™, PROCESS INTEGRATION

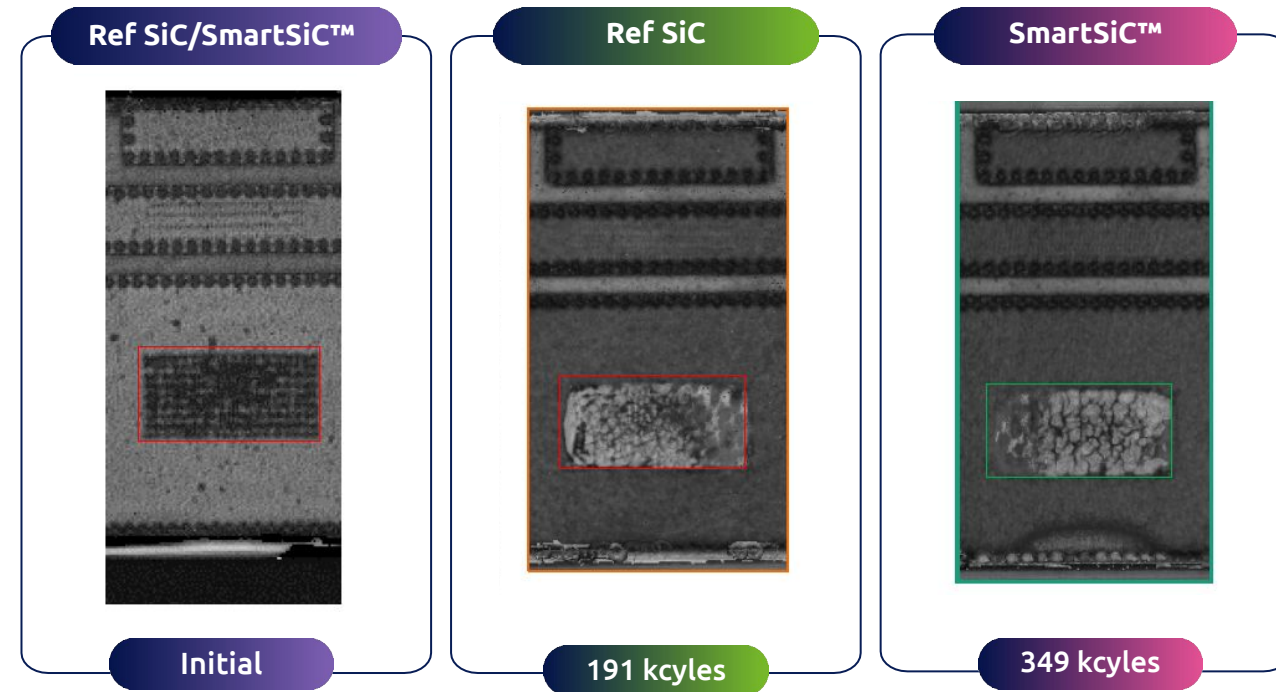
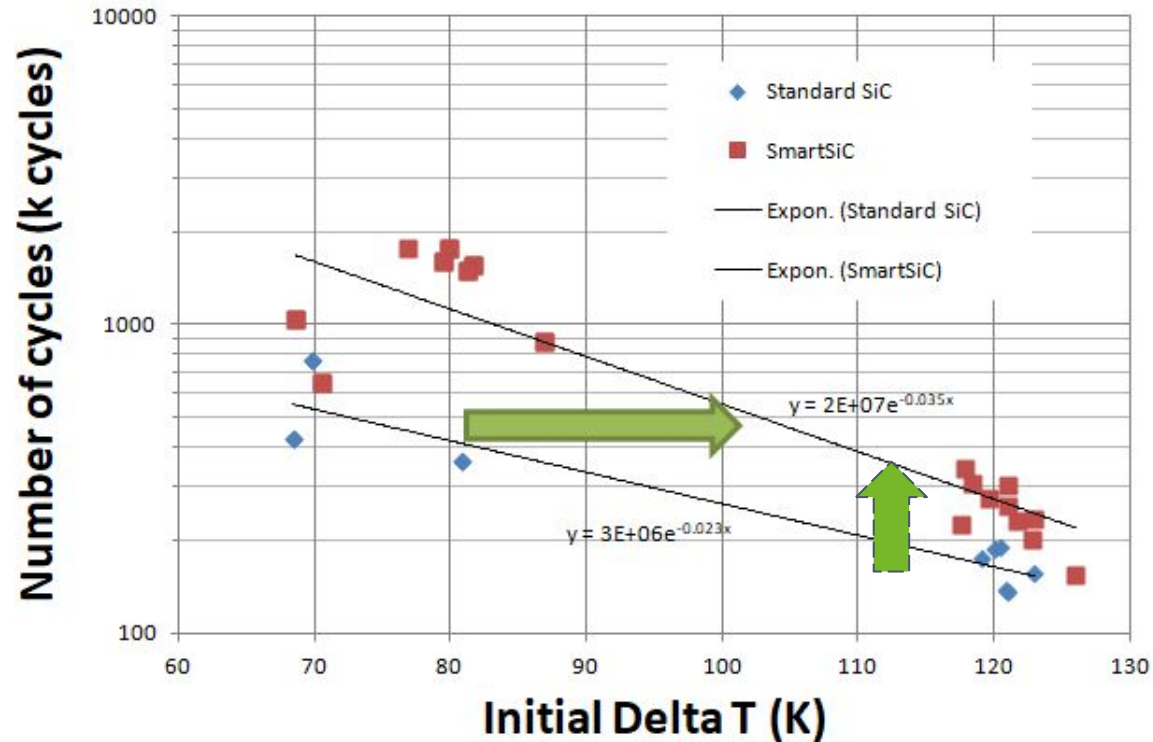
OUTSTANDING GEOMETRY STABILITY

Courtesy of IME Singapore



SmartSiC™, IMPROVED RELIABILITY

DEMONSTRATED THROUGH POWER CYCLING TESTS



Scanning Acoustic Microscope (SAM) Images

SmartSiC™ with silver sintering die attach: **lifetime x2 or 20K higher temperature swing**

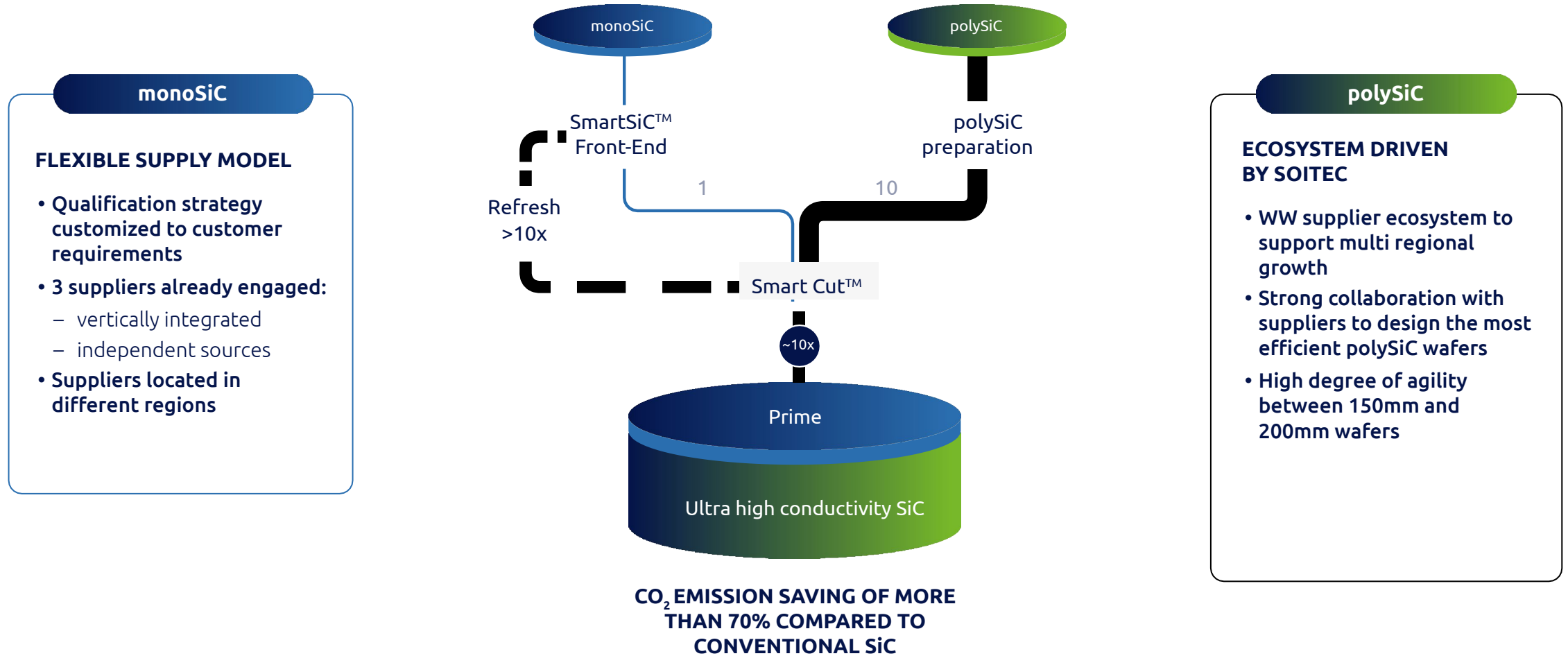
03

Robust Supply Chain

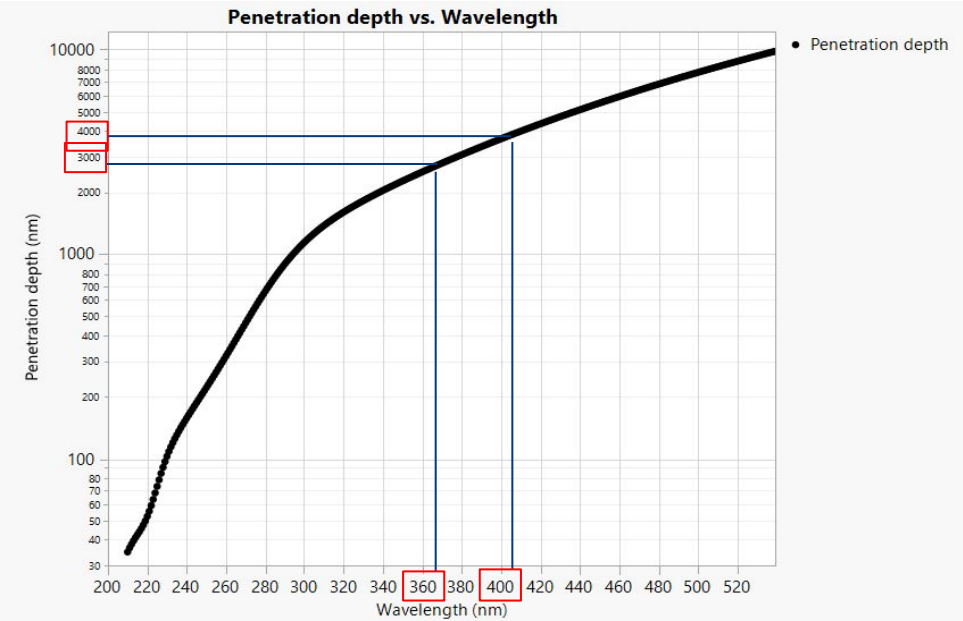
Steps of maturity of the technology

SmartSiC™, SECURED SUPPLY CHAIN

SUSTAINABLE AND AGILE

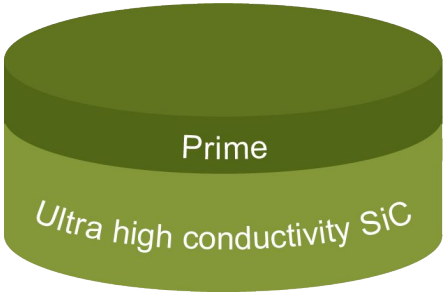


SmartSiC™ Specific Inspection Methodology

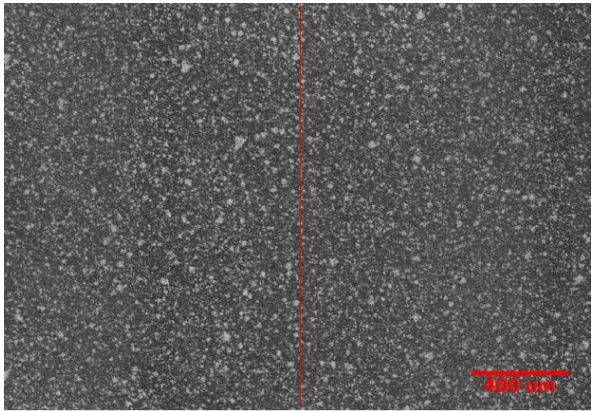


Candela Wavelength : 405nm, 630nm
SICA Lasertech Wavelength: 313nm, 365nm

SmartSiC™



- Smart Cut monoSiC layer is < 1 μm
- SICA inspection is detecting the polySiC through the top layer



SICA monoSiC recipe will see the pSiC base surface

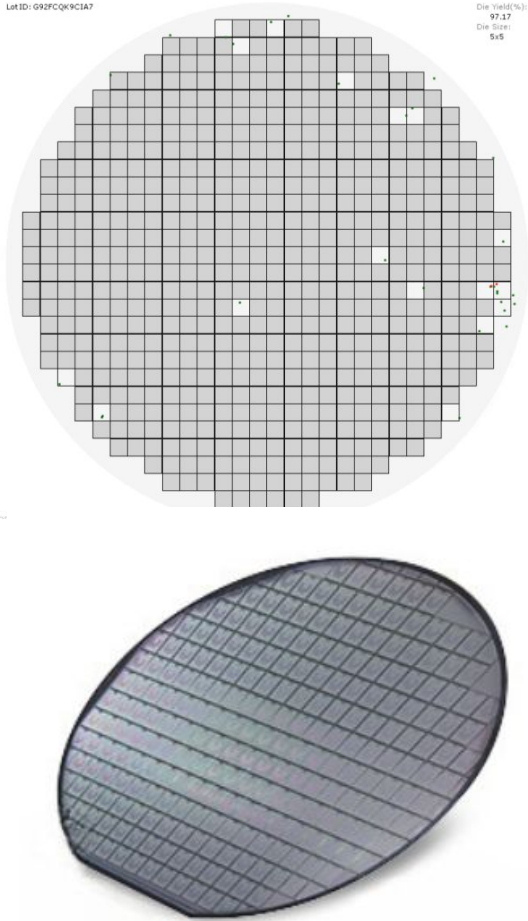


SmartSiC™ ENABLES MORE GOOD DIE/WAFER

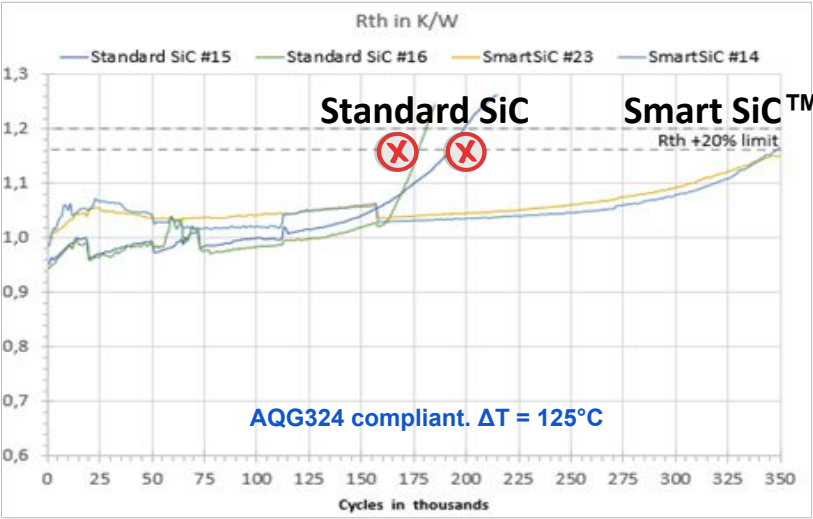
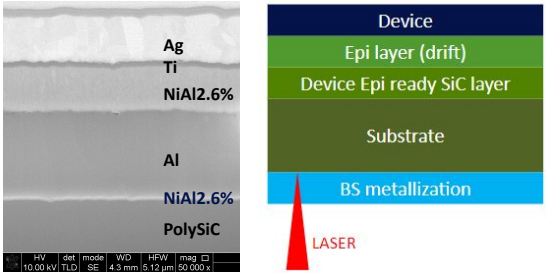
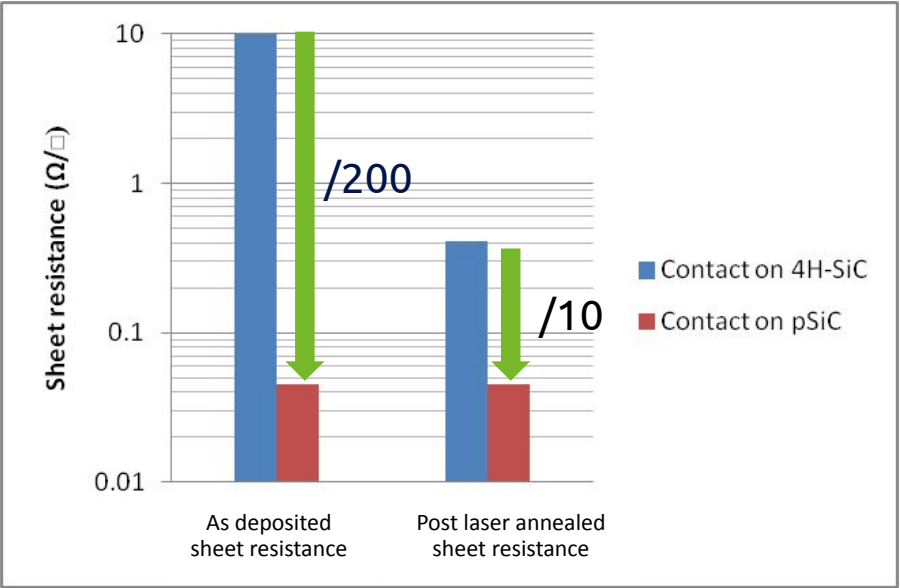
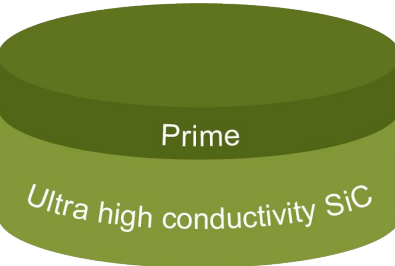
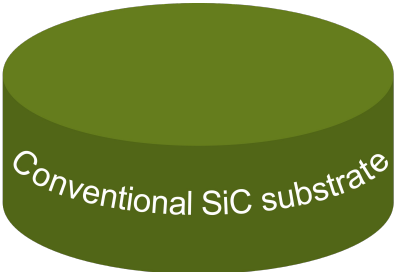
(For 200mm wafer)	Constant Ron redesign MOSFET 1200V		
	Single Crystal SiC	SmartSiC™	Gain
Initial die size	25mm²	21.3mm²	+15%
Gross Die / Wafer	1108*	1313*	+18%*
Yield	70% by 2024	74% by 2024	+4 % by 2024
Good Die / Wafer	776 by 2024	969 by 2024	+25% by 2024

* 3mm EE and 80µm scribe lanes

IMPROVED Ron.A AT THE ORIGIN OF IMPROVED PRODUCTIVITY by 25%



Backside Ohmic Contact without Laser Annealing

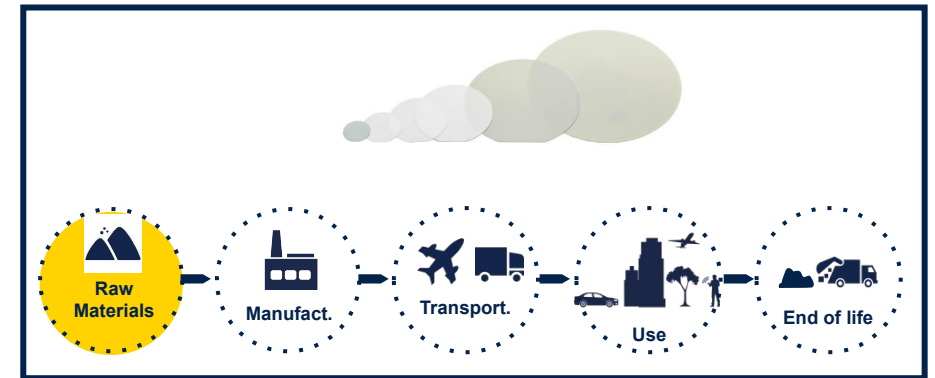
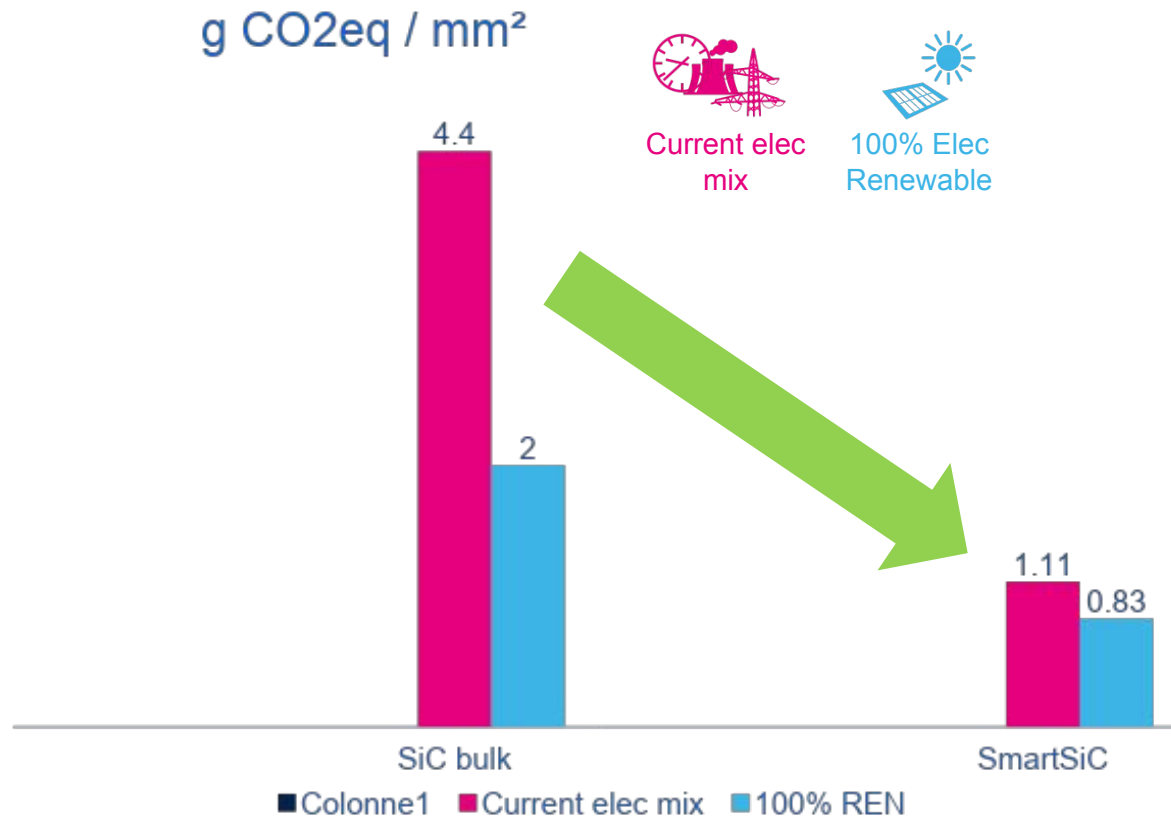


Back side sheet resistance on pSiC 10x lower w/o anneal
Validated through PCsec spec (AQG324) up to 300k+ cycles (w/o back side metal annealing)



SmartSiC™, A MORE SUSTAINABLE CHOICE

DIVIDING BY 4 THE CO₂ EMISSIONS TO MANUFACTURE A SIC WAFER



- Carbon emissions for wafers production following a life cycle analysis protocol
- Normalized results per mm² based on current and future electrical mix, and manufacturing data

SmartSiC™, FOR AUTOMOTIVE & INDUSTRIAL POISED TO BECOME A STANDARD IN EV's POWERTRAIN



Auto SmartSiC™, A DISRUPTIVE SOLUTION FOR LARGER SiC ADOPTION



xEV & Charging Infrastructure



Industrial



Renewable Energy

Auto SmartSiC™, A NEW PARADIGM FOR DEVICE PERFORMANCE AND PRODUCTIVITY

Greener

1/4th

the CO2 footprint
of standard SiC
wafers

Faster

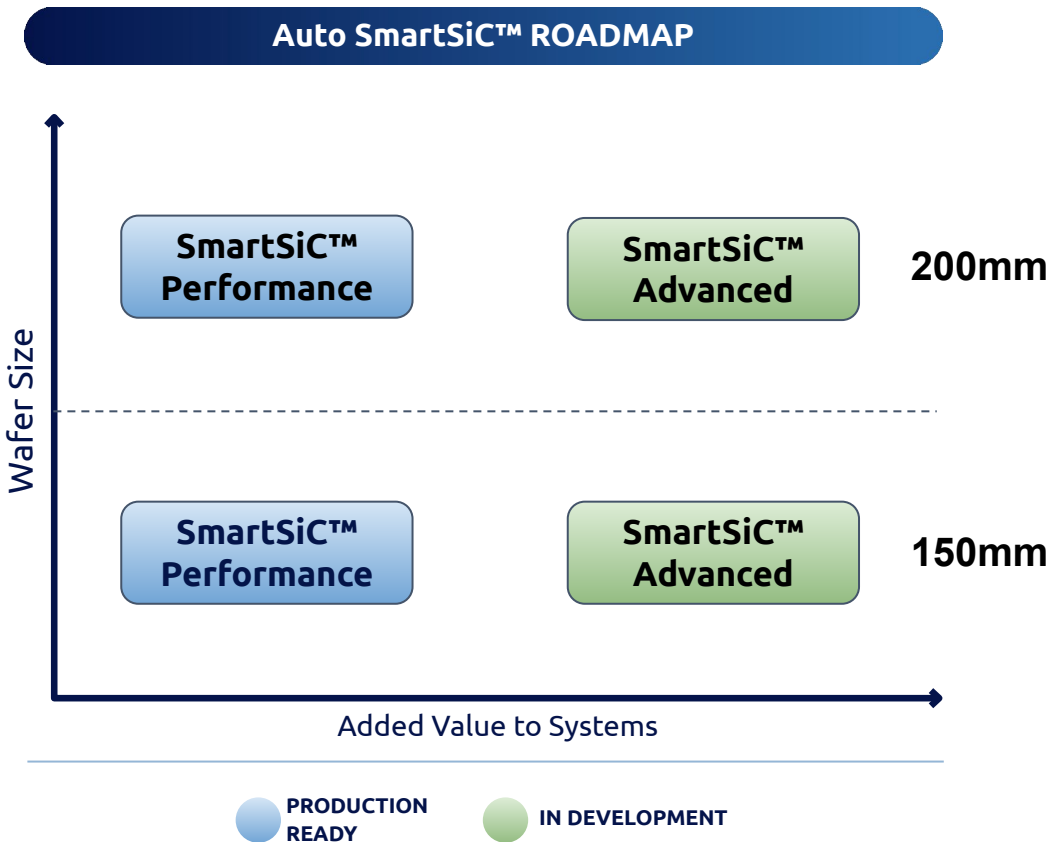
2-year

Acceleration of
mass deployment
of 200mm SiC
wafers

Better

20%

Higher power
density, enabling
more compact,
lighter and less
costly systems





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