



Chiplets - Accelerating System Innovation The Era Heterogeneous Integration

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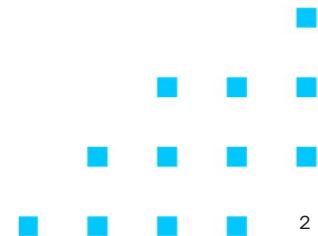
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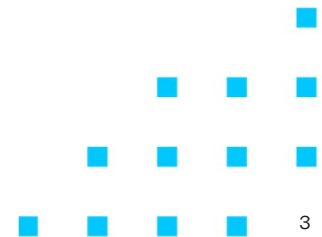
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Outline

- New Silicon Paradigms & Heterogenous Integration
- The Motivations for a Change
- The Aftermath
- How Intel Foundry Services plans its Contribution



Moore's Predicted "Day of Reckoning"

System on Chip -> System of Chips

"It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected¹."

-Gordon E. Moore

¹: "Cramming more components onto integrated circuits", Electronics, Volume 38, Number 8, April 19, 1965

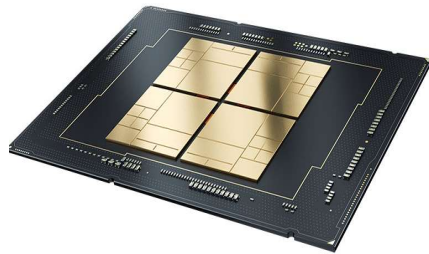


Image: Intel®



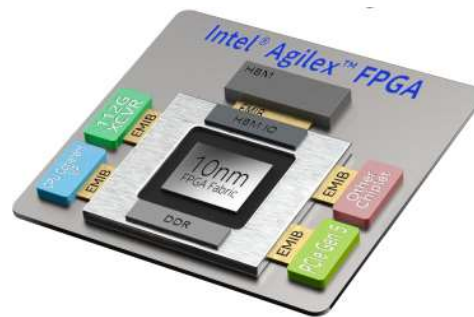
What is a Chiplet?

A physical IP block designed to integrate with other chiplets through **package level integration** and **standardized interfaces**



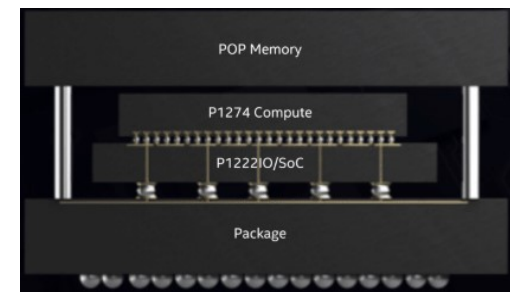
Sapphire Rapids

Source: Arch Day 2021



Agilex/EMiB

Source: Intel/Altera

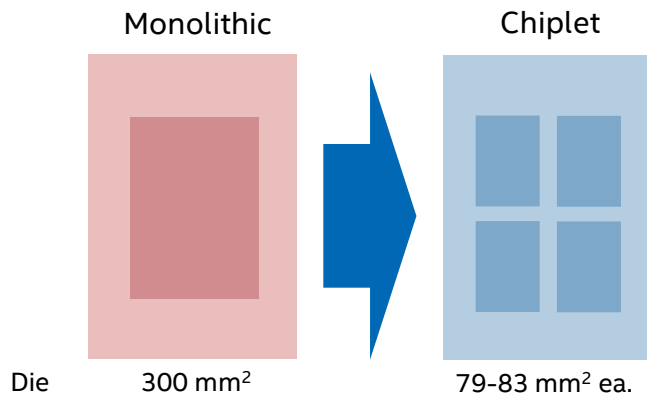


Lakefield/Foveros

Source: Intel

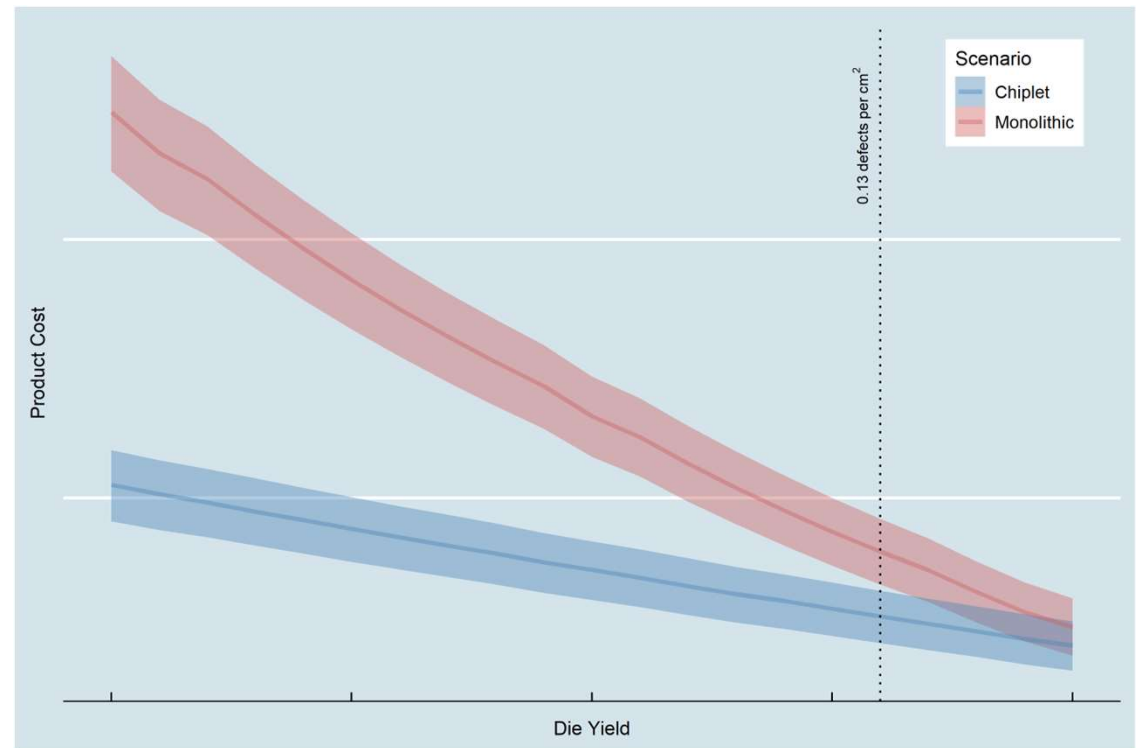
Our vision is to create competitive products with greater functionality,
improved agility, and faster time to market

Motivation: Cost & Manufacturing Optimization



Input Variables:

- Die Area
- # of Chiplets
- Wafer Cost
- Defect Density
- Package/Assembly/Test
- Known Good Die
- Die Area Tax & Overhead



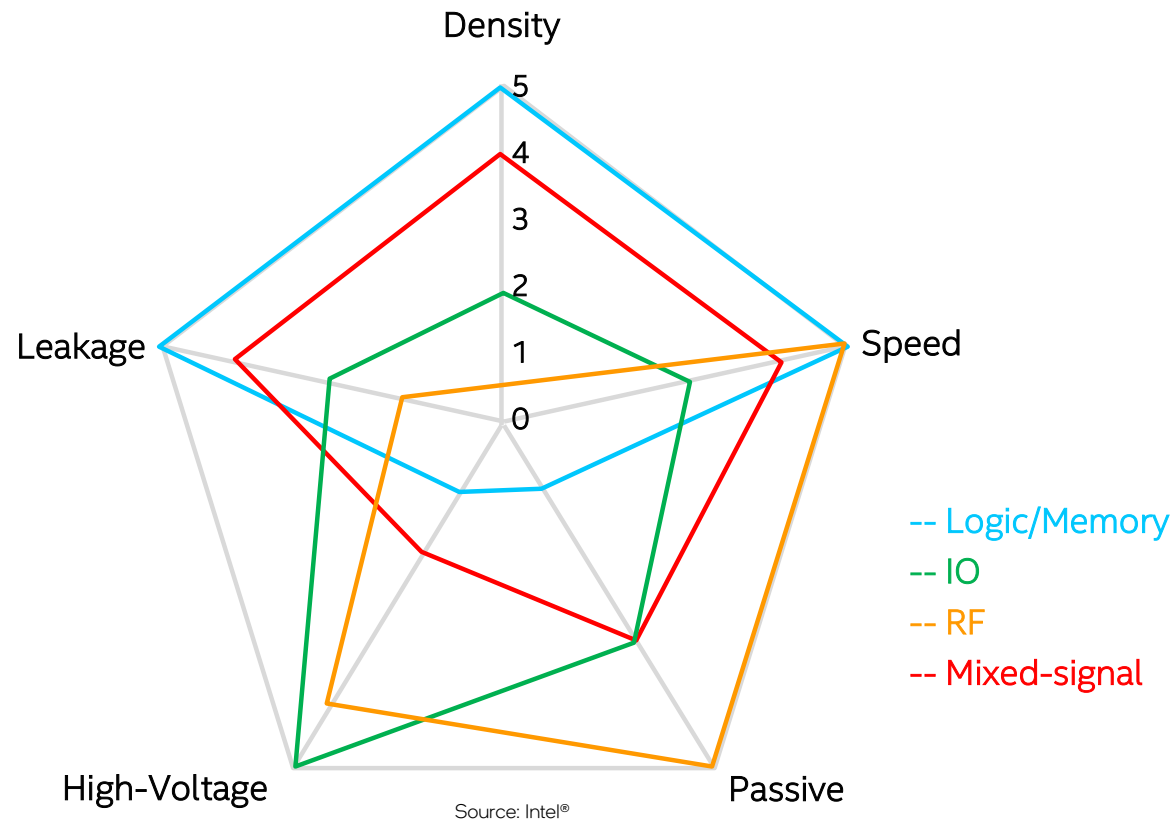
*Probabilistic trend by 1std dev

Source: Intel® Model

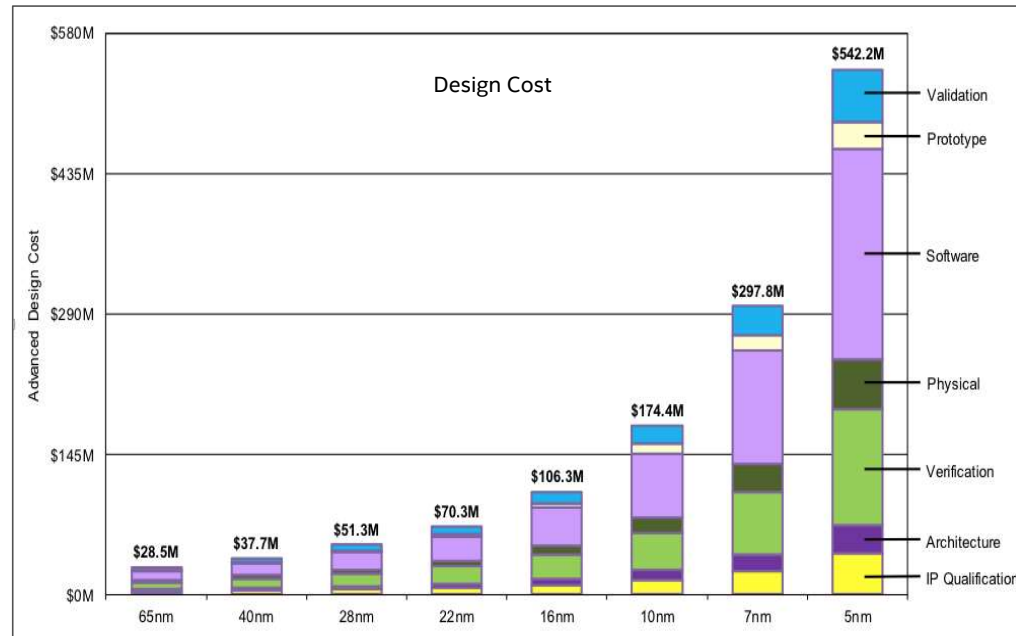
Reference: <https://ieeexplore.ieee.org/document/9758914>

"Heterogeneous Integration of Chiplets: Cost and Yield Tradeoff Analysis"

Motivation: Process Technology Optimization



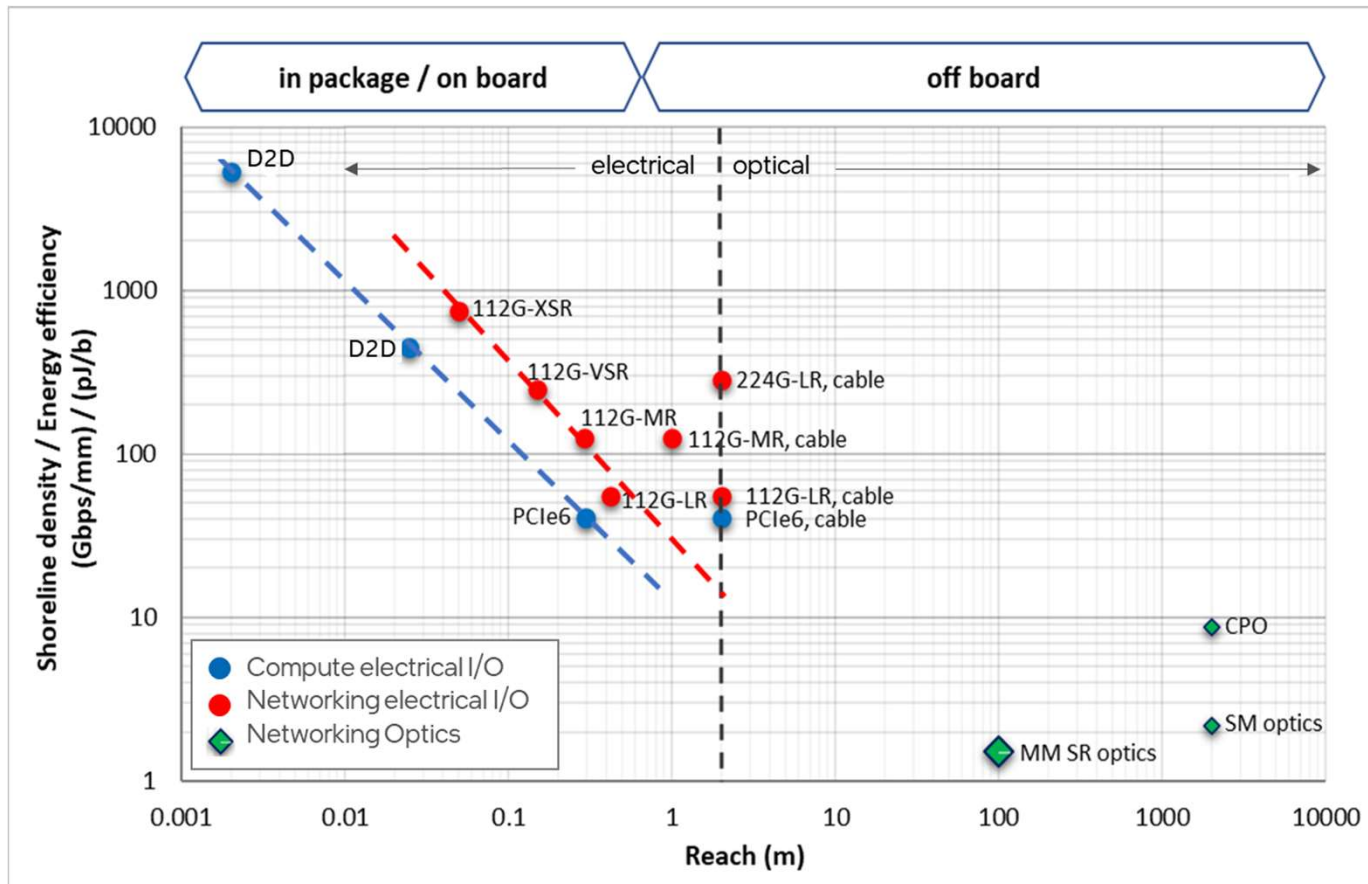
Motivation: R&D Cost and Product Velocity



Source: Lapadeus, M., "Big Trouble At 3nm", Semiconductor Engineering, June 21, 2018
cited in IEEE Heterogeneous Integration Roadmap
https://eps.ieee.org/images/files/HIR_2020/ch02_hpc_1.pdf

Move from Exponential -> Linear with modularity and reuse

Motivation: Optimize System Level High Speed IO



Source: Intel®

Collaboration in Silicon Development

- Gap in expectations:
 - System Performance Optimization
 - Future-proof System
 - Control on Quality and Safety Levels
 - Control on Sourcing along the Supply-chain
 - Cost
- Way to go
 - ➔ Collaboration, Leverage Synergies along Supply Chain
 - ➔ Engagement on Standards and Platforms to Mitigate Challenges



Mega Trends Driving System Foundry Need

Super-powers driving workload diversity and new customers

Super-powers

Ubiquitous Compute



Cloud to Edge Infrastructure



Pervasive Connectivity



Sensing



Artificial Intelligence



New advanced node customers



CSP

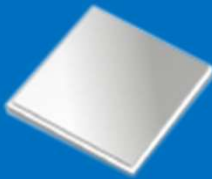


Auto OEM & Tiers



MAG

Industry moving from System on Chip (SoC) to System in Package (SIP)



System on Chip

- 1 die, 1 process node
- Limited diversity of chips in a system

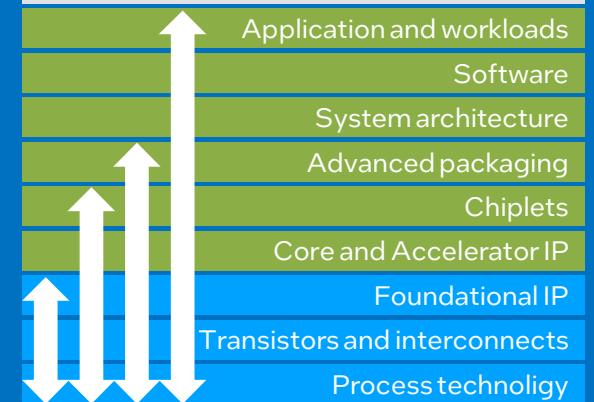


System in Package

- X die, Y process nodes
- Extreme diversity of chips in a system

Industry must evolve optimization from design (DTCO) to system level (STCO) co-optimization

System co-optimization hierarchy

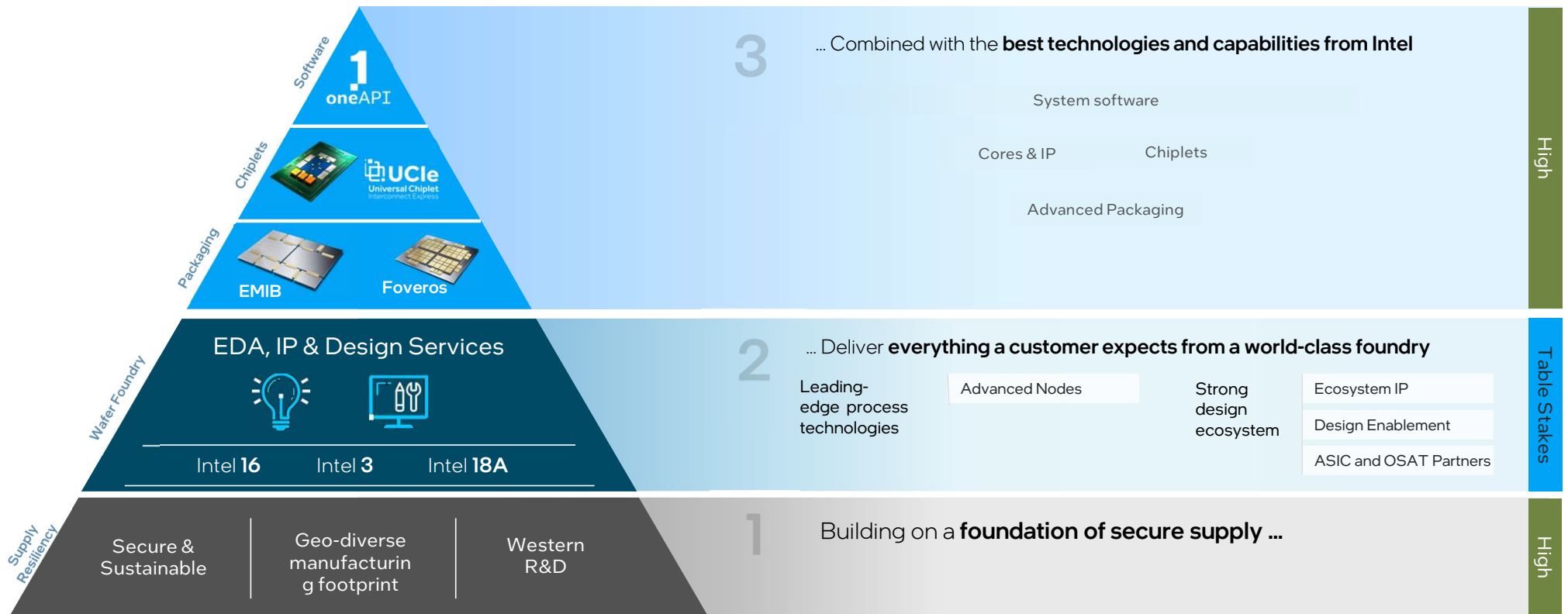


Unique to Intel among foundries

Foundry table stakes

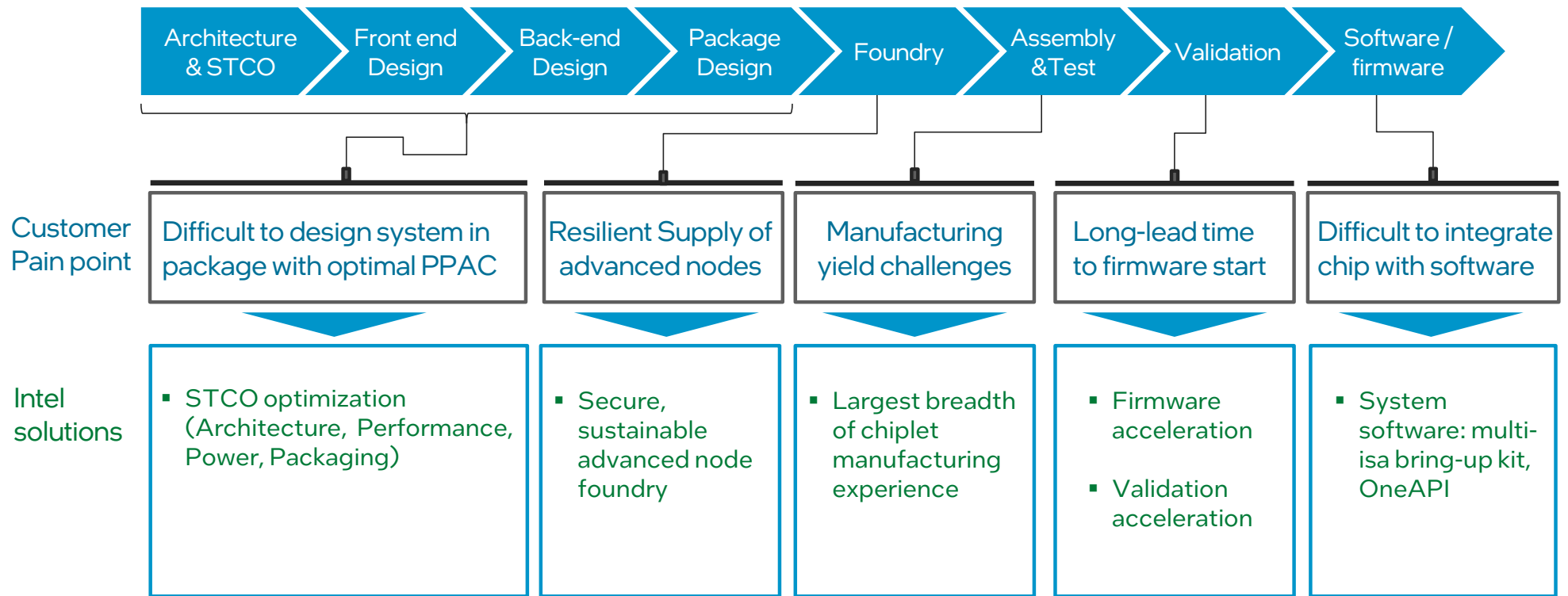
Intel Foundry Services - The Open System Foundry

Intel
differentiation



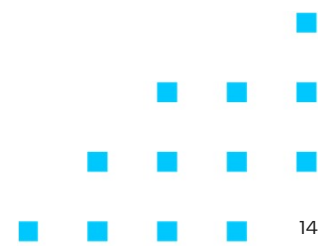
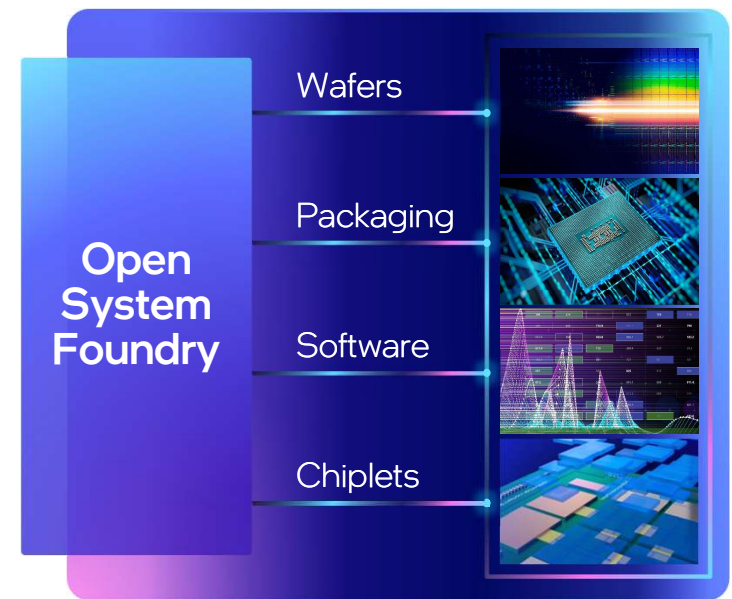
Customer Pain Points & IFS solutions

Difficult to design for optimal PPAC, manufacture with high yield, and longer time to market - Intel can help



Summary

- The Chiplet R-Evolution is here
- Technical Challenges:
 - R&D, Interop, Die size, Process, I/O
- Support Needed – EDA and CAD tools
 - Architecture, Design, Debug & Test
- It's just the beginning...
...let's collaborate with IFS ecosystem

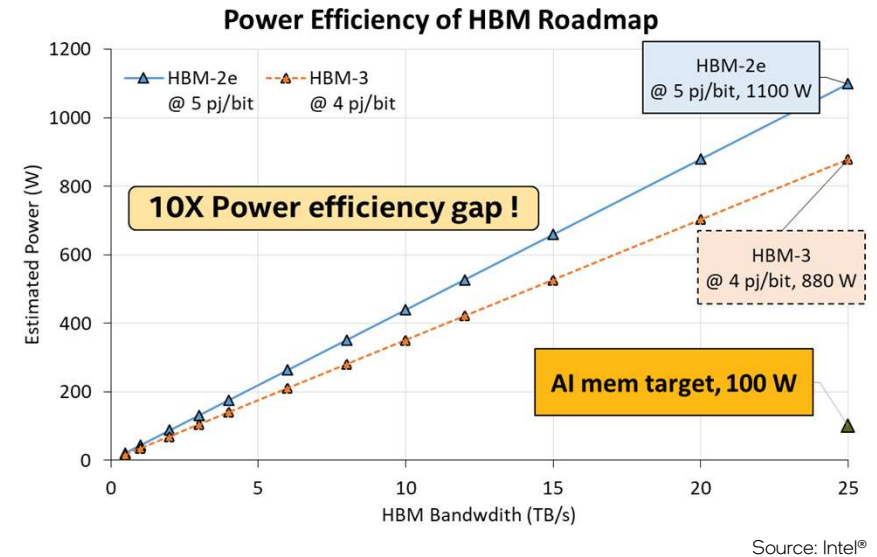
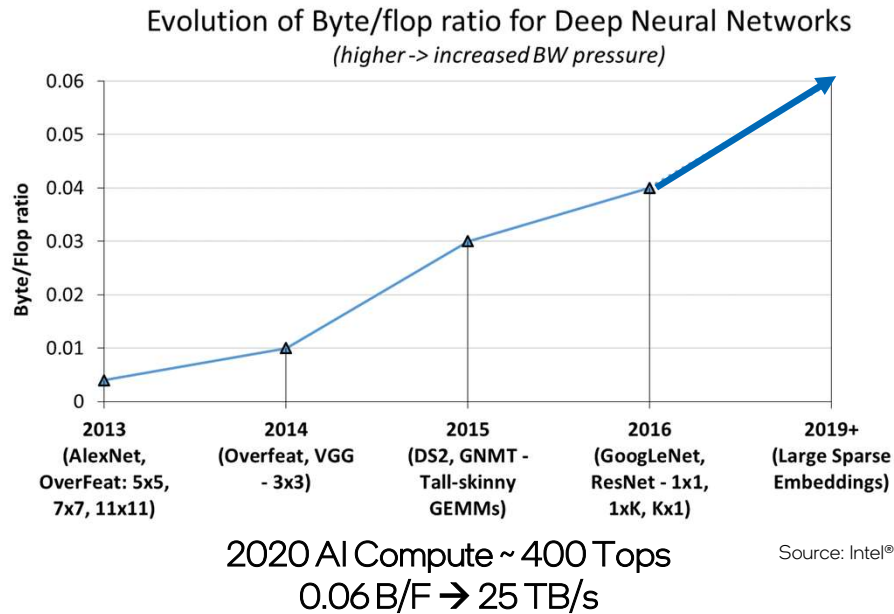


Thank you

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Motivation: AI Memory BW/Power Gap



□ Insatiable Memory Bandwidth

□ The energy efficiency gap is getting bigger