

October 2023

Manufacturing next generation power devices – How temporary bonding allows wide bandgap power devices to go vertical

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- Motivation – Losses in Power Devices
- SiC Status & Outlook
- GaN Status & Outlook
- Summary

WBG Power Devices I Introduction

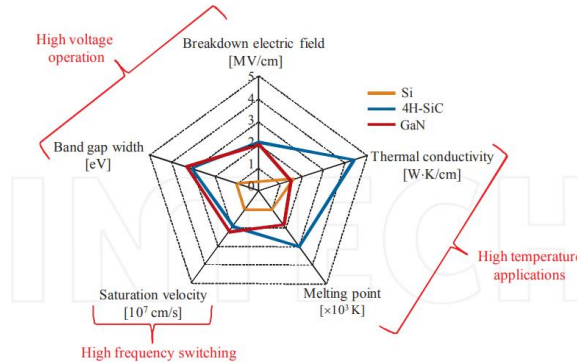


Increase of power consumption demands efficient, low loss power conversion
→ Reduction of Power Device Losses is needed

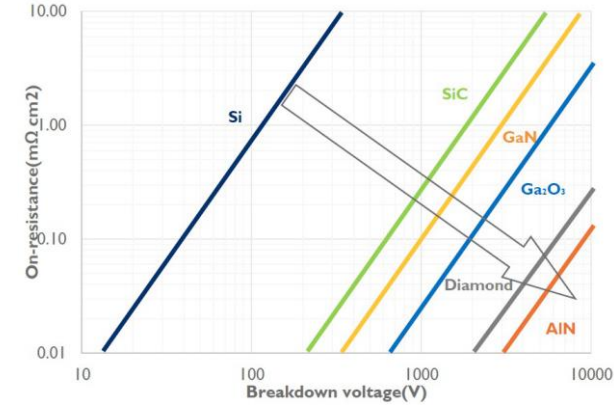


Main Power Device Loss Contributors

- Conduction losses
 - Device thickness (vertical devices)
 - Material properties
 - Device type & design
- Switching losses
 - Frequency dependent
 - Material properties
 - Device type & design



Source: O. Deblecker et al: "Comparative Study of Optimally Designed DC-DC Converters with SiC and Si Power Devices"



Source: Yole



Using WBG materials can reduce losses

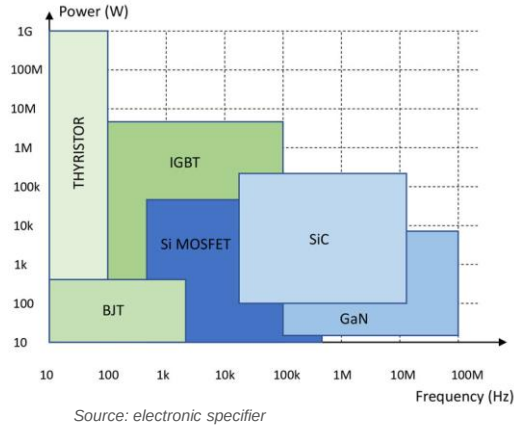
- Materials with lower on-resistance can offer a conduction loss reduction
- Materials with higher electron velocity can offer switching loss reduction, especially at higher frequencies



Focus of this presentation on SiC & GaN

Vertical Power Devices I **Advantages and Challenges**

→ Increase of power consumption demands efficient, low loss power conversion



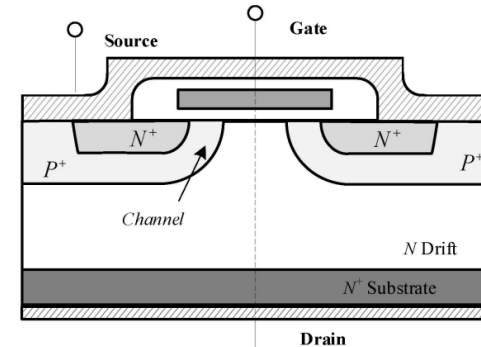
→ Majority of Power Devices are vertical devices (exception: GaN)

→ Advantages of vertical Power Devices compared to lateral devices

- Higher device safety (Lateral devices have risk for electrostatic discharge)
- Smaller devices (As voltages become bigger, lateral devices would become larger)

→ General Challenges of vertical power devices

- Wafer front and back side processing
- High Material quality throughout the device
- Conduction losses depend on device thickness → thinning is necessary to increase device performance
- Handling concepts because of thin wafers



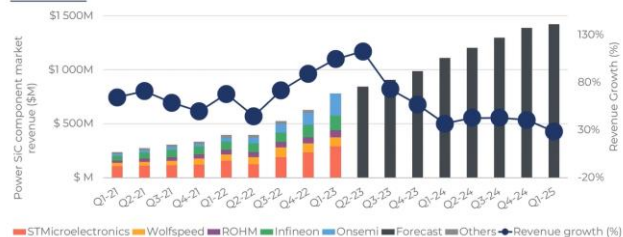
Vertical Structure of power MOSFET v

Source: Cen Chen et al: "PHM Application of Power Converters Using Health Precursor of Power MOSFETs", Harbin Institute of Technology

SiC already well established and growing

Main driver: EV

POWER SiC DEVICE REVENUES* - MARKET DYNAMICS - 000**



*Power SiC device revenues include discrete devices and modules

^{***}QoQ: Quarter-on-quarter. Similar to YoY, quarter-over-quarter growth rate calculates the percentage change of one period to the same period from the previous year.

*** The total revenue for device suppliers is higher than the market size estimation from the top-down approach due to double counting.

Double counting: please refer to the Terminology and Definitions chapter



1

SIC DESIGN-WIN MATRIX AS OF Q2-2023

Leading SiC device players' design-wins at OEMs

OEM	SCF device	TESLA	HYUNDAI	Volvo	VW	Mercedes-Benz	BMW	MINI	gim	NIO	XPeng	Li Auto	BYD
Infineon	✓	✓	✓										
ansem	✓	✓	✓		✓	✓	✓	✓		✓			✓
Wolfspeed					✓	✓	✓	✓	✓			✓	✓

- As of 2023, major OEMs are looking for double-sourcing SiC devices for their current and future models to be released.
- It's a non-exhaustive list.
- The information is based on Yole's understanding, sources from press releases and industry feedback.



1

Challenges of SiC vertical power devices

- Transition to 200 mm is happening (substrate quality is still a challenge)
- Generally SiC is a very robust material – good to handle
- Thinning is necessary – need for mechanical support on 200 mm is needed → temporary bonding to a carrier wafer



Temporary Bonding Process



SiC power devices – process integration

Temporary Bonding Principle

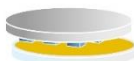
Carrier wafer coated with release layer



Front side processed device wafer



Flip wafer



Alignment

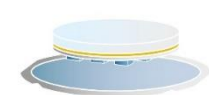


Bonding



Wafer thinning & Backside processing

Debonding Principle



Mount wafer stack onto film frame



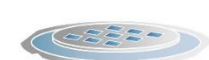
Debond process



Clean process



Thin wafer on film frame



Front Side Processing



Temporary Bonding



Thinning



Metal deposition & Contact formation



Debonding

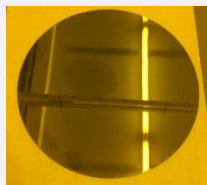


Electrical testing

Laser Annealing to be compatible with TBDB process

Temporary Bonding and Debonding of 200 mm SiC wafer

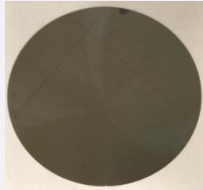
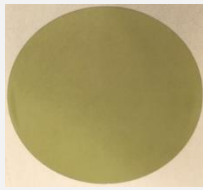
Incoming 200 mm SiC Wafer



II-VI

(now Coherent)

Temporary Bonding

	SiC + Carrier Wafer	thinned SiC + Carrier Wafer
Si Carrier Thermoplastic Adhesive		
Glass Carrier Thermoset Adhesive		



Debonding



Work conducted within EU
project REACTION



first and euRopEAn siC eight Inches piLot line
Coordinator: ST Catania



This project has received funding from the ECSEL Joint Undertaking (JU) under grant agreement No 783158. The JU receives support from the European Union's Horizon 2020 research and innovation programme and Italy, Germany, Belgium, Sweden, Austria, Romania, Slovakia, France, Poland, Spain, Ireland, Switzerland, Israel.

GaN Power Devices | Status & Outlook



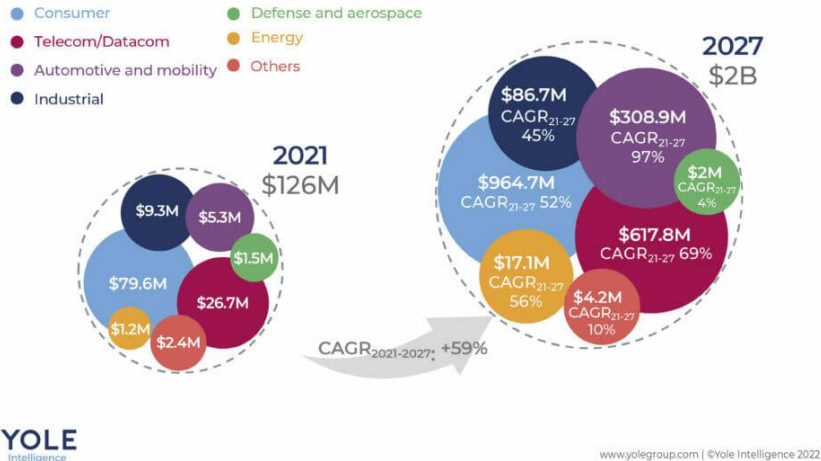
GaN market strongly growing
Main driver: Consumers (lateral devices)



Challenges of GaN vertical power devices

2021-2027 POWER GAN DEVICE MARKET REVENUE

Source: Power GaN report, Yole Intelligence, 2022

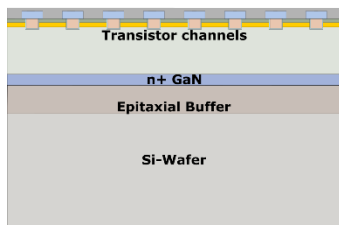


- GaN typically grown on foreign substrate (Si or Sapphire) because of cost reasons
- Dislocations threaten the device safety of vertical devices
 - at the moment lateral devices commercially available
 - Maximum power is limited for lateral devices with reasonable size
- R&D is going on for vertical GaN power devices

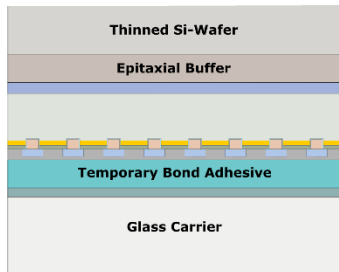


Backside process technology for membrane access

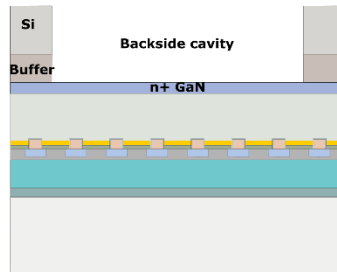
Frontside process finished



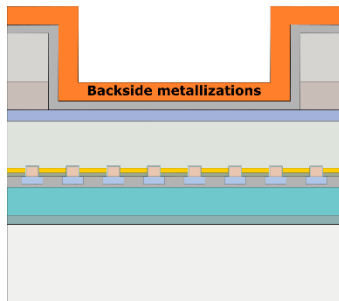
Temporary bonding



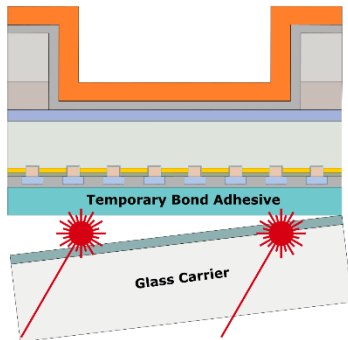
Backside access etching



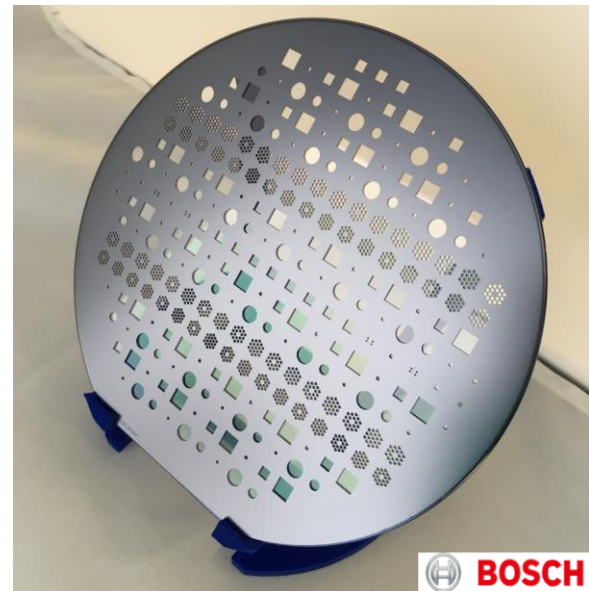
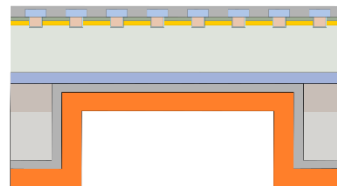
Contact + reinforcement metals



Laser debonding



Dicing

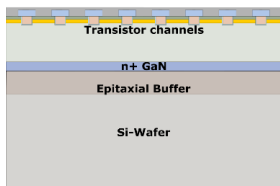


Up to 5 mm GaN membrane diameter has been realized on 150 mm wafers using temporary bonding with laser debonding.

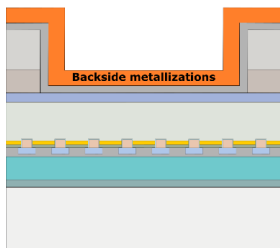


Process Compatibility Challenges

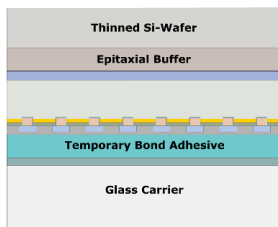
Frontside process finished



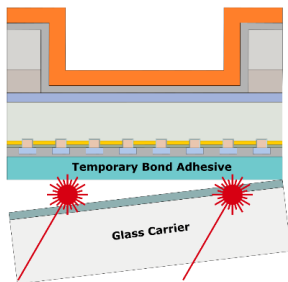
Contact + reinforcement metals



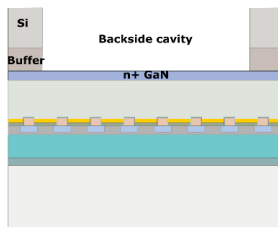
Temporary bonding



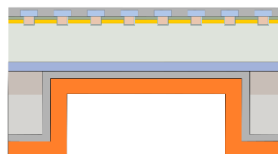
Laser debonding



Backside access etching



Dicing



Temporary Bonding necessary to enable backside processing
(process implementation on 150 and 200 mm wafer)

Organic adhesive used at temporary bonding has to be compatible with used temperatures and chemistry

- Backside access etching
 - Temperature input during etching must be limited – compatible process recipe was found
- Backside metallization
 - Especially annealing for ohmic contact formation is critical
 - Laser annealing / chemical treatment for ohmic contact formation

→ **Temporary bonding enables 200 mm SiC backside processing**

→ **Vertical GaN power devices need support during thinning and backside processing – temporary bonding is compatible with the process flow**

Temporary Bonding Principle

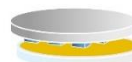
Carrier wafer coated with release layer



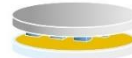
Front side processed device wafer



Flip wafer



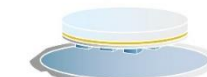
Alignment



Bonding



Debonding Principle



Mount wafer stack onto film frame



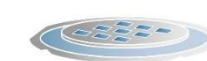
Debond process



Clean process



Thin wafer on film frame



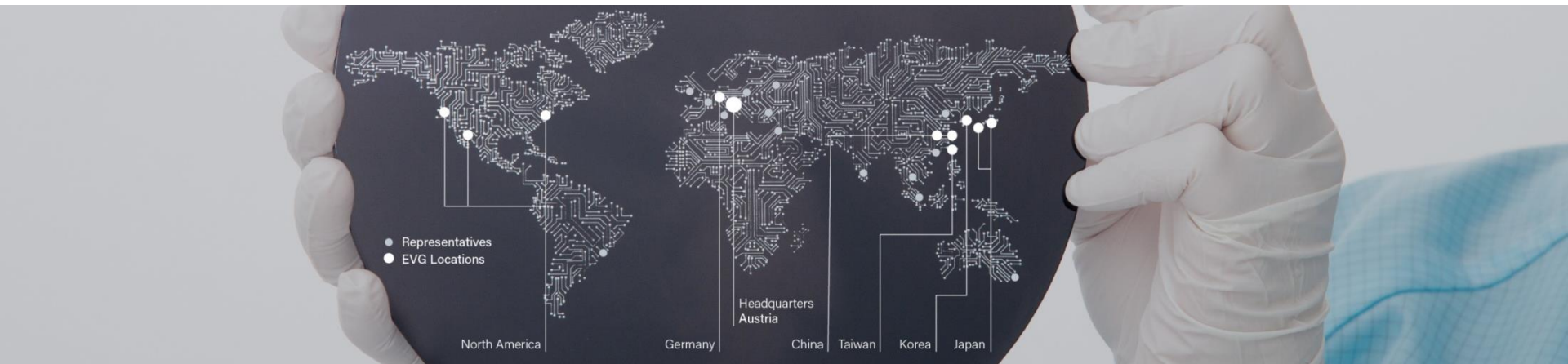
Wafer thinning & Backside processing

Process Technology and Services

- State-of-the-art cleanrooms and application labs at headquarters, in North America and in Asia.
- Process development services ease adoption and enhance efficiency of EVG equipment.
- Partnering with customers to deliver peak performance throughout the entire product lifecycle.
- NILPhotonics® Competence Center established in 2014.
- Heterogeneous Integration Competence Center established in 2020.
- First-of-its-kind Step-and-Repeat Mastering Services for nanoimprint lithography launched 2021.



Thank you!



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