
Cost-Efficient Wafer-level SOI Process for Thermal Stability and Area Shrinkage in 3D NAND Peripheral Circuit

Seungmin Lee

Sungkyunkwan University

Department of Semiconductor and Display Engineering

Advanced Display and Nano Device Laboratory

Outline

I. Introduction

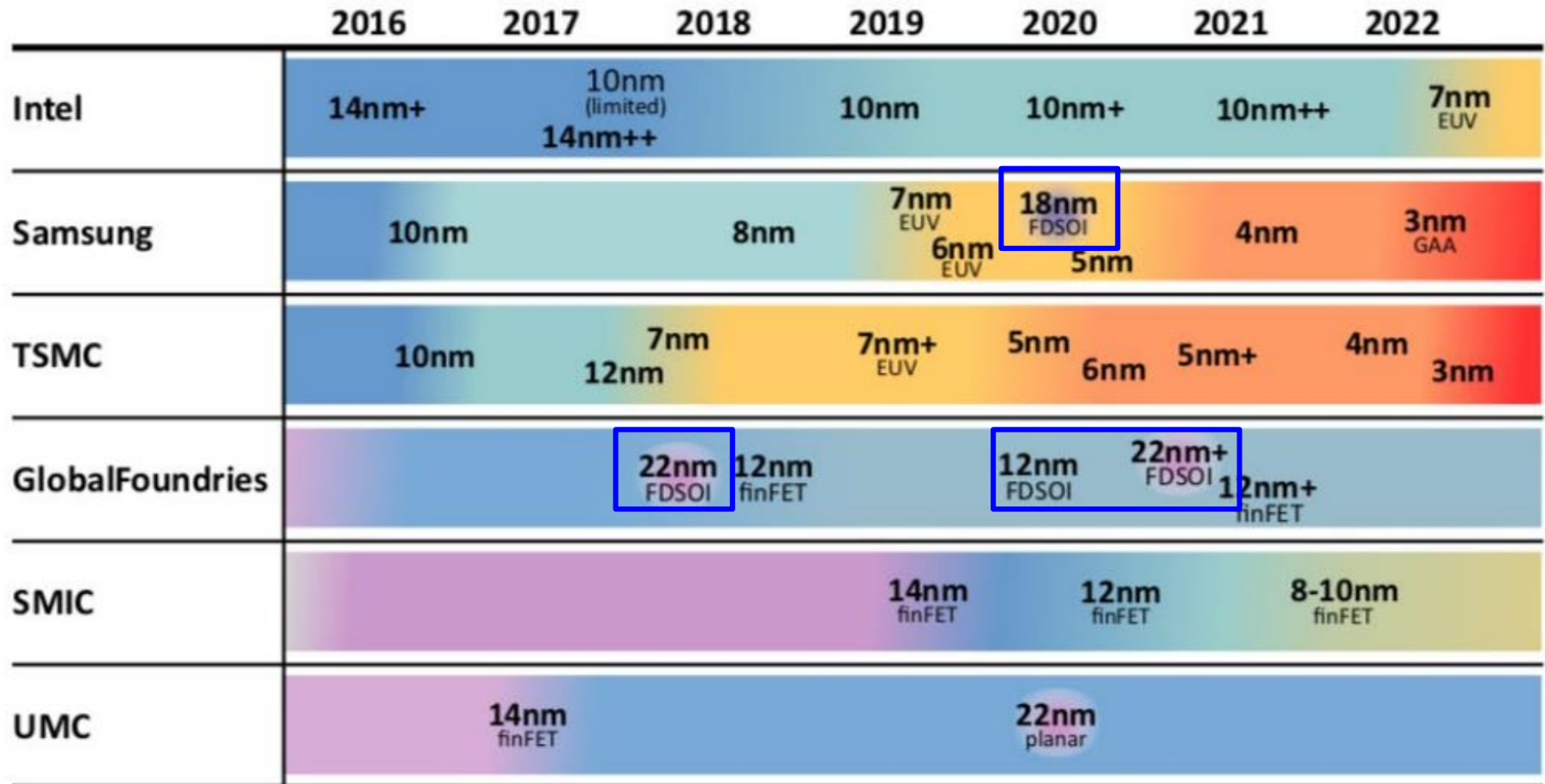
II. Wafer-level SOI process

III. Thermal Stability

IV. Charge Pump Capacitor in 3D NAND

Logic Foundry Process Roadmap

- FDSOI is utilized in specific nodes due to its high wafer cost.



Sources: Companies, conference reports and IC Insights

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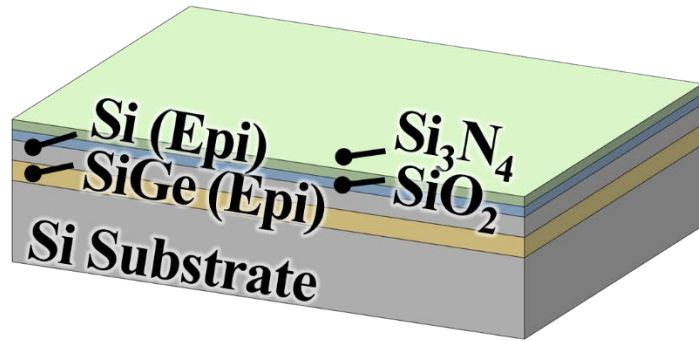
II. Wafer-level SOI process

III. Thermal Stability

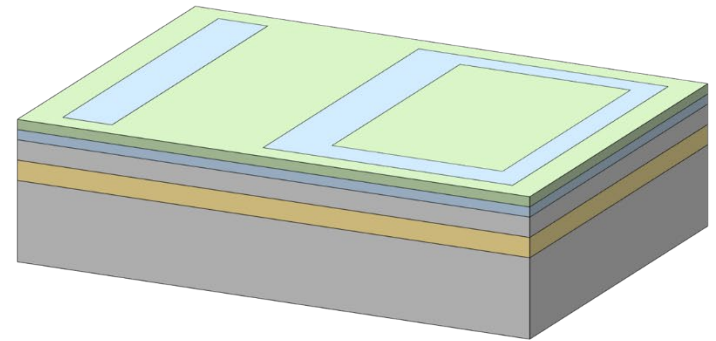
IV. Charge Pump Capacitor in 3D NAND

Wafer-level SOI Process

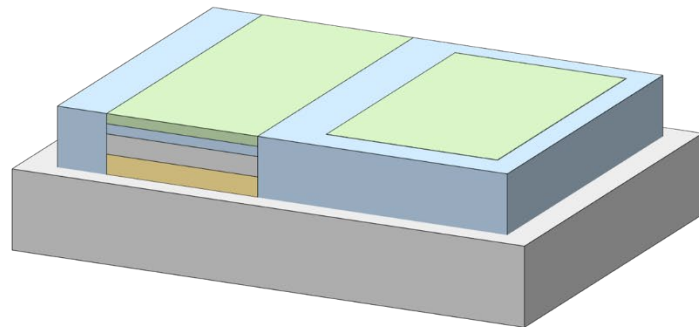
- SiGe $\rightarrow$ SiO₂ Replacement by High Selectivity removal and ALD.
- Supporter Pillar = Another STI process.



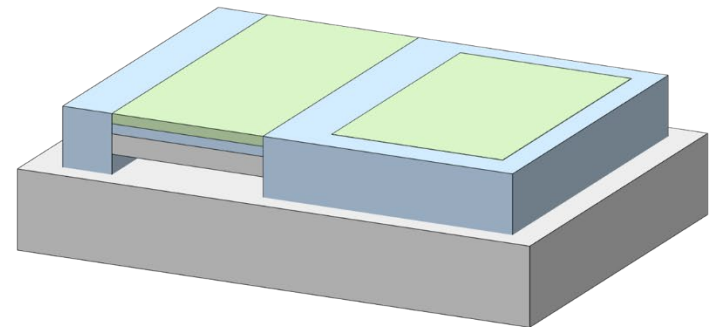
(a) Epitaxial growth of SiGe and Si. Passivation of SiO₂ and Si₃N₄



(b) Supporter pillar formation



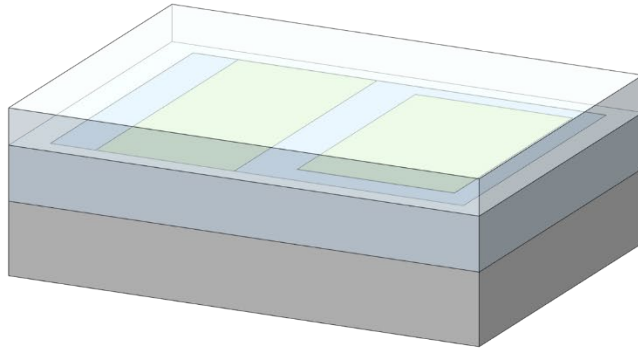
(c) STI etch



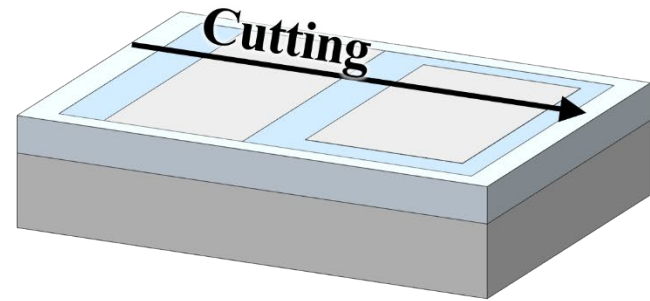
(d) SiGe selective etch

Wafer-level SOI Process

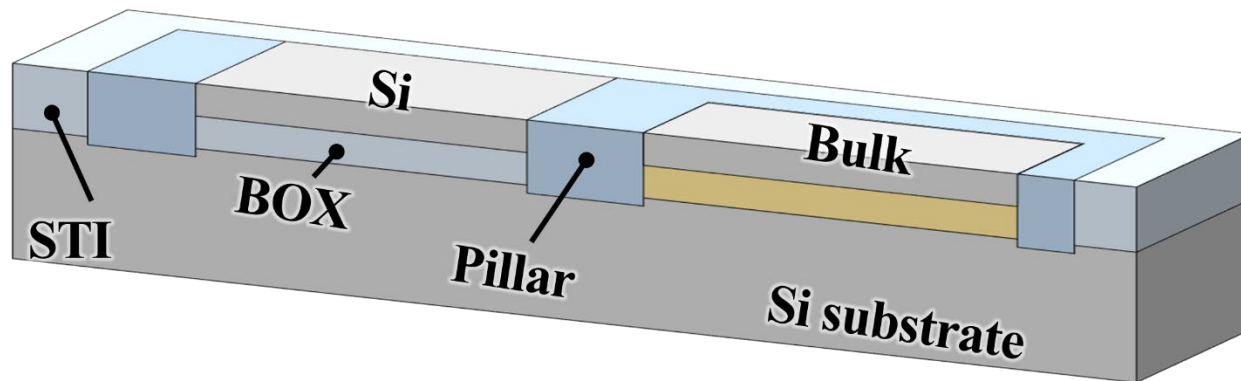
- The SOI area and bulk area can be formed without steps.



(e) BOX and STI oxide gap filling



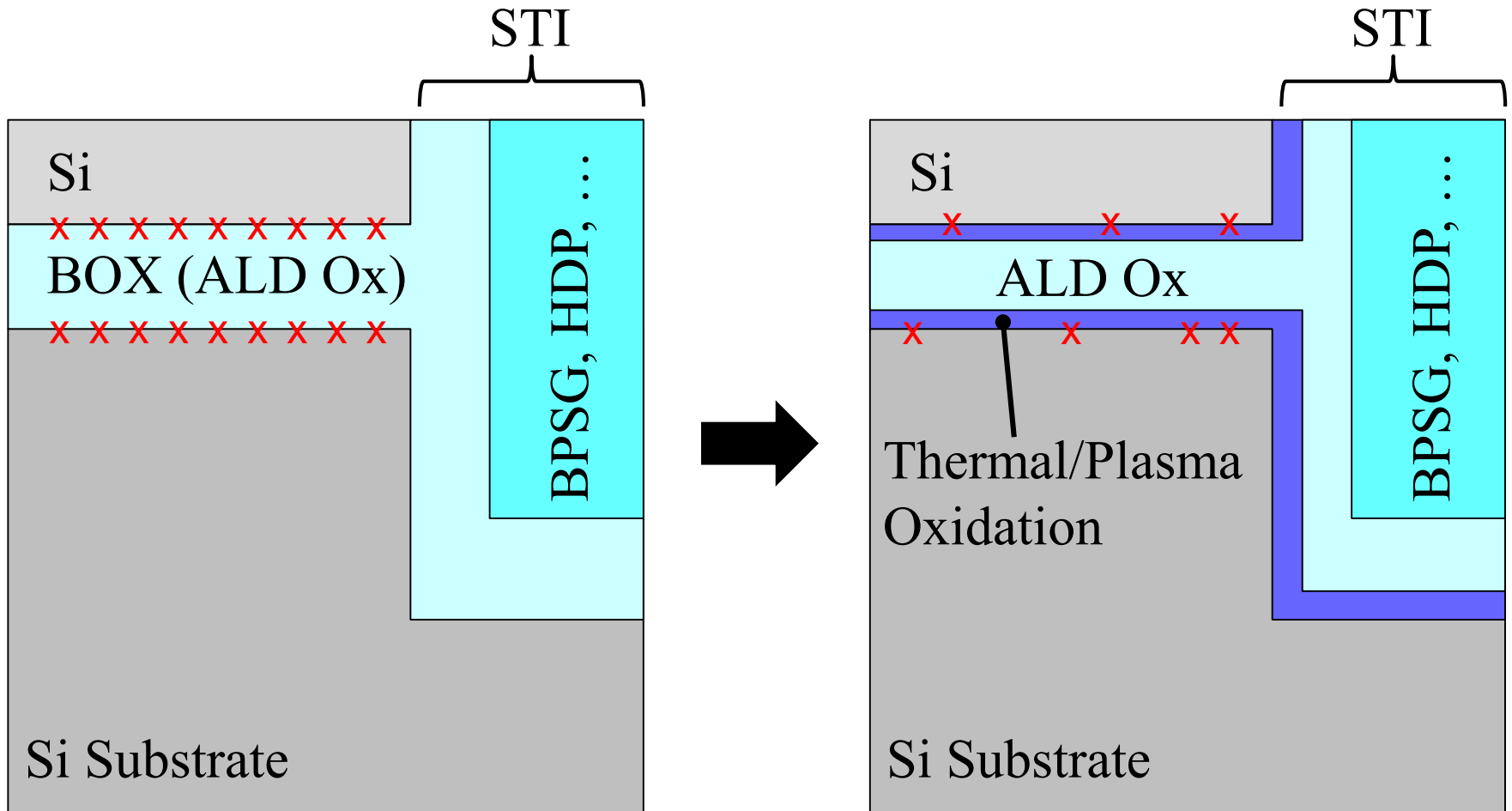
(f) STI CMP and passivation layer removal



(g) 2D cross section (SOI and Bulk area)

Wafer-level SOI Process

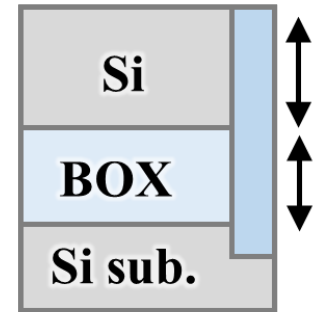
- Interface traps can be minimized through thermal/plasma oxidation.



Pros and Cons of Wafer-level SOI

(Pros)

- **Low cost fabrication.**
(Only one- photo layer; supporter pillar process.)
- **Easy to control the thickness of BOX and Si.**
- **The material of the BOX can be changed.**
(e.g., SiO_2 , Si_3N_4 , Al_2O_3 , ...)



(Cons)

- **The layout design is limited** (because it is formed through the support pillar and STI).
→ **Memory Device (DRAM, Flash) is more suitable.**
(Design and production are carried out by one company.)

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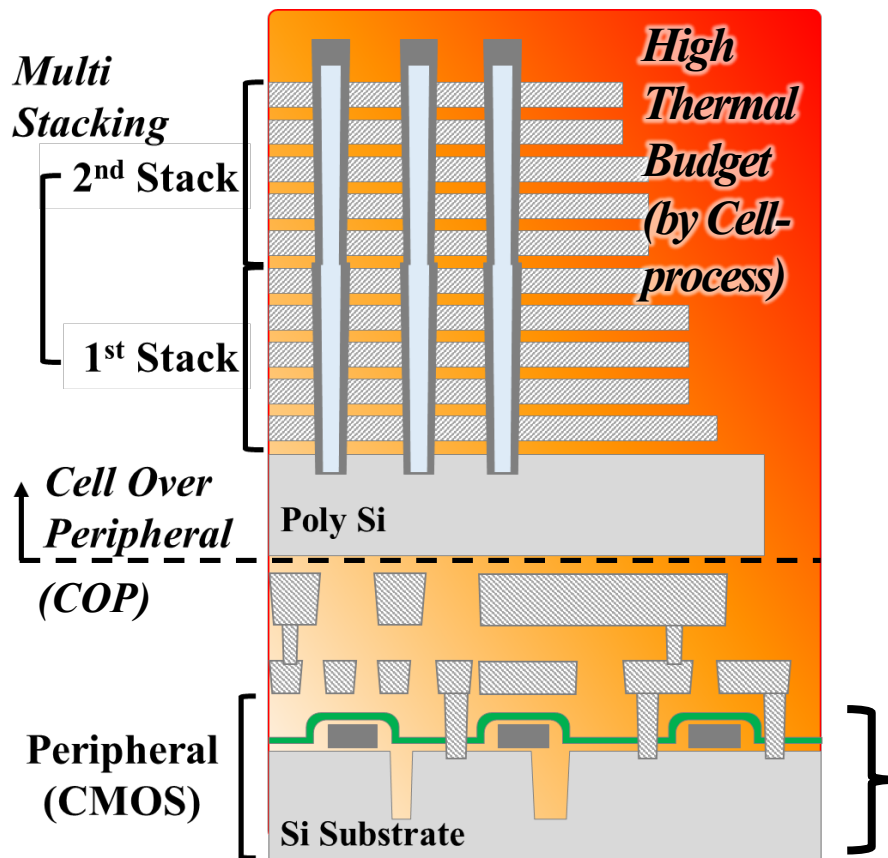
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III. Thermal Stability

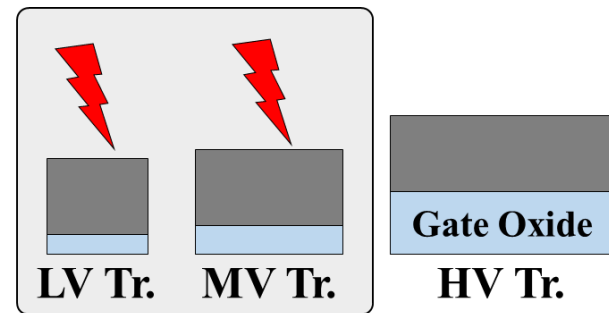
IV. Charge Pump Capacitor in 3D NAND

Thermal Budget Issue in 3D NAND

- High thermal process occurs after the CMOS process.
- Dopant diffusion due to high thermal budget deteriorates transistor performance → difficult to make the peripheral area small.



Vulnerable to Thermal Budget



LV: Low Voltage, MV: Medium Voltage, HV: High Voltage

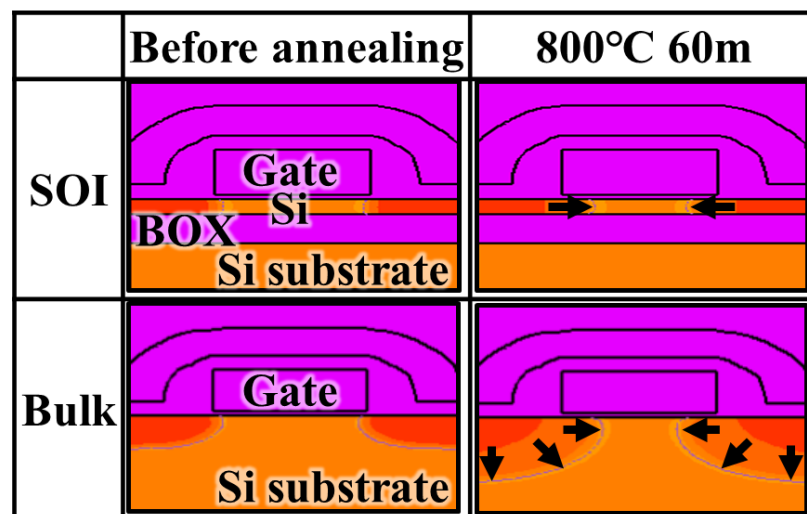
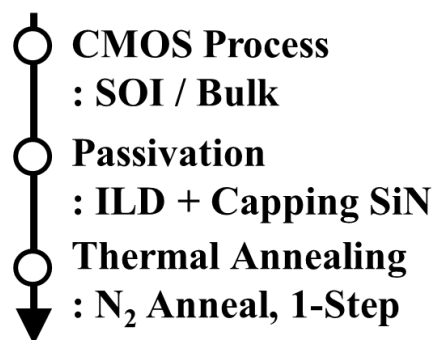
Thermal Stability Simulation

- Simulation for thermal stability validation.

< Simulation Parameters >

	SOI	Bulk
Gate length	45, 65, 90 nm	
Gate material	P+ poly Si (PMOS)	
T _{GOX}	3 nm SiO ₂	
T _{BOX}	20 nm	—
T _{Si}	10 nm	—
Junction depth	10 nm	25 nm
N _D , N _{S/D}	10 ¹⁸ cm ⁻³ , 10 ²⁰ cm ⁻³	
Passivation	ILD oxide 100 nm Capping SiN 200 nm	
Thermal annealing	N ₂ 800 °C 0, 60, 120 minute	
Diffusion model	Fermi	
Drain voltage	-1, -0.1 V (DIBL)	

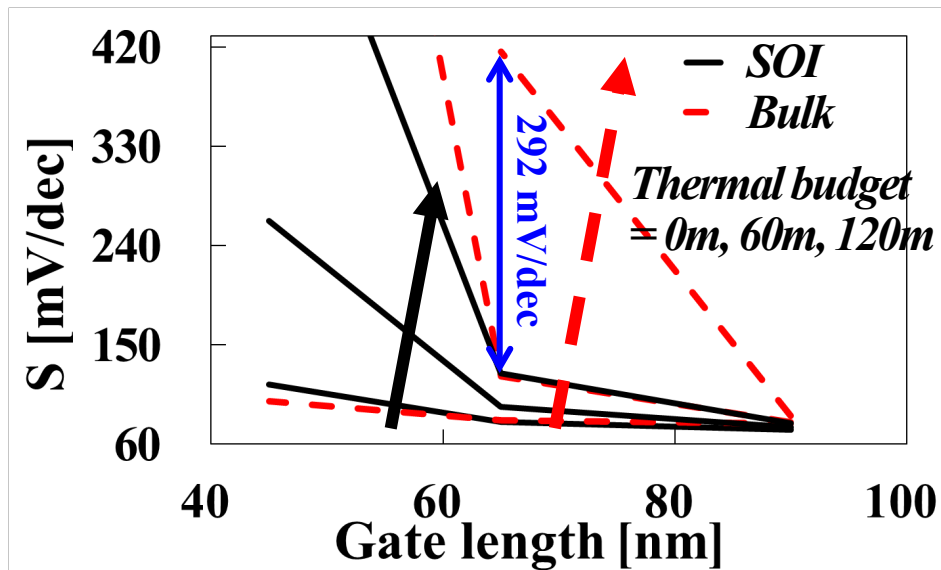
< Test flow & Junction profile >



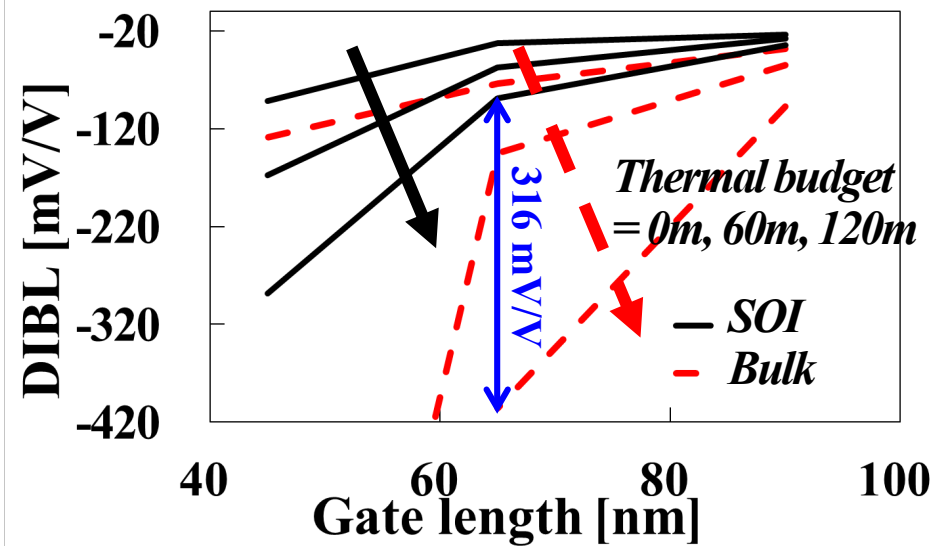
Simulation Result

- Less deterioration in Swing and DIBL characteristics in SOI.

< Subthreshold Swing >



< DIBL >



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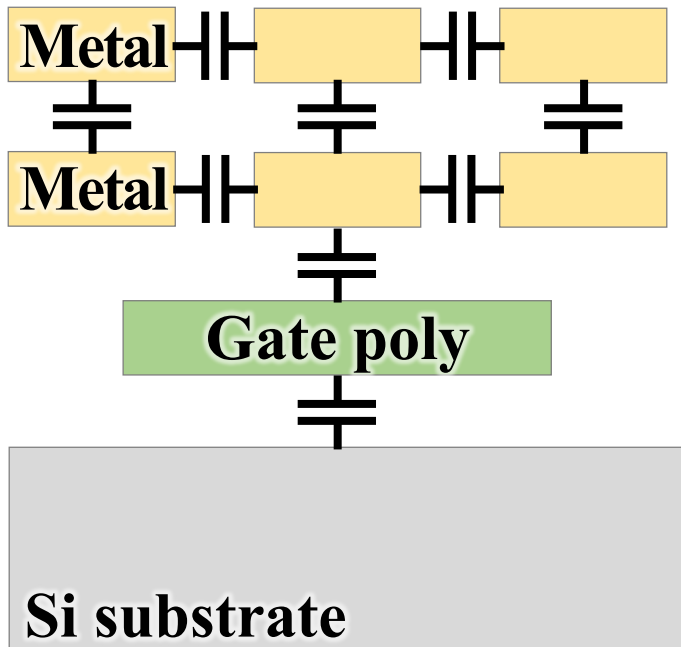
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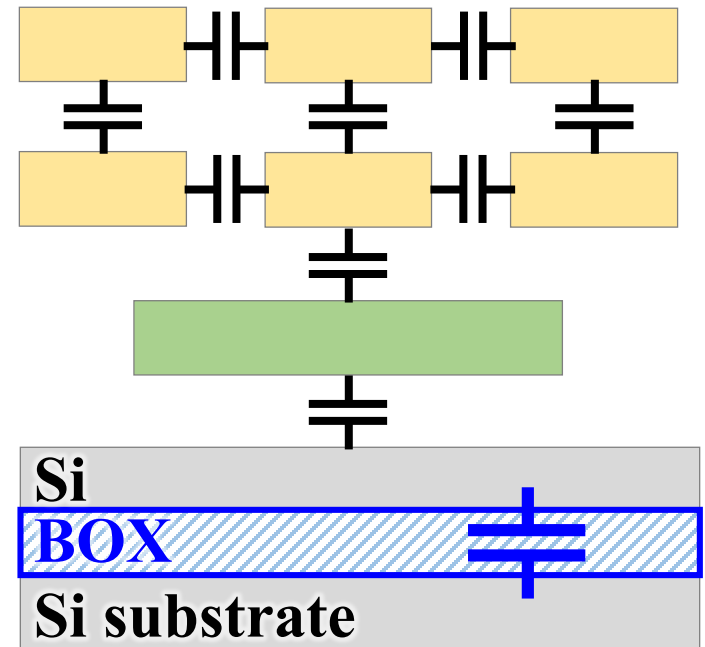
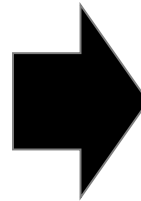
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Charge Pump Capacitor in 3D NAND

- Program / Erase Operation: $> 20\text{V}$ (FN Tunneling)
- High voltage charge pump circuit is required.
- SOI can provide additional capacitors.



Charge pump capacitor
in 3D NAND

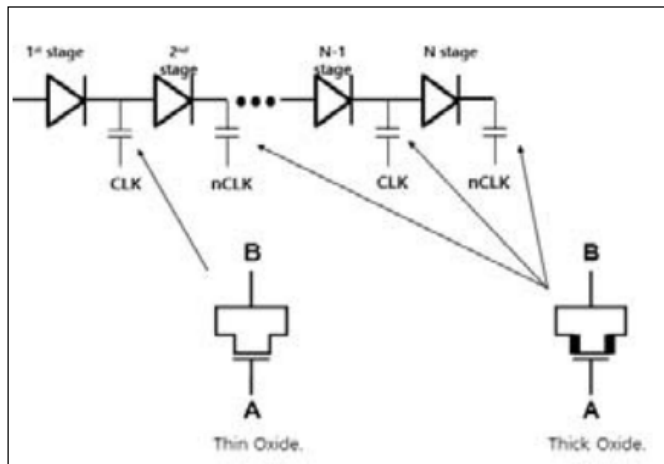


Charge pump capacitor
in 3D NAND using SOI

Charge Pump Capacitor in 3D NAND

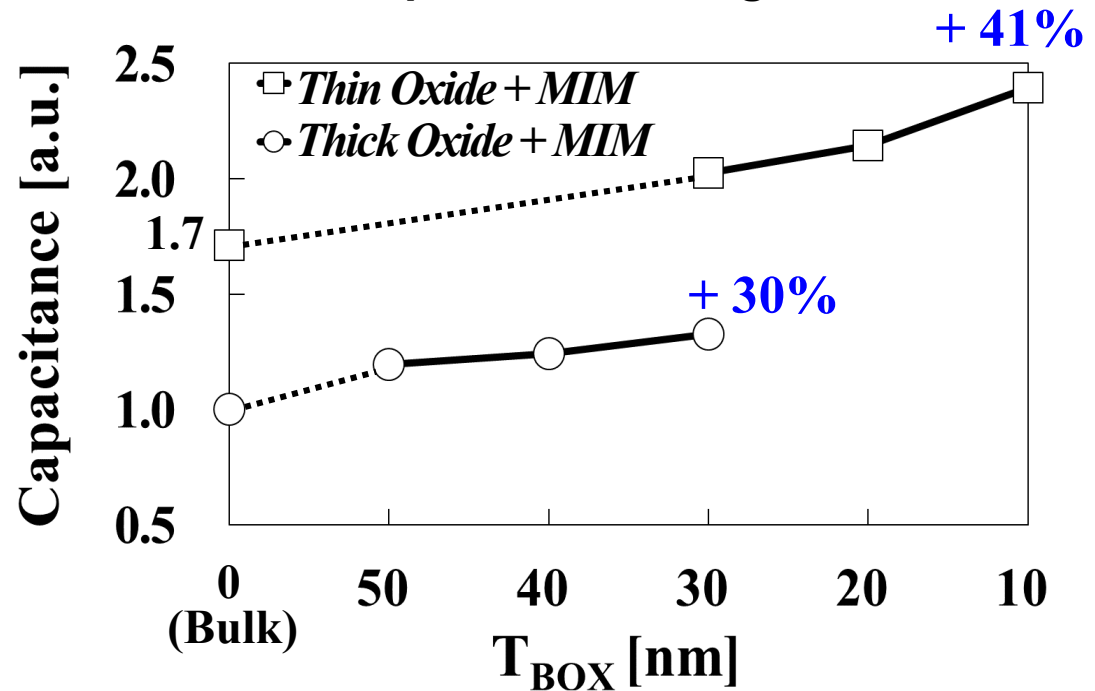
- When configured with SOI, the capacity of the charge pump capacitor can be increased by up to 40% or more.

< CP Cap. by series stages >



Source: J. Cho, ISSCC, 2021, pp. 426-428

< Capacitance using SOI >



Thank you