



SmartSiC™: a greener, faster and better technology for SiC

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SEMICON EU |

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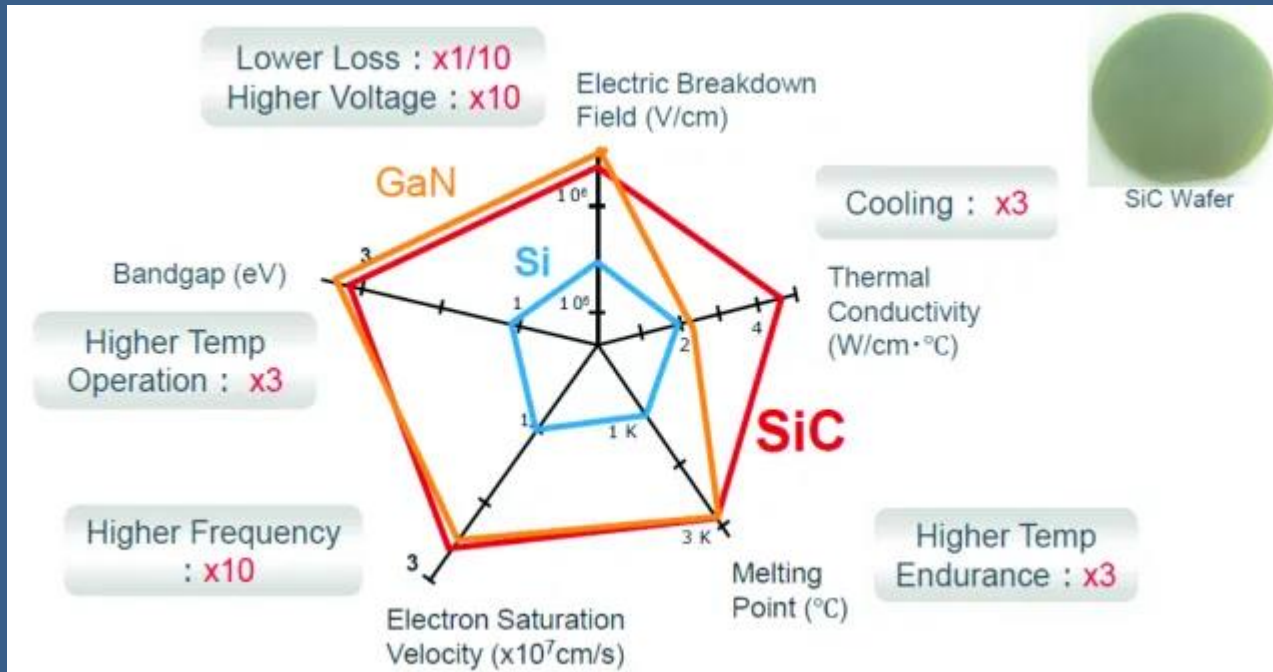
“Innovation for a Sustainable World”

SmartSiC™ Engineered Substrate

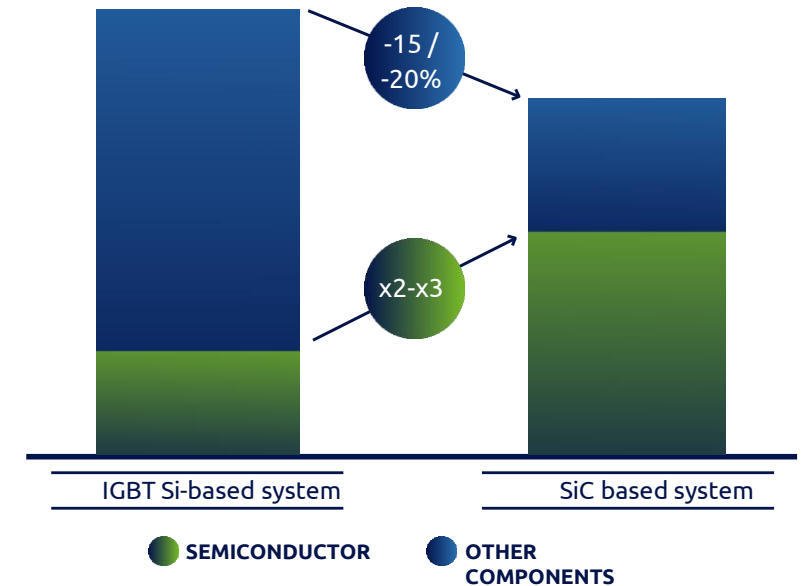
SiC has better PPAC than Si
SmartCut™ is bringing unique performances &
energy savings

SiC IS THE OBVIOUS WINNER IN THE POWER DEVICE Pentathlon

DELIVERING ENERGY EFFICIENCY



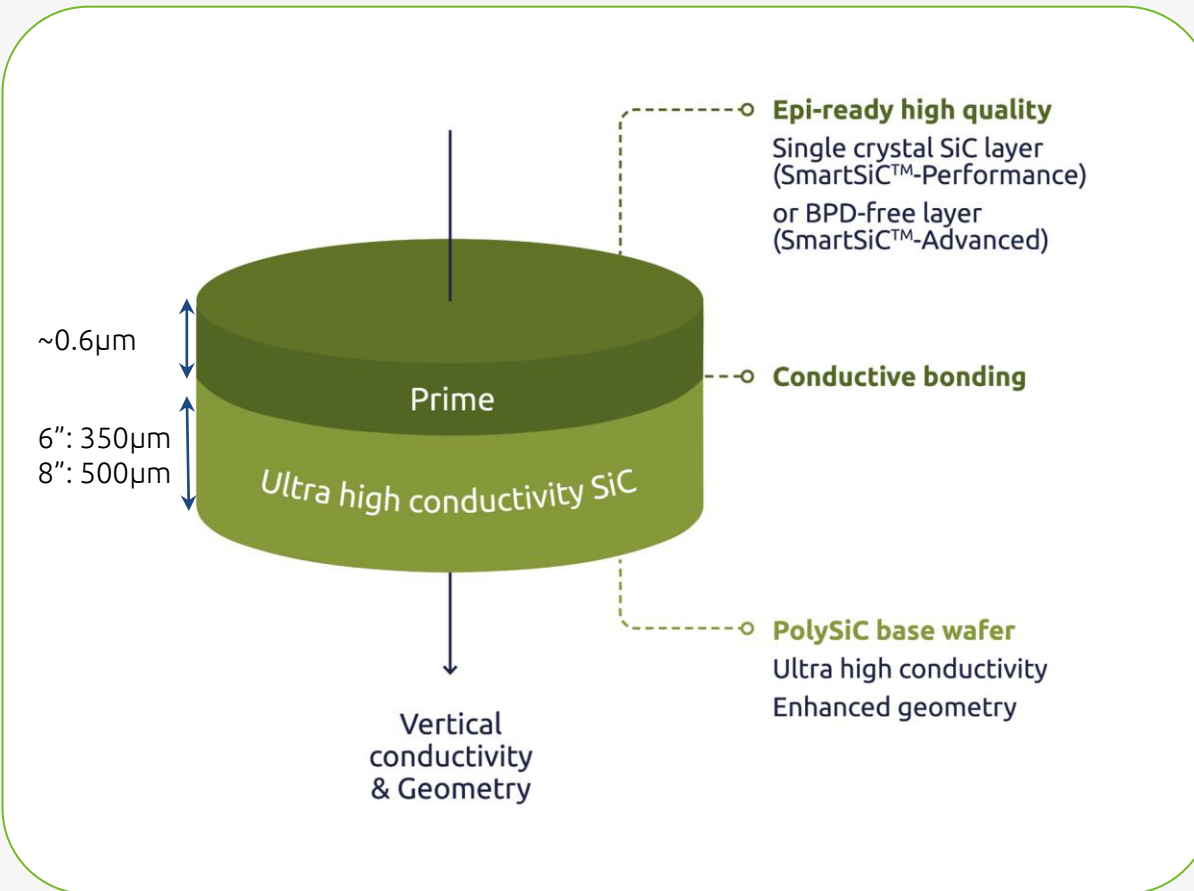
TOTAL SYSTEM COST – 15-20% REDUCTION



Shorter charge time 800V	~50% FASTER
Increased battery range	~5-10% LONGER
Reduced system / battery cost	~\$500-\$1,000

SmartSiC™

SOITEC'S 30 YEARS OF EXPERTISE ADAPTED TO SiC



SmartSiC™ is a new-generation SiC substrate with:

- **ultra-high conductivity**

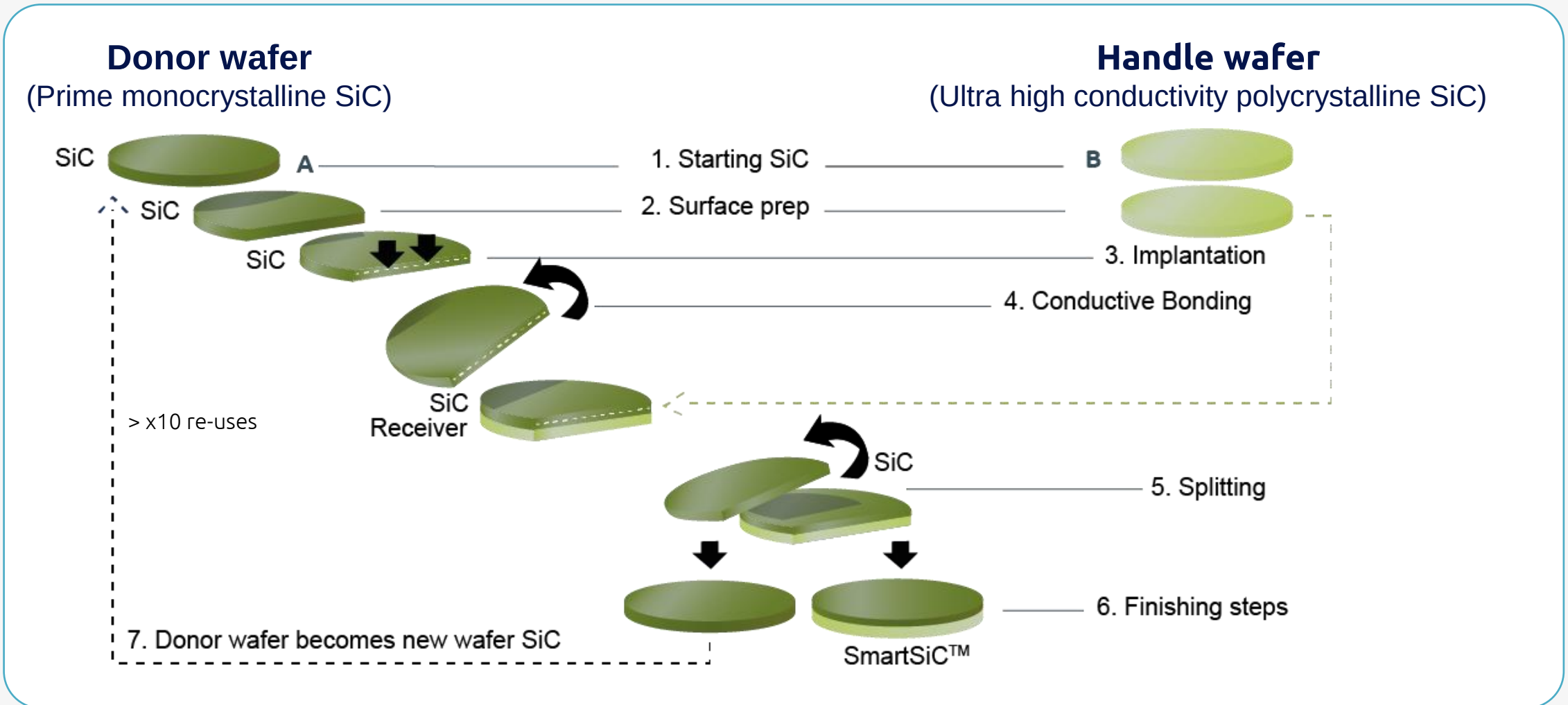
$\sim 8\times$
pSiC BETTER
CONDUCTIVITY

- better usage of **high quality** single crystal SiC layer benefitting from the **re-usability** provided by the Smart Cut™ process

$>10\times$
MONO-SiC WAFER
RE-USABILITY

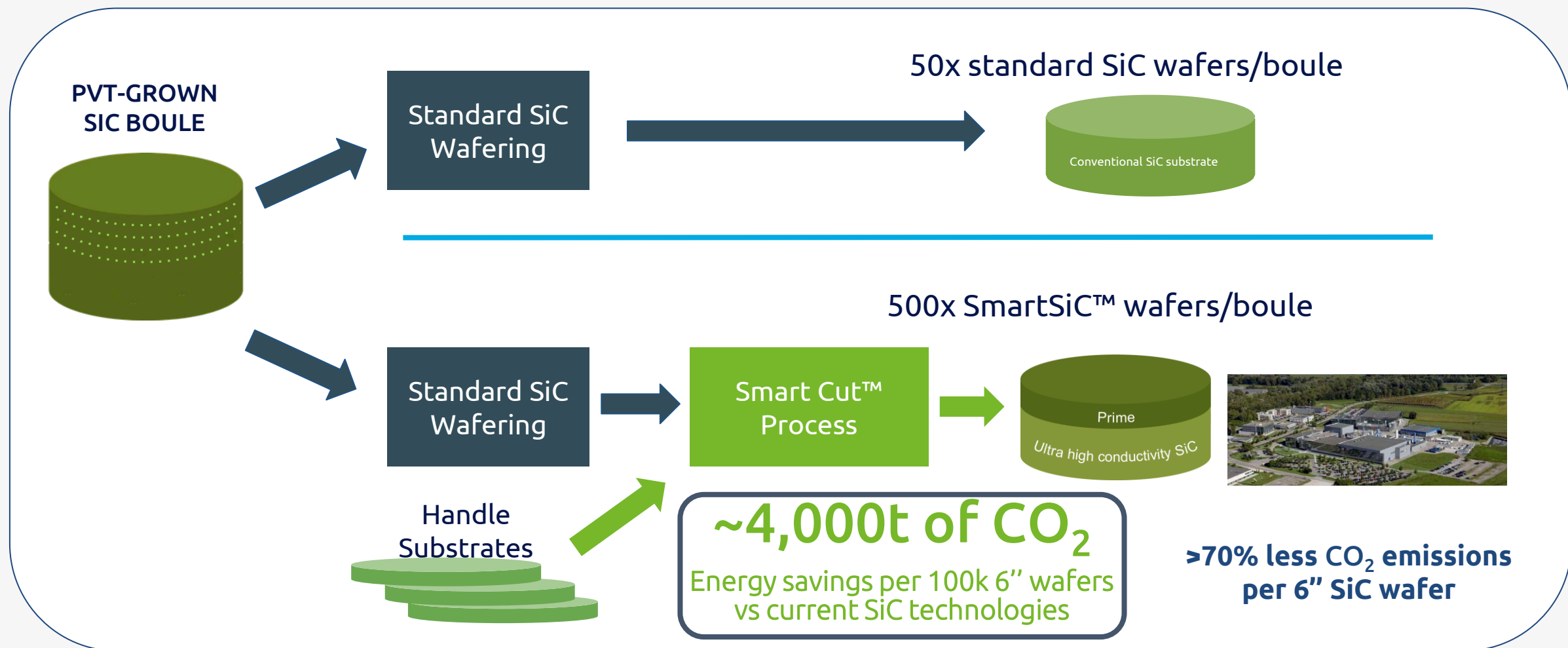
SmartCut™

PROCESS ADAPTED TO SiC



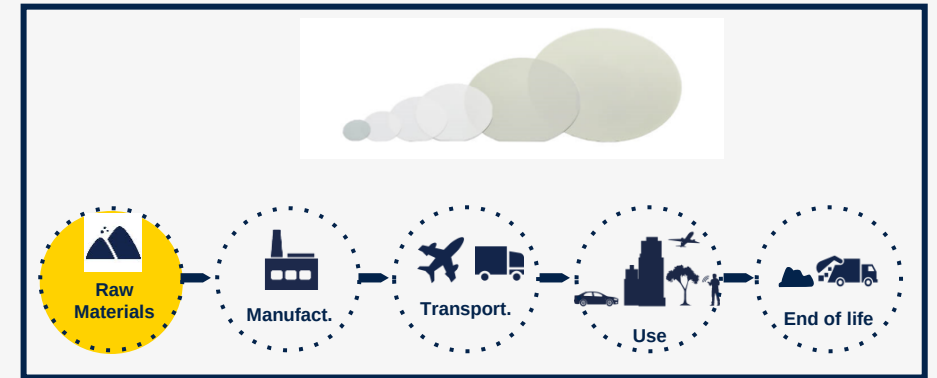
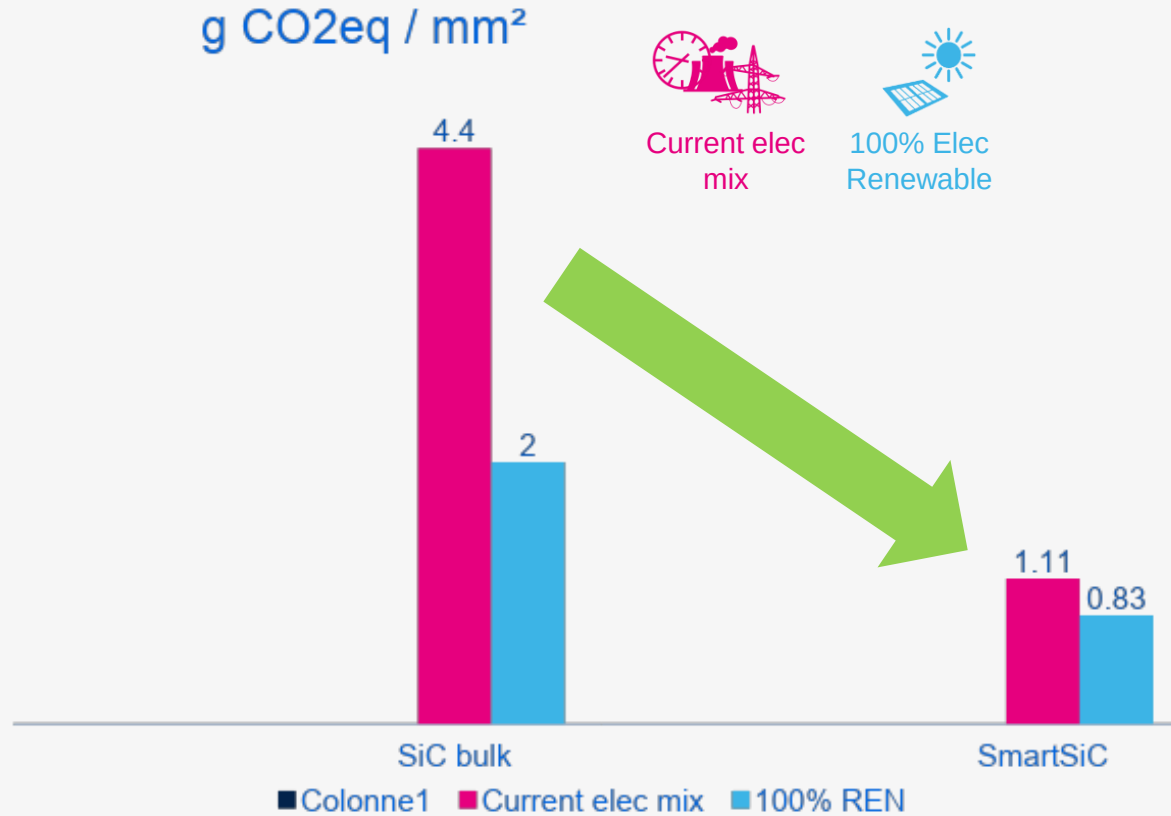
SmartSiC™

REDUCED CO₂ FOOTPRINT



SmartSiC™

TECHNOLOGY DIVIDES BY 4 THE CO₂ EMISSIONS TO MANUFACTURE SiC WAFER

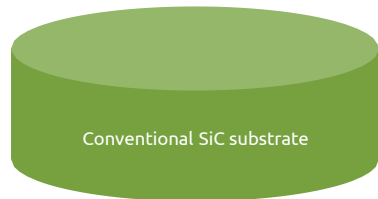


- Carbon emissions for wafers production following a life cycle analysis protocol
- Normalized results per mm² based on current and future electrical mix, and manufacturing data

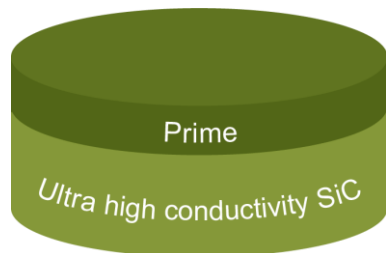
SOITEC SmartSiC™ TECHNOLOGY

USE ADVANTAGE

Current industry solution (monocrystalline bulk)



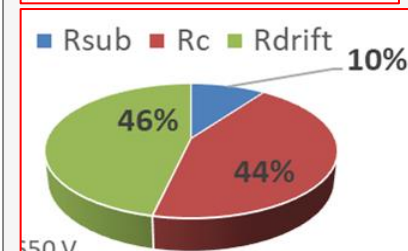
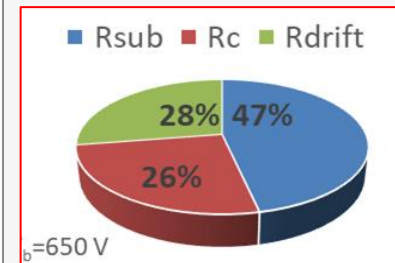
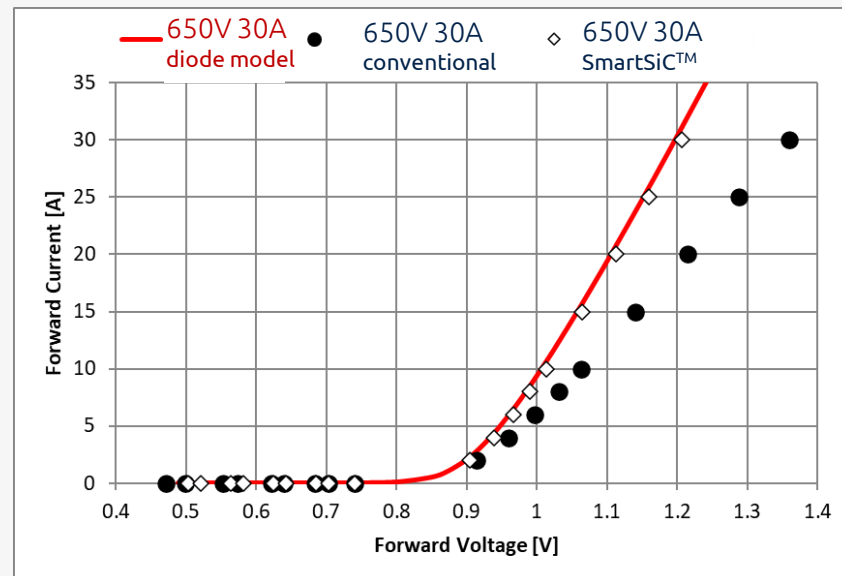
SmartCut™'s engineered Epi-ready substrate solution



VALUE PROPOSITION

- High increase of number of producible wafers
- Maximize substrate value
- Higher manufacturing yield
- Device feature size reduction / RDSon improvement
- Copy & paste of MOSFET process flow
- Acceleration of the path to 200mm transition

Experimental data on 650V SiC diode



SUBSTRATE CONTRIBUTION VANISH

BASED ON SOITEC ESTIMATIONS - 1200V MOSFET

8x higher substrate conductivity + Better current spreading + 10x lower resistivity of back-side contact =

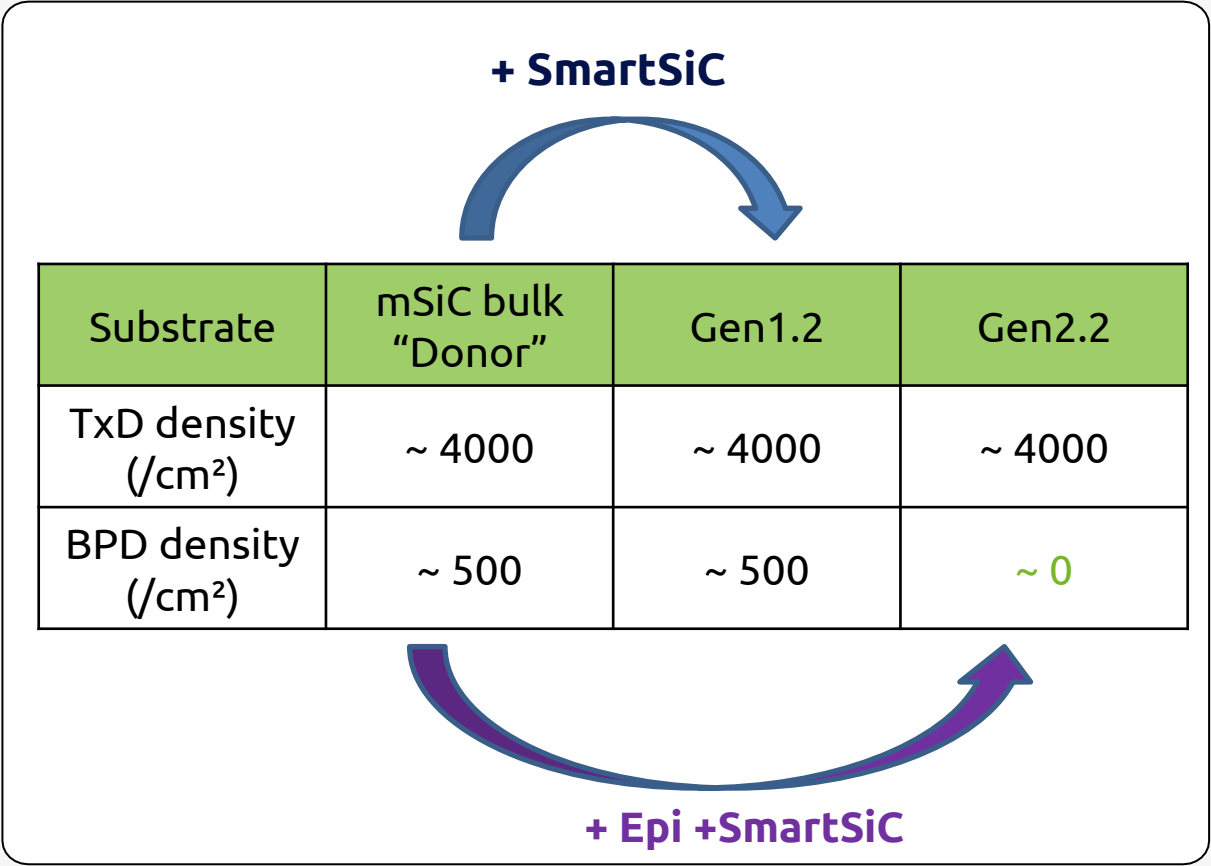
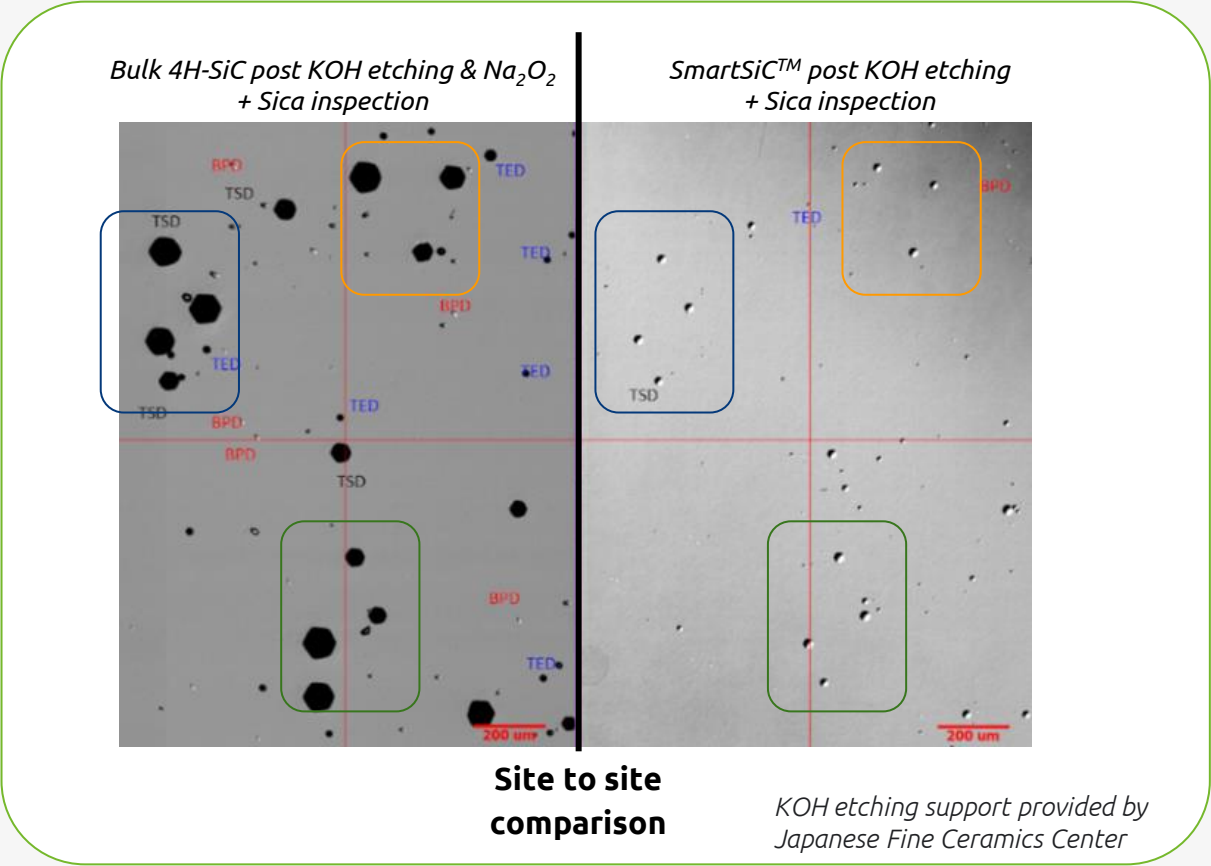
DEVICE MANUFACTURER		A	B	C	D
EGen (release year)		3 (2021)	2 (2022)	4 (2022)	3 (2022)
Techno (die thickness in μm)		Planar	Trench	Trench	Planar
Ron.A ($\text{m}\Omega\cdot\text{cm}^2$) @ 25°C (Public)		2.7	2.5	2.5	2.7
Reverse eng thickness, μm (*)		180	110	150	180
Smart SiC™	Substrate contribution (pSiC)	2.2%	1.6%	2.1%	2.3%
	Back-side contact pSiC ($\text{m}\Omega\cdot\text{cm}^2$)	0.002	0.002	0.002	0.002
	Gain vs mSiC	16.2%	12.1%	15.2%	16.9%

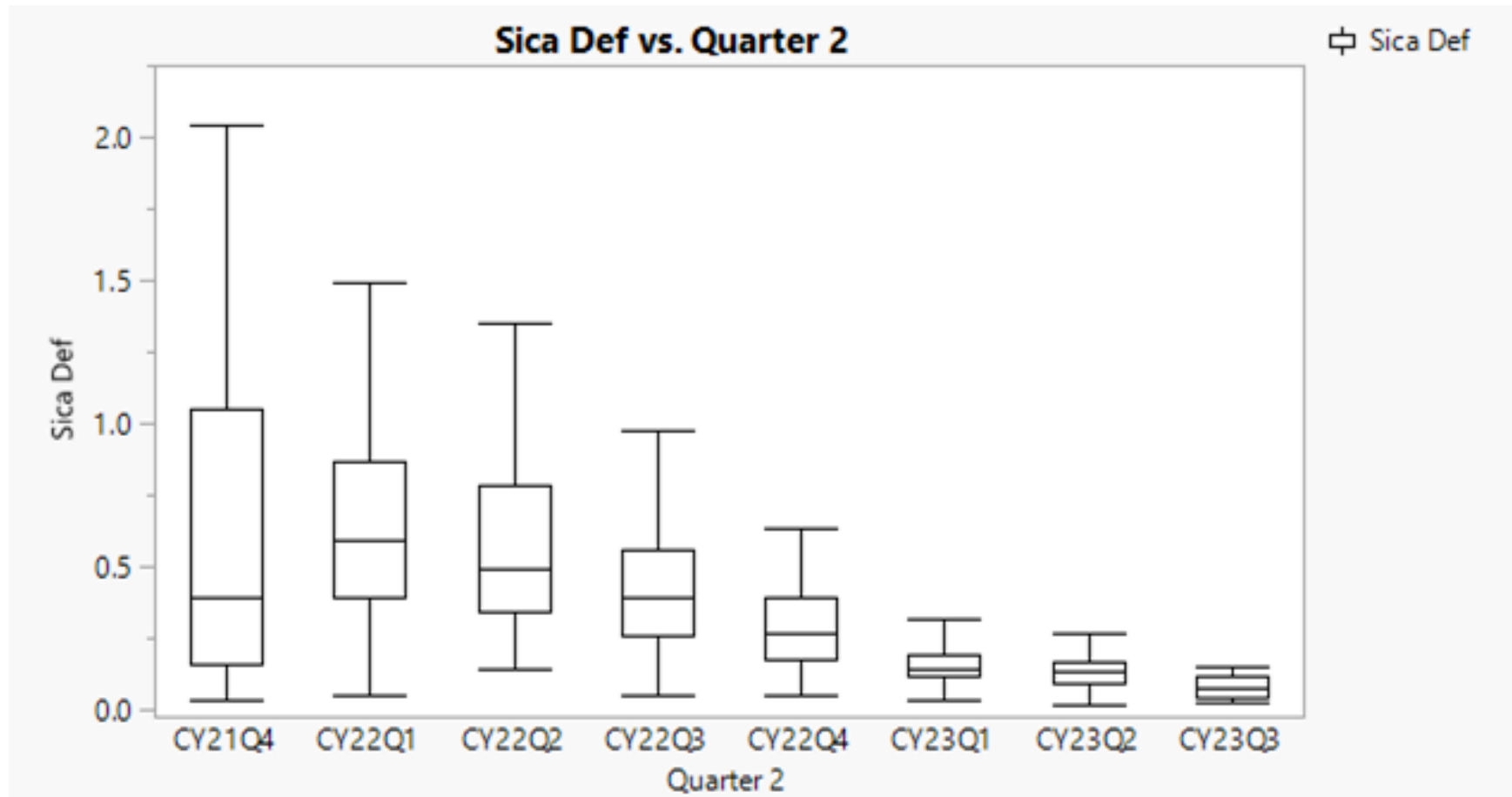
Substrate modeling refined based on estimations and field data

ONE DEVICE GENERATION GAIN BY USING SMARTSIC™



KOH etching and Sica inspection on Bulk 4H-SiC versus SmartSiC™





SiC CLEANING OVERVIEW

SURFACE DEFECTIVITY IMPROVEMENT

PROCESS NEEDS

HIGH PRE

HYDROCARBON
DECONTAMINATION

HIGH MRE

TECHNICAL / ENVIRONMENTAL CONSTRAINTS

NO LIFTOFF, NO SiC ETCHING WITH STD
CHEMICAL & STD CONCENTRATION AND
TEMPERATURE

No SPM

NO SPM
GRINDING METALLIC CONTAMINATION
 $E13 \text{ ATOMS/CM}^2 \rightarrow E10 \text{ ATOMS/CM}^2$

PROPOSAL / STRATEGY

SCRUBBER USAGE BEFORE WETBENCH
DISSOLVE PARTICLES

DiO3

STRONG CHEMICAL
VPD MONITORING ON SiC
HYDROPHILIC SURFACE

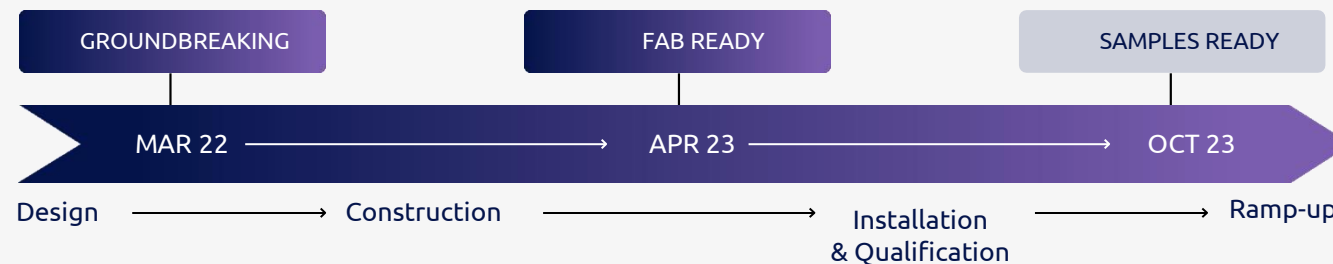
SUSTAINABLE SOLUTIONS TO ADDRESS THE CHALLENGES OF SiC

Surface Defectivity Improvement

- Scrubber PRE optimization using Screen acceleration tube upgraded (AT 2.5)
 - Same PRE @ -30% N2, or Higher PRE @ same N2 flow + throughput gain
- Ozoner idle flow management (UPW saving : 20lpm → 3lpm)
- Overflow rinse bath management (UPW saving : 5lpm → 3lpm)
- Hot water rinse management (UPW saving : 12lpm → 3lpm)
- Operation BKM : batch mutualisation (production & qualification) vs automation (multi stage)

SmartSiC™ HVM FACTORY

NEW CLEANROOM FOR SmartSiC™ 500kwpy 150/200mm CAPACITY



SmartSiC™

DECISIVE STEP TOWARDS HVM

	~Perfect	Very low	Yes / Ref	200mm □ 300 mm “easy”	IGBT
vs	Crystal	Variability	Availability	Scalability	End-user Benefit
	SiC Like	Reduced	10x SiC / Cash Efficiency	150 □ 200mm “Easy”	>> E Efficiency



ICSCRM 2023

THANK YOU