



SCREEN Laser Annealing Technology for the next generation of Semiconductor

November 16th, 2023

SCREEN Semiconductor Solutions Co., Ltd.



The names of company or products or services, etc. on this document are the trademarks or registered trademarks of their respective companies.

Although "TM" and "®" may not be specified in this document, it is prohibited by the Trademark Law, etc. to use them without the permission of each right holder.

本資料に記載の会社名、製品名、サービス名等は、各社の商標または登録商標です。

本資料上では「TM」「®」を明記していない場合もありますが、これらを各権利者の許諾なしに使用等することは、商標法等で禁止されています。

SCREEN Group Business & Organization

SCREEN Holdings



Corporate Philosophy

Purpose

Innovation for a Sustainable World

Sharing the Future

Building a better future for society with commitment and integrity

Personal Development

Realizing everyone's full potential through trust and teamwork

The Pursuit of Technological Excellence

Exploring technologies while integrating with innovative collaboration

Founder's Motto

Shi Ko Ten Kai

Broadening everyone's thoughts and horizons for innovation

Business Operating Company

SCREEN Semiconductor Solutions

SCREEN Graphic Solutions

SCREEN Finetech Solutions

SCREEN PE Solutions

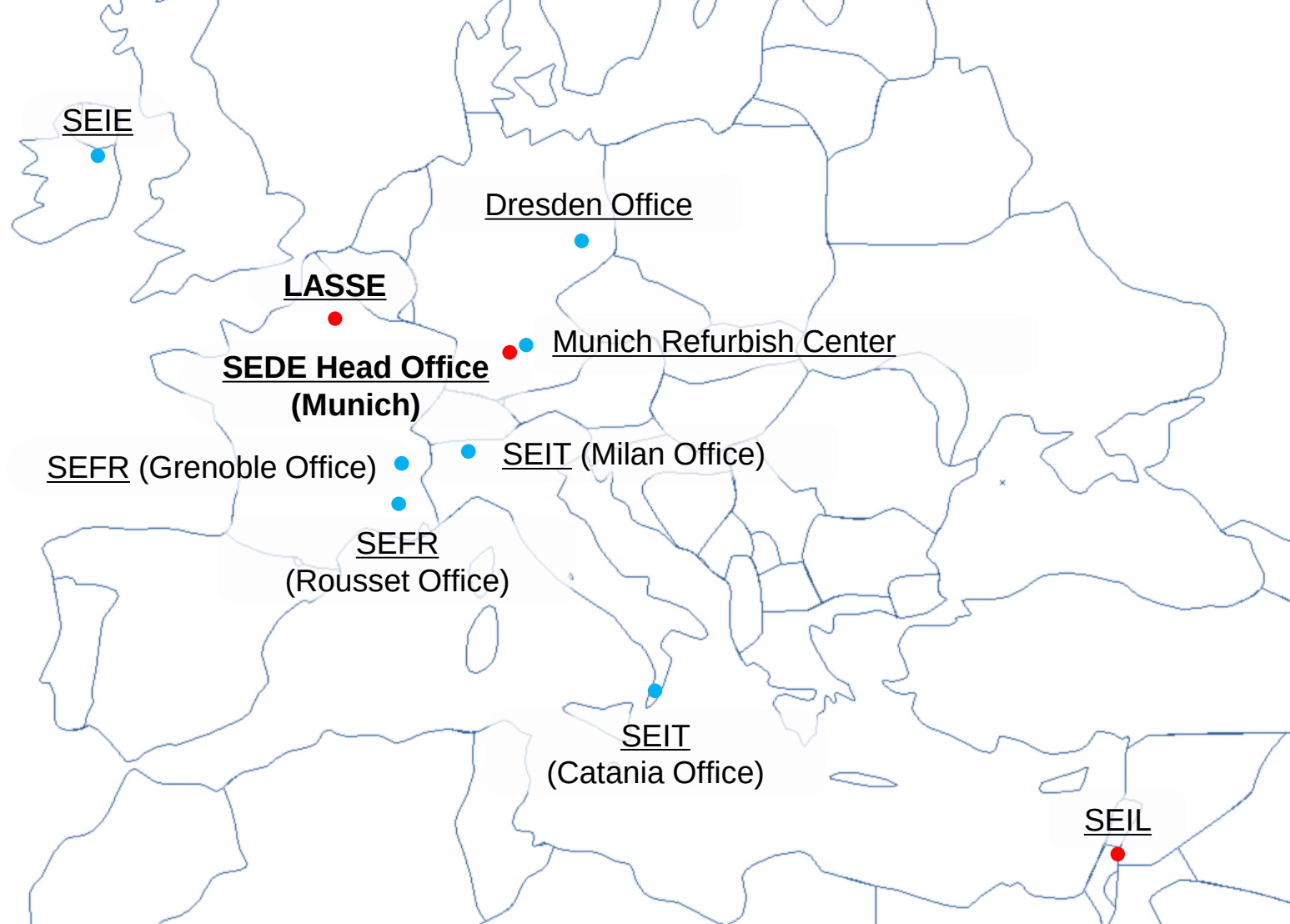
SCREEN Advanced System Solutions

Subsidiaries
of Holding
Company

Functional Support Company

SCREEN IP Solutions

Subsidiaries
of the
Business
Operating
Company



- Head Office
- Other Office

Overseas Bases: Europe



SCREEN SPE Germany GmbH

Laser Systems & Solutions of Europe (LASSE)

SCREEN



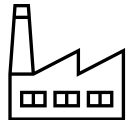
Headquarters: Paris (France)



Development and manufacturing of laser annealing equipment



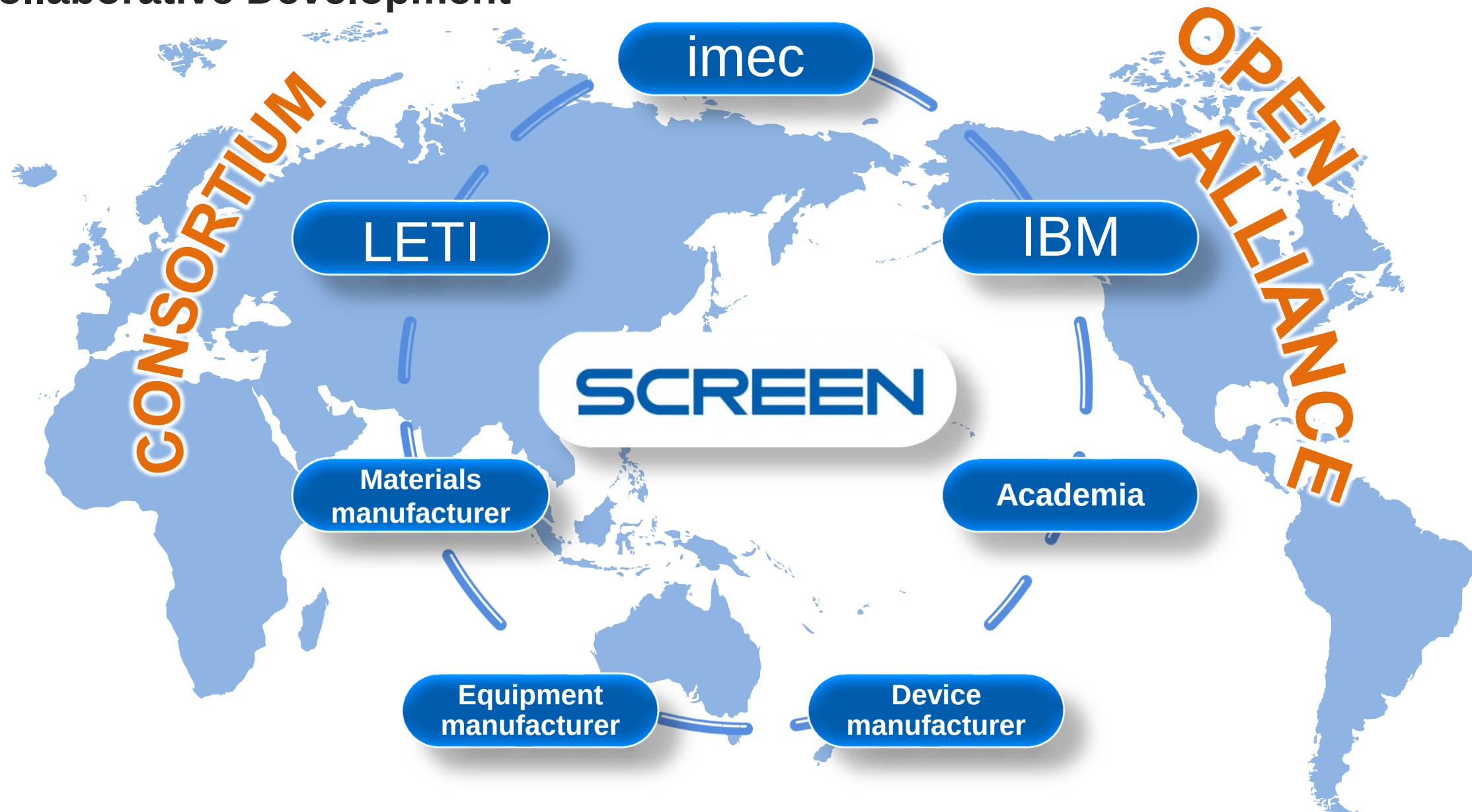
Employees: 60+



Clean Room Area: 2500 m²



Collaborative Development



Future Challenges of Semiconductor Devices

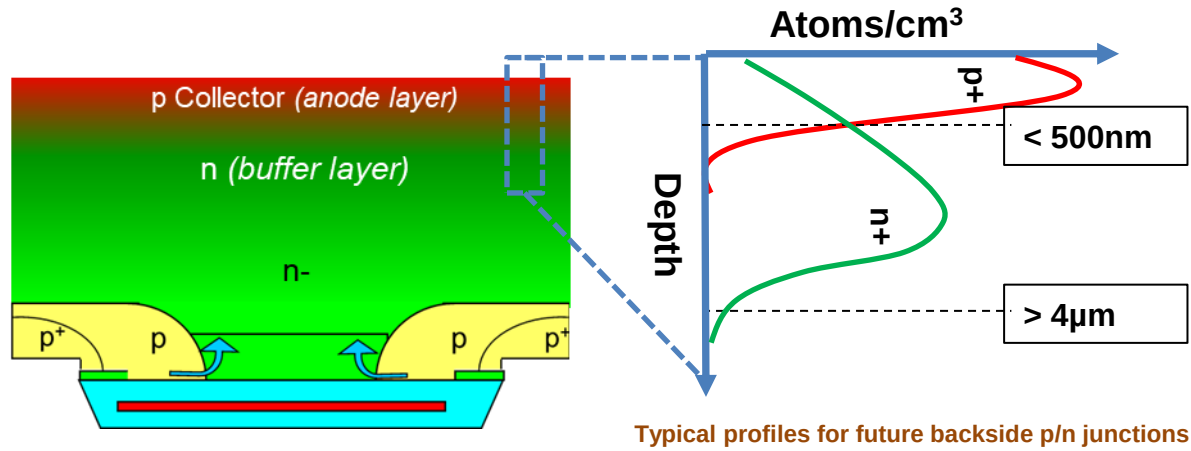
Future Challenges of Semiconductor Devices

Junction Engineering for next generation of Power Devices

Future Challenges of Semiconductor Devices

Junction Engineering for next generation of Power Devices

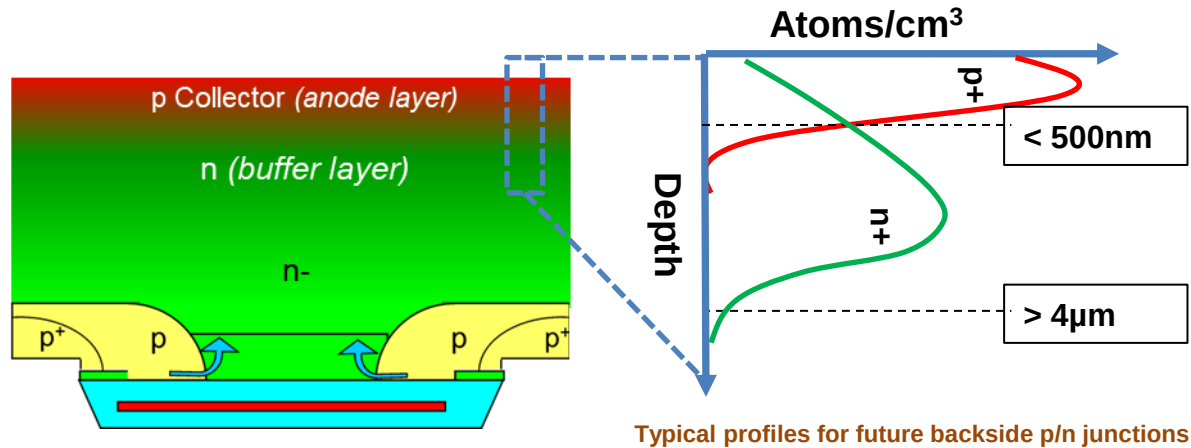
Si IGBT



Future Challenges of Semiconductor Devices

Junction Engineering for next generation of Power Devices

Si IGBT



Challenges:

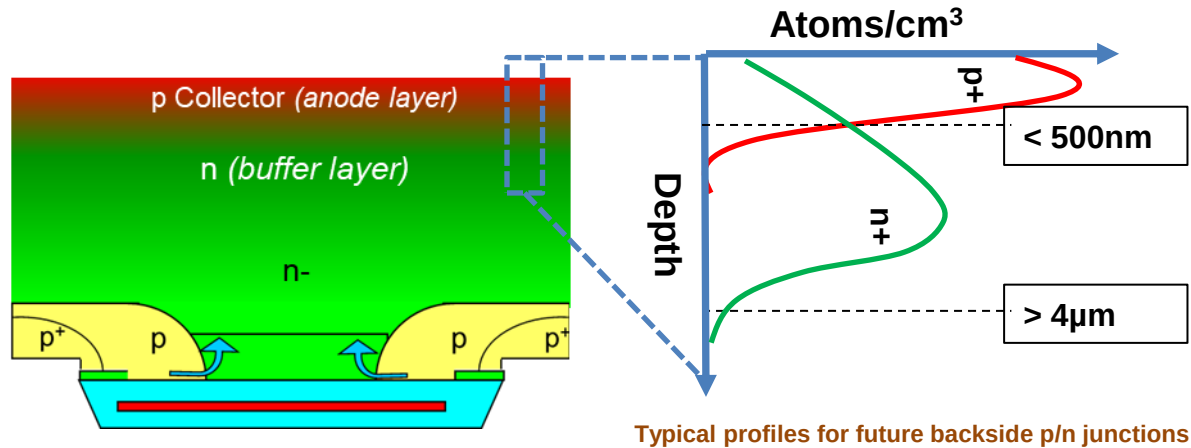
- High-level activation of back-side deep p/n junction
- No dopant diffusion or B/Ph intermixing
- No degradation on Frontside
- Single anneal process

Future Challenges of Semiconductor Devices

Junction Engineering for next generation of Power Devices

Si IGBT

SiC MOSFET



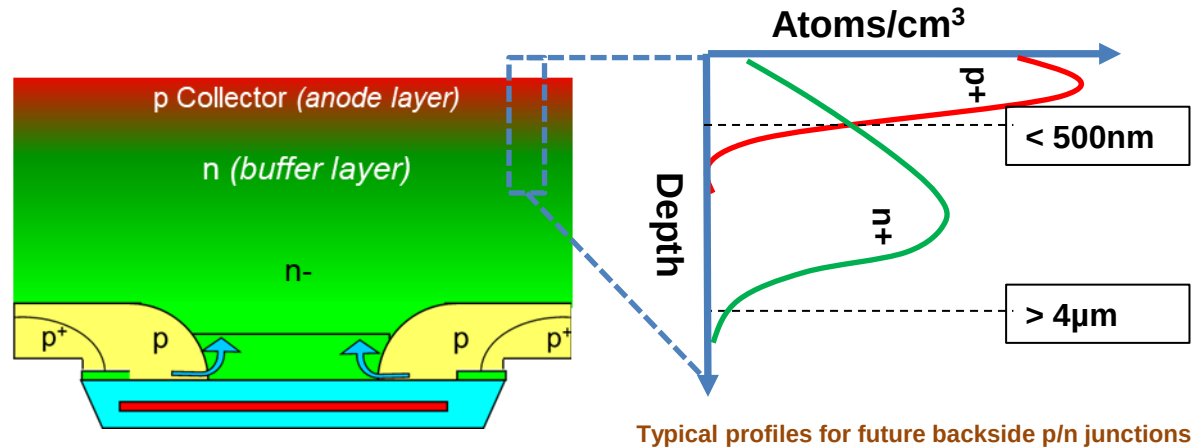
Challenges:

- High-level activation of back-side deep p/n junction
- No dopant diffusion or B/Ph intermixing
- No degradation on Frontside
- Single anneal process

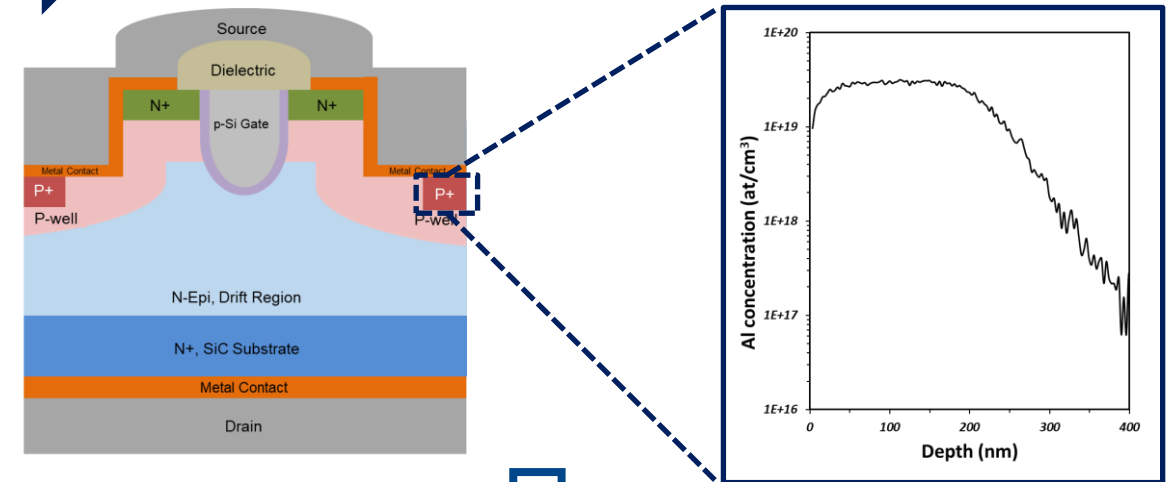
Future Challenges of Semiconductor Devices

Junction Engineering for next generation of Power Devices

Si IGBT



SiC MOSFET



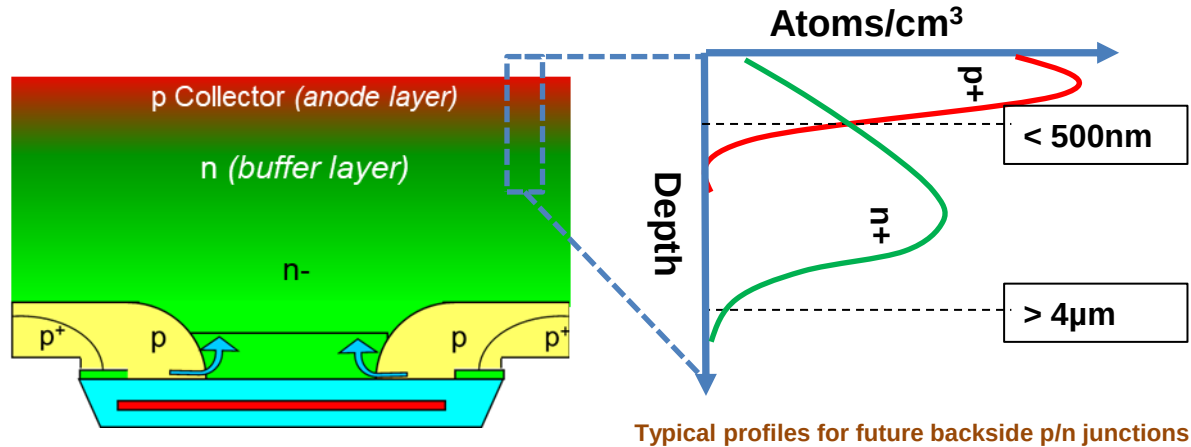
Challenges:

- High-level activation of back-side deep p/n junction
- No dopant diffusion or B/Ph intermixing
- No degradation on Frontside
- Single anneal process

Future Challenges of Semiconductor Devices

Junction Engineering for next generation of Power Devices

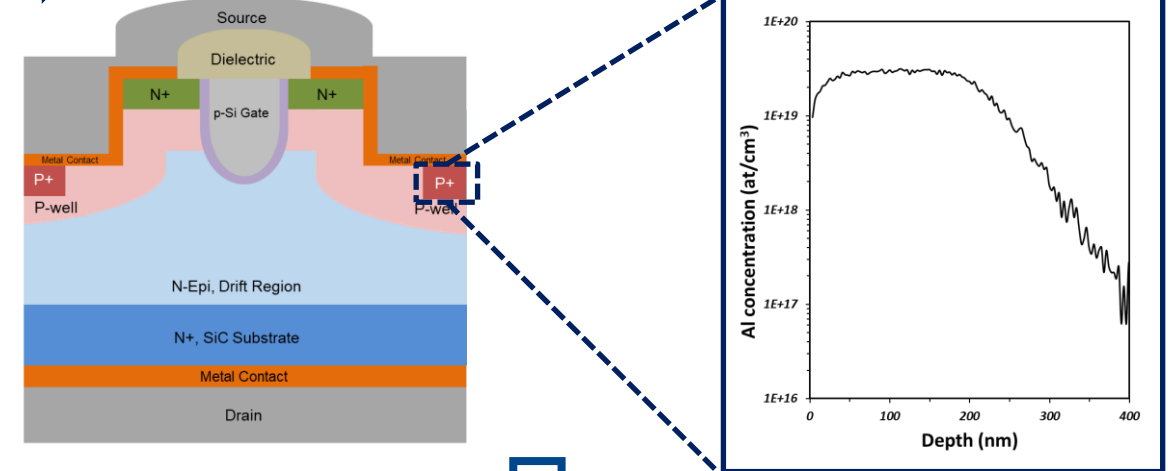
Si IGBT



Challenges:

- High-level activation of back-side deep p/n junction
- No dopant diffusion or B/Ph intermixing
- No degradation on Frontside
- Single anneal process

SiC MOSFET



Challenges:

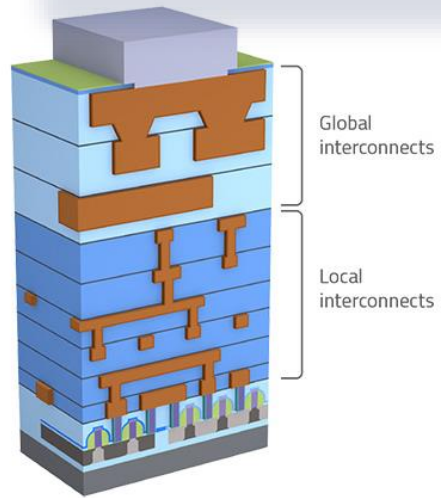
- High level of dopant activation
- Curing of defects generated by implantation
- No generation of extending defects during annealing
- Avoid capping layer during the activation process

Future Challenges of Semiconductor Devices

Interconnects for next generation of advanced CMOS

Future Challenges of Semiconductor Devices

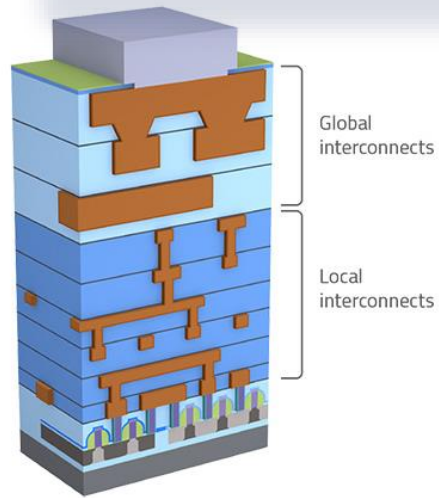
Interconnects for next generation of advanced CMOS



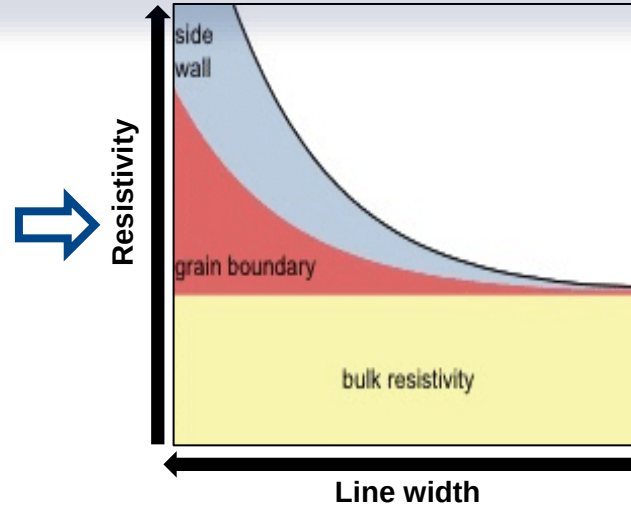
Schematic of next generation of interconnects

Future Challenges of Semiconductor Devices

Interconnects for next generation of advanced CMOS



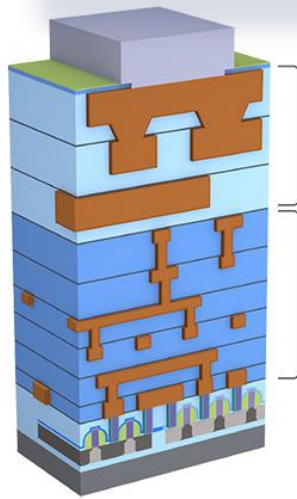
Schematic of next generation of interconnects



Contributors of the dependance of the resistivity to the line dimensions

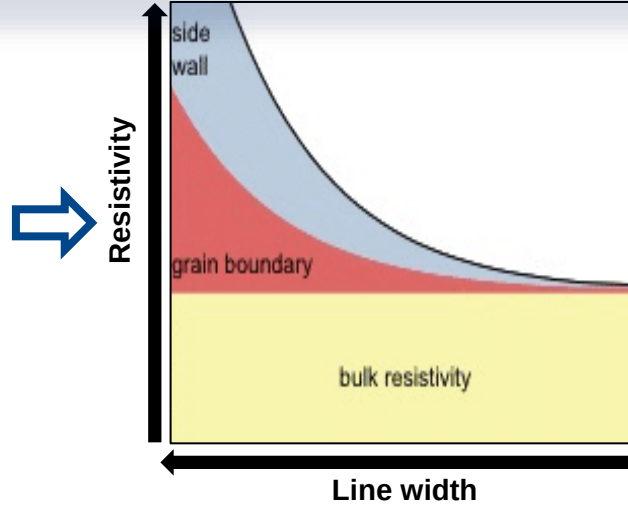
Future Challenges of Semiconductor Devices

Interconnects for next generation of advanced CMOS

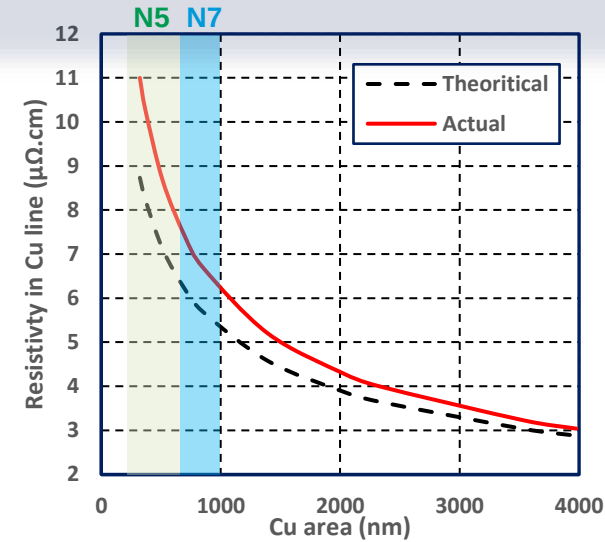


Schematic of next generation of interconnects

Global interconnects
Local interconnects



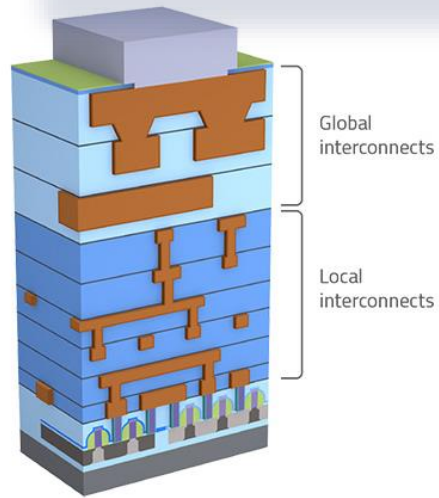
Contributors of the dependance of the resistivity to the line dimensions



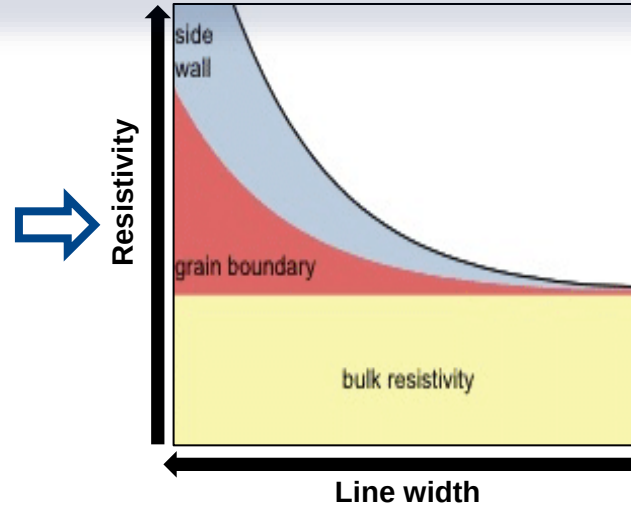
Theoretical and actual performances of Copper

Future Challenges of Semiconductor Devices

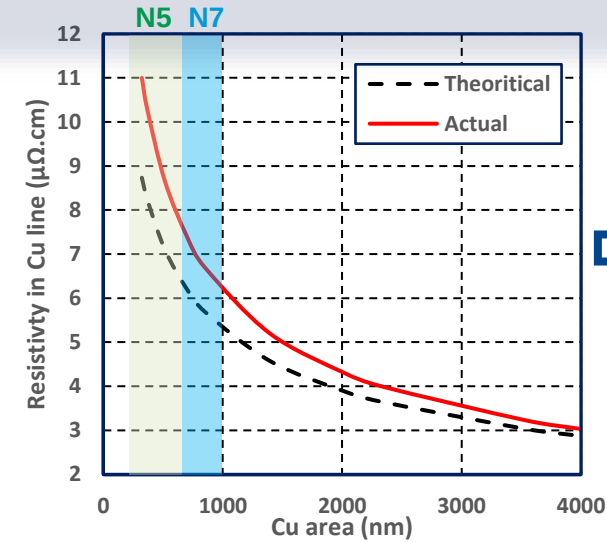
Interconnects for next generation of advanced CMOS



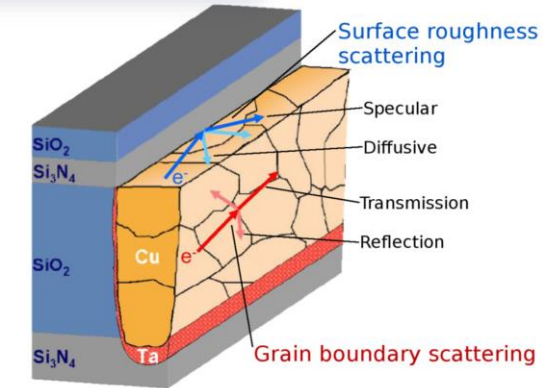
Schematic of next generation of interconnects



Contributors of the dependance of the resistivity to the line dimensions



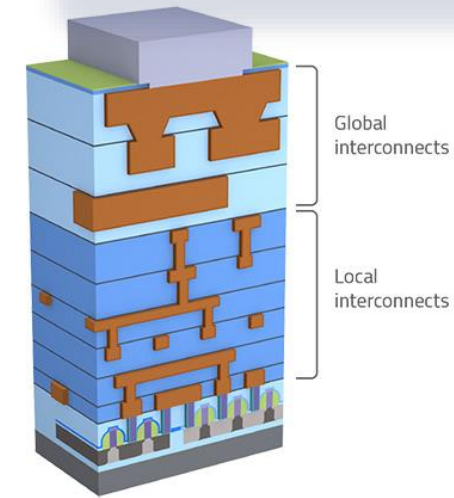
Theoretical and actual performances of Copper



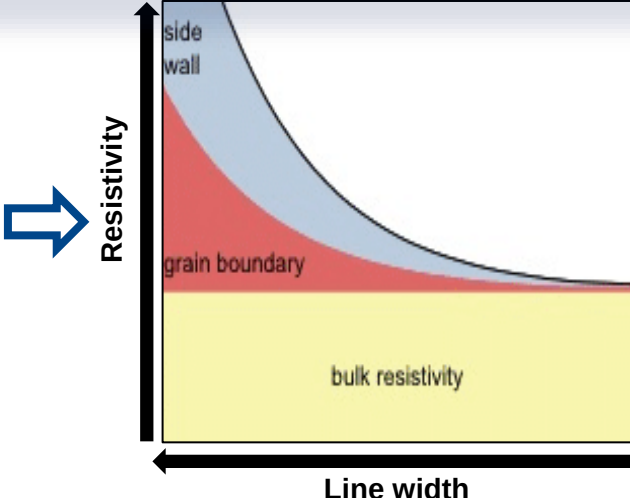
Representation of the different scattering phenomena

Future Challenges of Semiconductor Devices

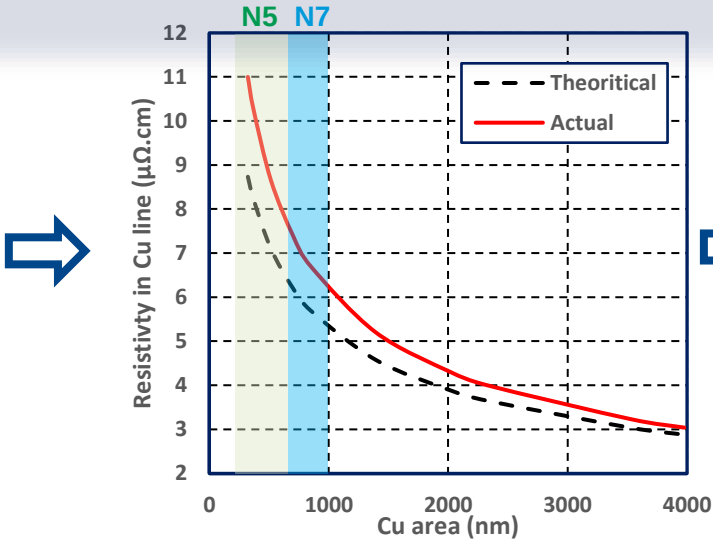
Interconnects for next generation of advanced CMOS



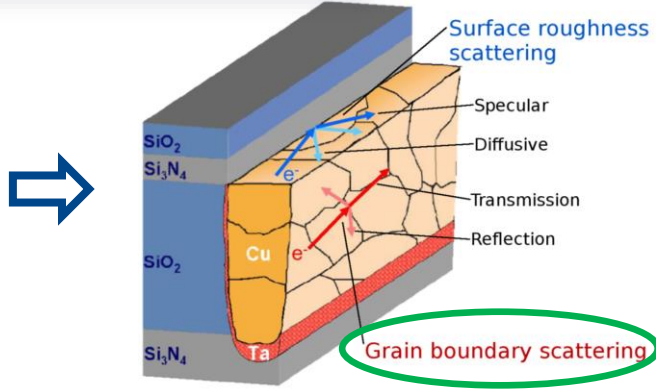
Schematic of next generation of interconnects



Contributors of the dependence of the resistivity to the line dimensions



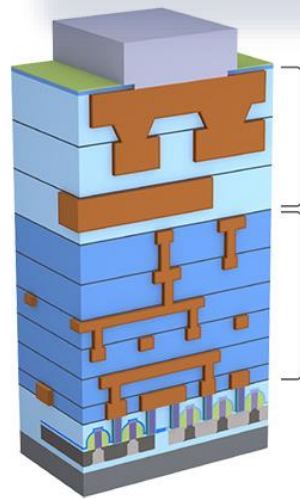
Theoretical and actual performances of Copper



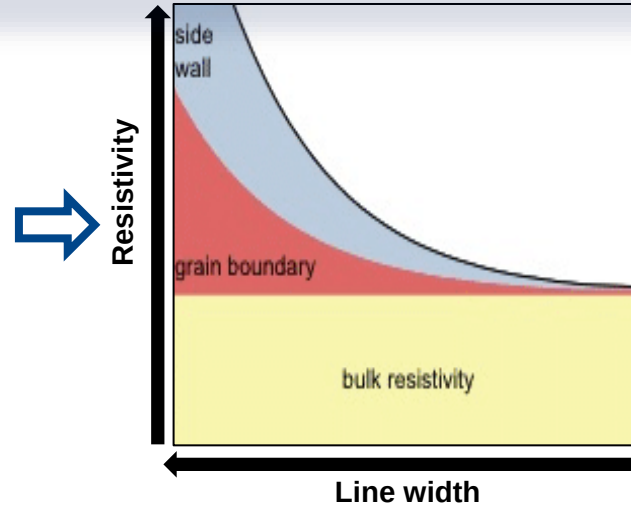
Representation of the different scattering phenomena

Future Challenges of Semiconductor Devices

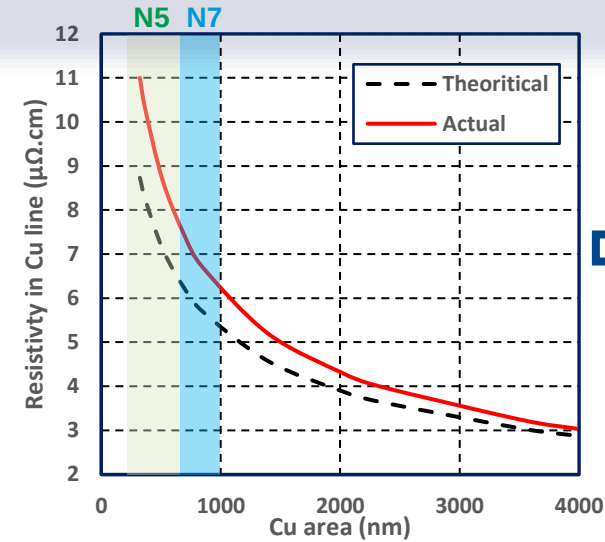
Interconnects for next generation of advanced CMOS



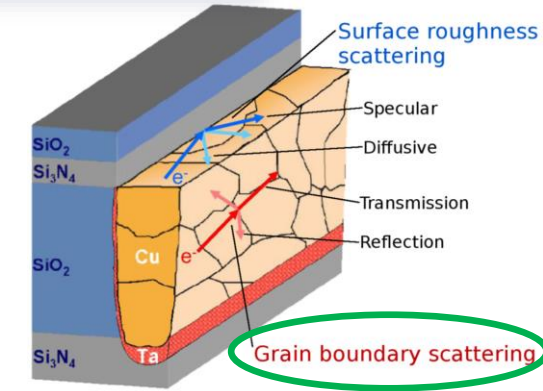
Schematic of next generation of interconnects



Contributors of the dependance of the resistivity to the line dimensions



Theoretical and actual performances of Copper



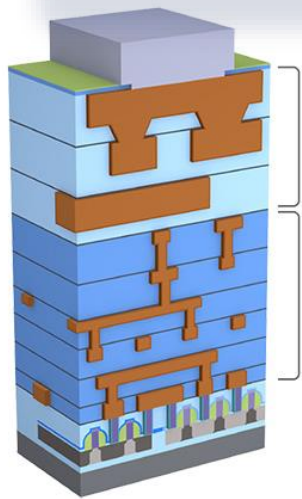
Representation of the different scattering phenomena

Potential Solutions to reduce Grain Boundary Scattering

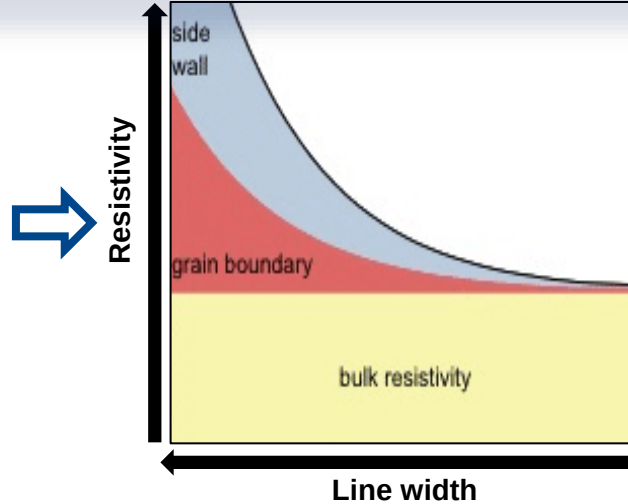
Metal	Bulk Resistivity ($\mu\Omega\cdot\text{cm}$)	e-MFP (nm)
Cu	1.68	39.9
Co	6.2	11.8
Ru	7.8	6.59

Future Challenges of Semiconductor Devices

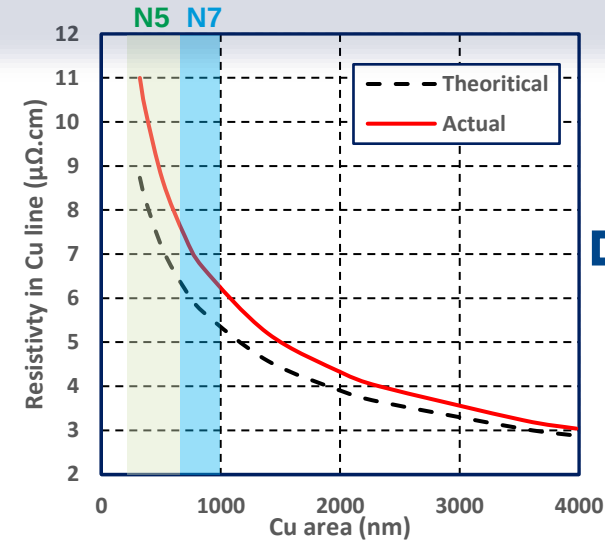
Interconnects for next generation of advanced CMOS



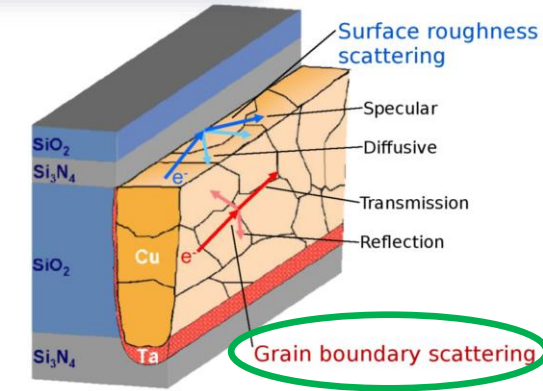
Schematic of next generation of interconnects



Contributors of the dependence of the resistivity to the line dimensions



Theoretical and actual performances of Copper



Representation of the different scattering phenomena

Potential Solutions to reduce Grain Boundary Scattering

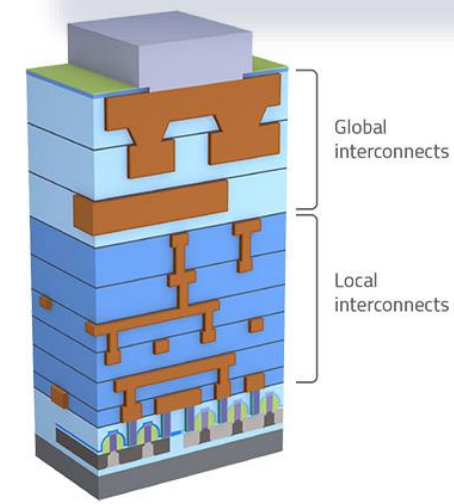
Metal	Bulk Resistivity ($\mu\Omega\cdot\text{cm}$)	e-MFP (nm)
Cu	1.68	39.9
Co	6.2	11.8
Ru	7.8	6.59

e-MFP stands for Electron Mean Free Path

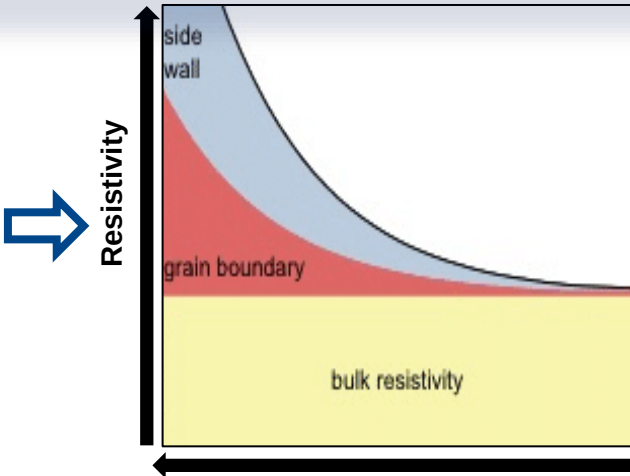
- Enlarge Copper Grain Size > e-MFP (39,9nm)
- Integrate a metal with smaller e-MFP (ie : Ru)

Future Challenges of Semiconductor Devices

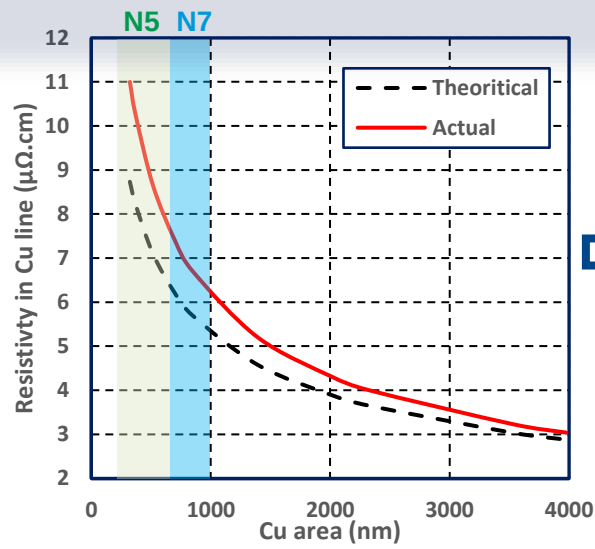
Interconnects for next generation of advanced CMOS



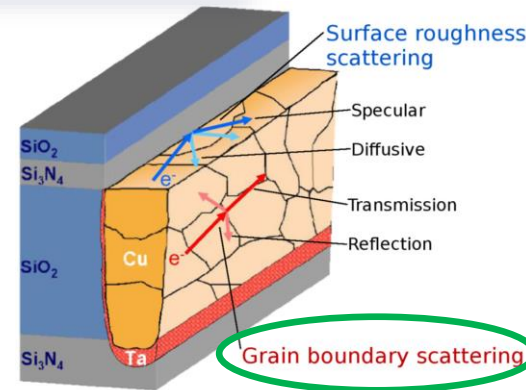
Schematic of next generation of interconnects



Contributors of the dependence of the resistivity to the line dimensions



Theoretical and actual performances of Copper



Representation of the different scattering phenomena

Potential Solutions to reduce Grain Boundary Scattering

Metal	Bulk Resistivity ($\mu\Omega\cdot\text{cm}$)	e-MFP (nm)
Cu	1.68	39.9
Co	6.2	11.8
Ru	7.8	6.59

e-MFP stands for Electron Mean Free Path

- ➔ Enlarge Copper Grain Size > e-MFP (39,9nm)
- ➔ Integrate a metal with smaller e-MFP (ie : Ru)



- Challenges:**
- Sufficient Grain size enlargement
 - No degradation of BEOL structures
 - Thermal budget compatible with FEOL constraints

Future Challenges of Semiconductor Devices

Si IGBT

Interconnects

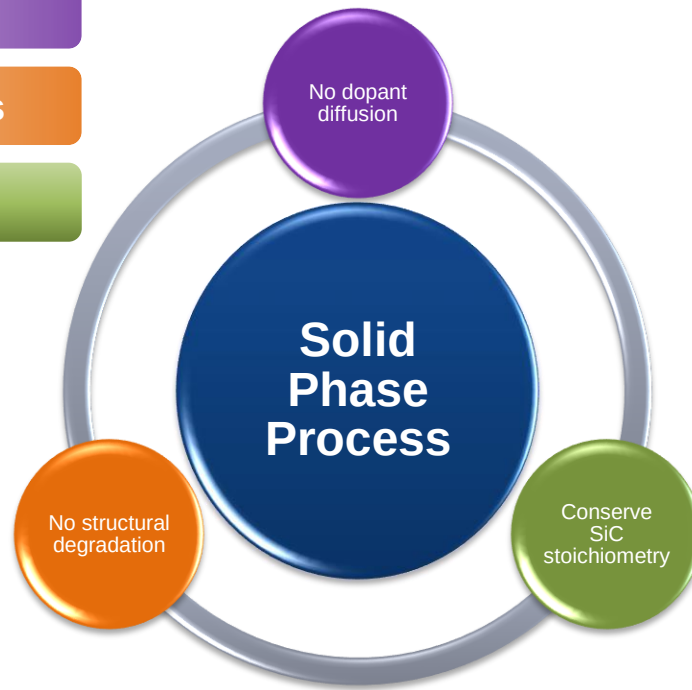
SiC MOSFET

Future Challenges of Semiconductor Devices

Si IGBT

Interconnects

SiC MOSFET

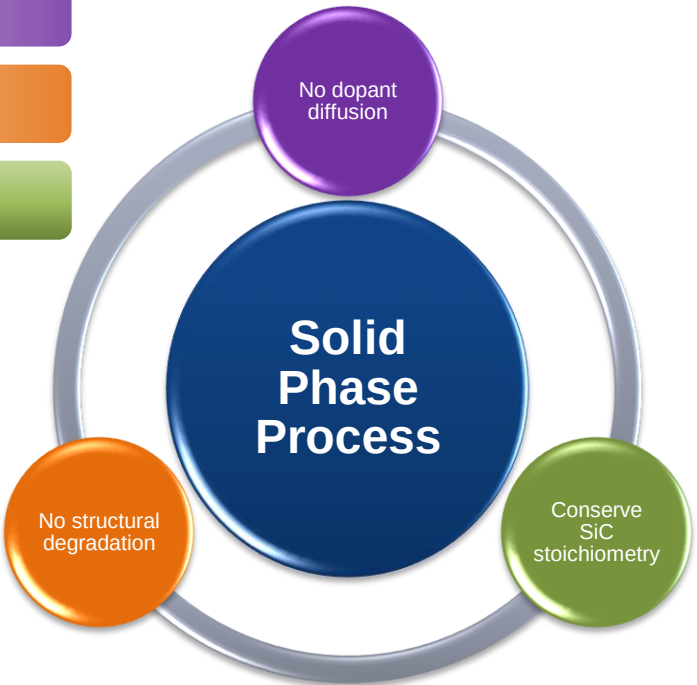


Future Challenges of Semiconductor Devices

Si IGBT

Interconnects

SiC MOSFET

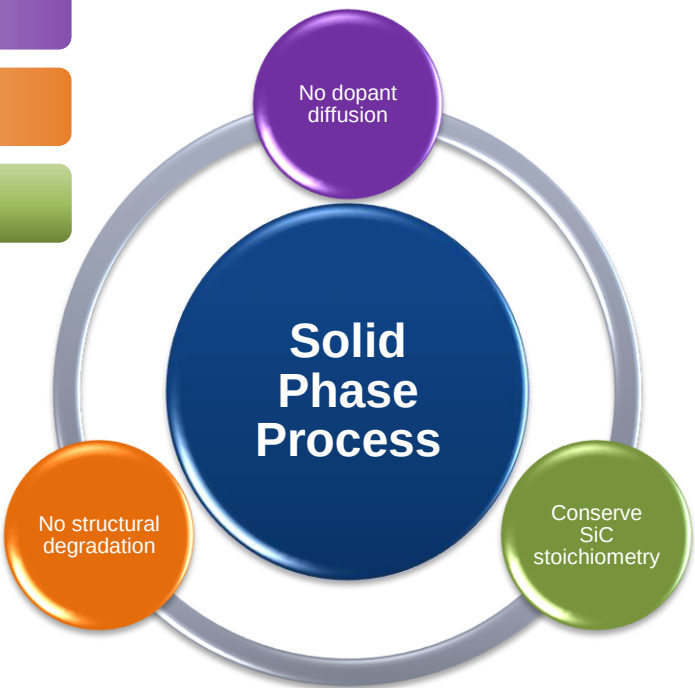


Future Challenges of Semiconductor Devices

Si IGBT

Interconnects

SiC MOSFET

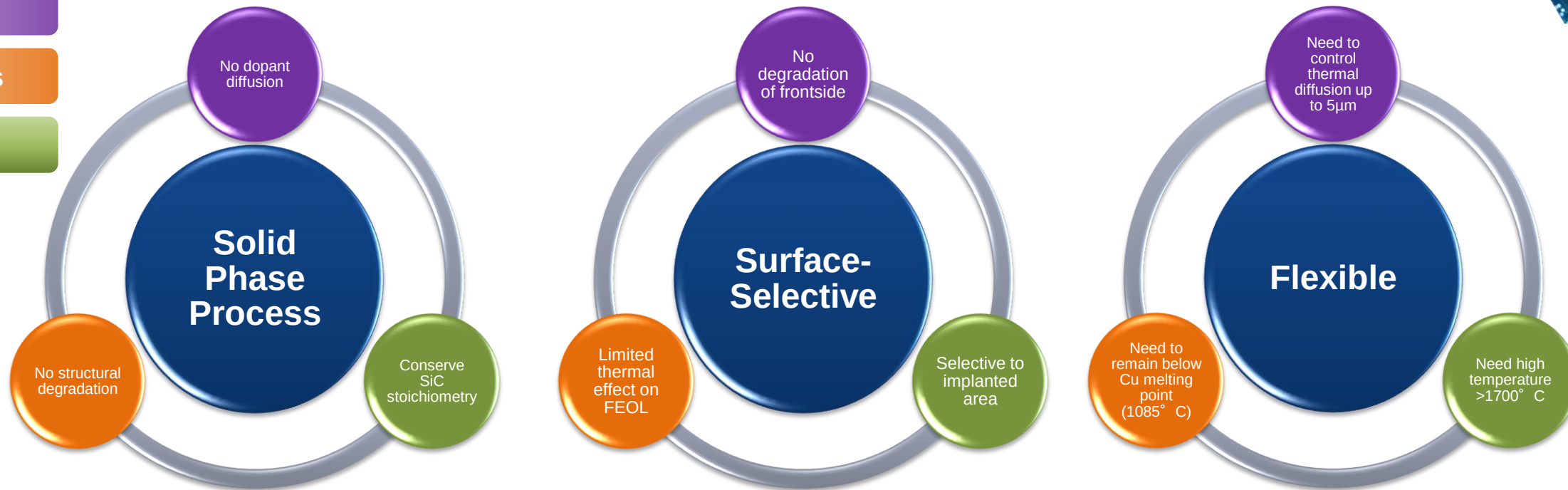


Future Challenges of Semiconductor Devices

Si IGBT

Interconnects

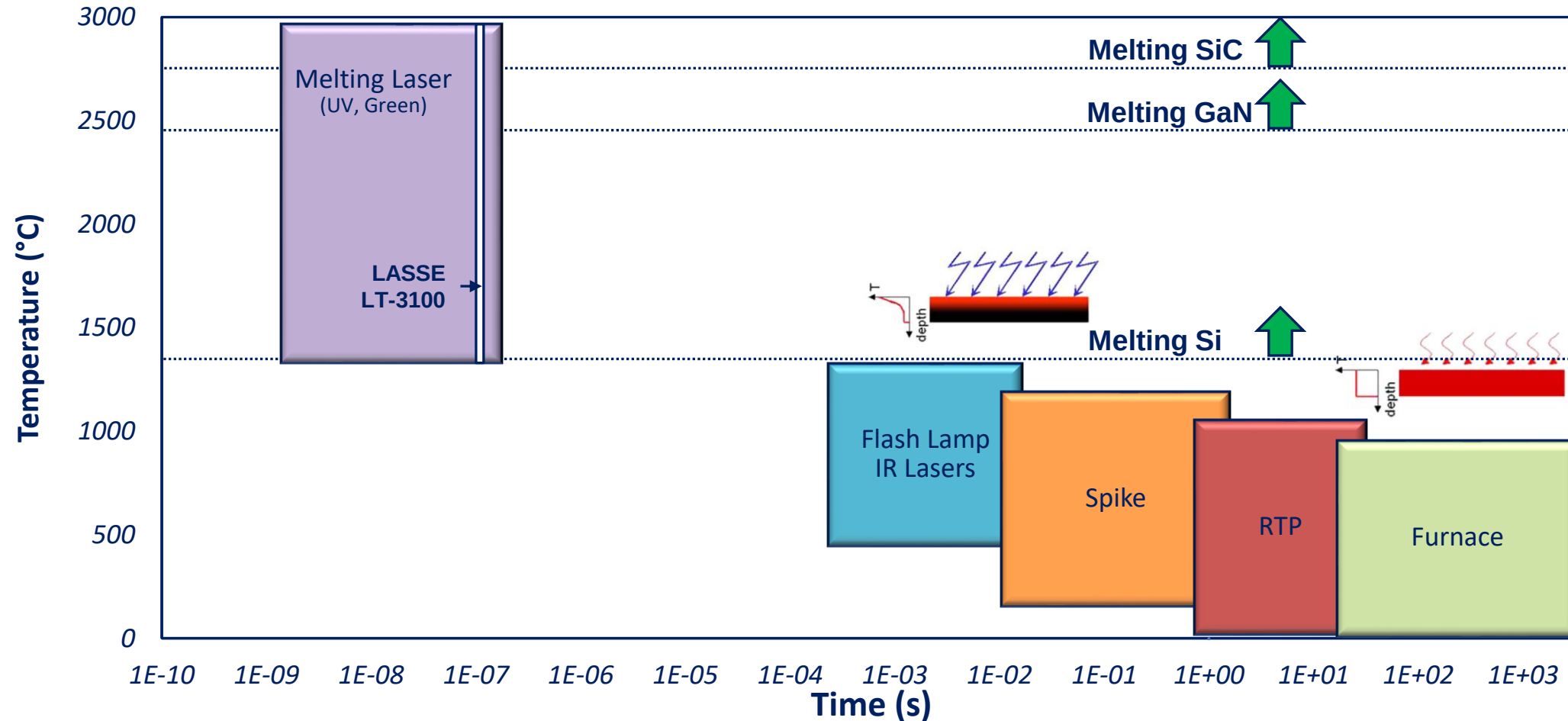
SiC MOSFET



Need to find a thermal annealing solution who can meet all the requirements !

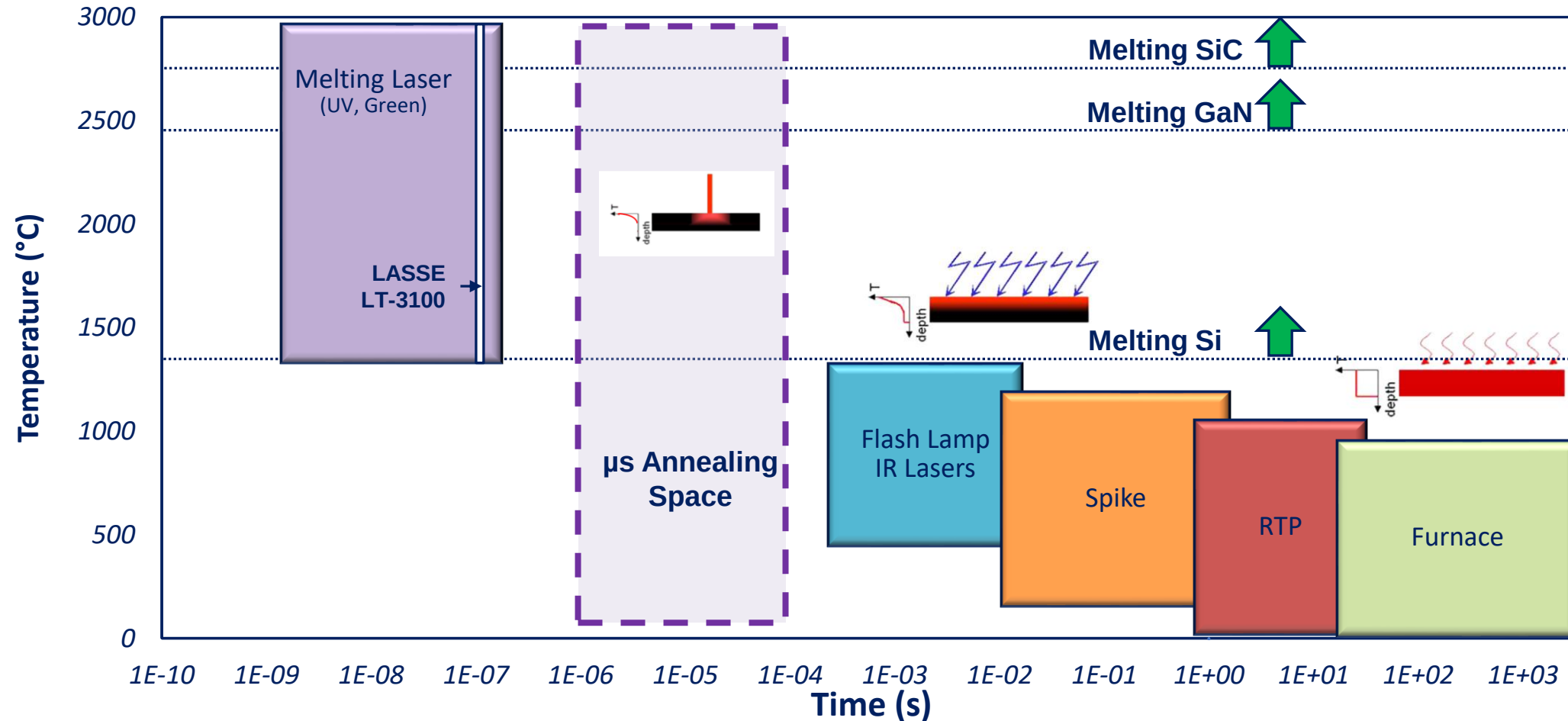
Next generation of Laser Annealer

Screen solution for surface-localized annealing



Screen annealing solution combines the advantages of both longer submelt annealing and laser selective annealing

Screen solution for surface-localized annealing



Screen annealing solution combines the advantages of both longer submelt annealing and laser selective annealing

Advantages of this next generation of laser annealer

Advantages of this next generation of laser annealer

Ultraviolet

Advantages of this next generation of laser annealer

Ultraviolet

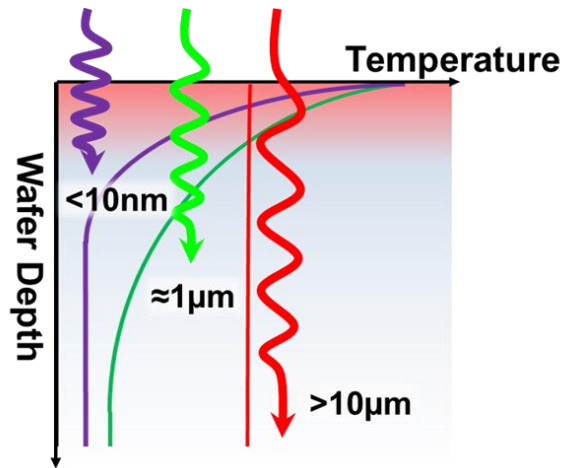


Illustration of absorption depth into the silicon for different wavelengths

Advantages of this next generation of laser annealer

Ultraviolet

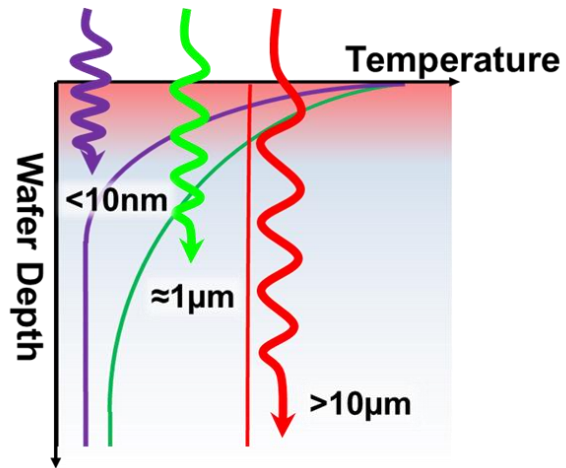
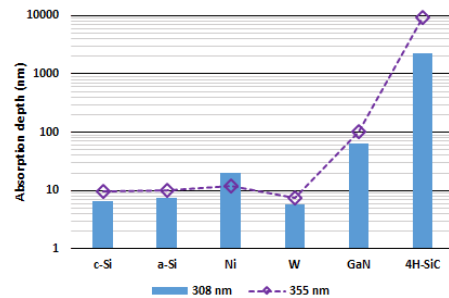


Illustration of absorption depth into the silicon for different wavelengths



Light Absorption depths in UV for different materials

Advantages of this next generation of laser annealer

Ultraviolet



Tunable *Laser Energy Density (ED)*
and μ s-Irradiation time (τ)

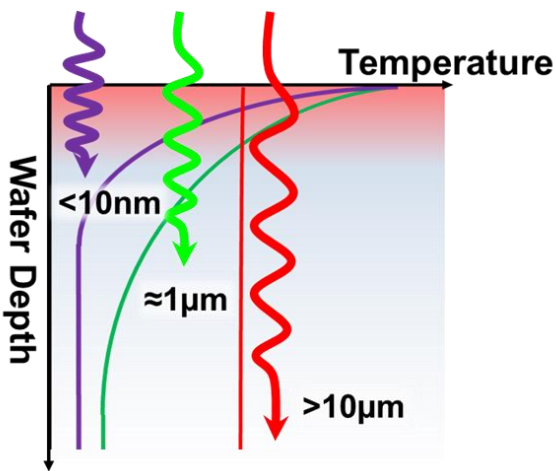
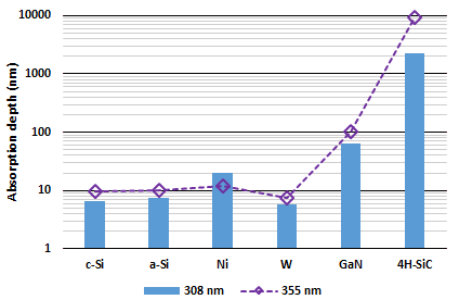


Illustration of absorption depth into the silicon for different wavelengths



Light Absorption depths in UV for different materials

Advantages of this next generation of laser annealer

Ultraviolet



Tunable *Laser Energy Density (ED)*
and μ s-Irradiation time (τ)

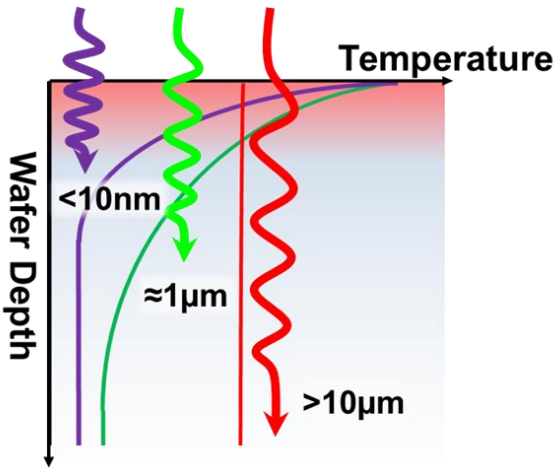
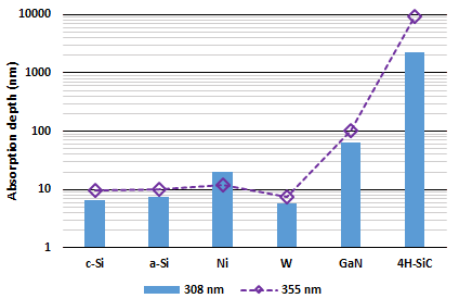
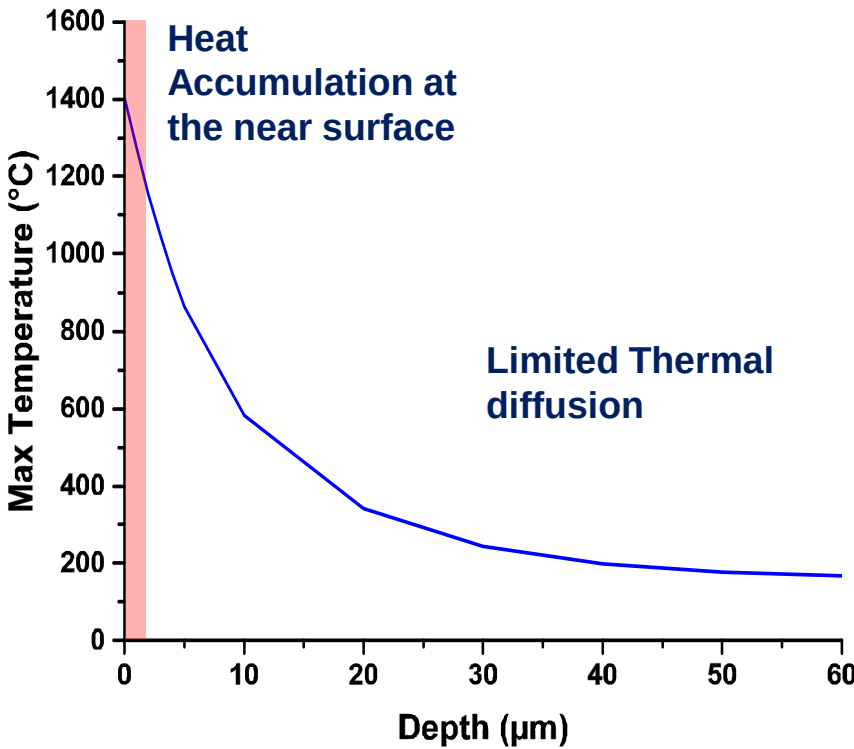


Illustration of absorption depth into the silicon for different wavelengths



Light Absorption depths in UV for different materials



Thermal simulation of a UV-laser obtained by in-house simulation software LIAB

Only Near Surface
Not impact backside

Advantages of this next generation of laser annealer

Ultraviolet



Tunable *Laser Energy Density (ED)*
and μ s-Irradiation time (τ)

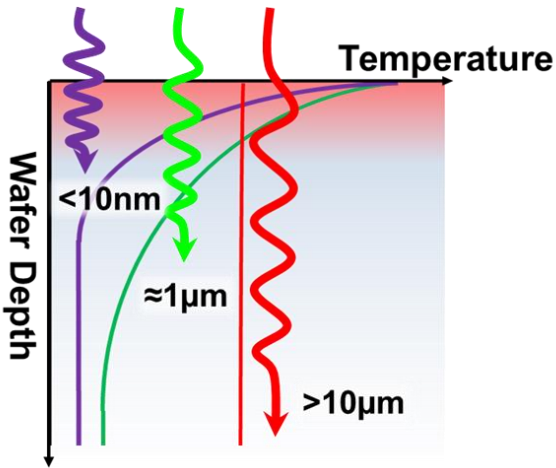
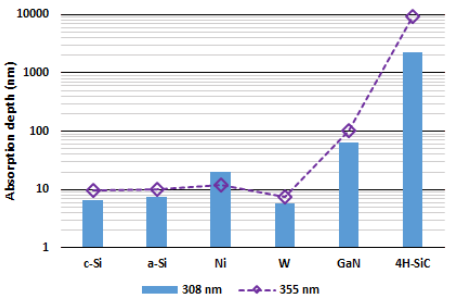
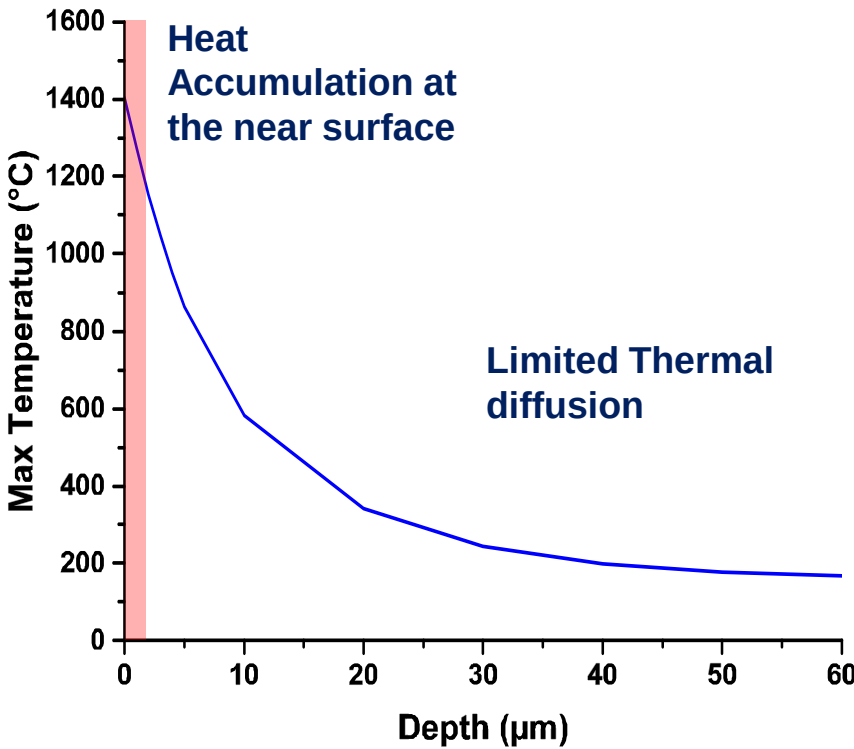


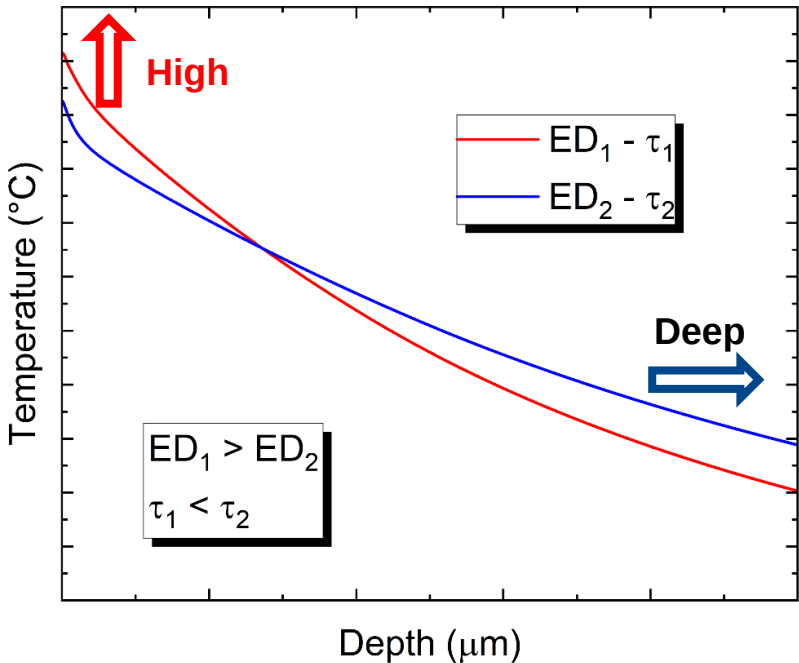
Illustration of absorption depth into the silicon for different wavelengths



Light Absorption depths in UV for different materials



Thermal simulation of a UV-laser obtained by in-house simulation software LIAB



Thermal simulation of a UV-laser obtained by in-house simulation software LIAB

Only Near Surface
Not impact backside



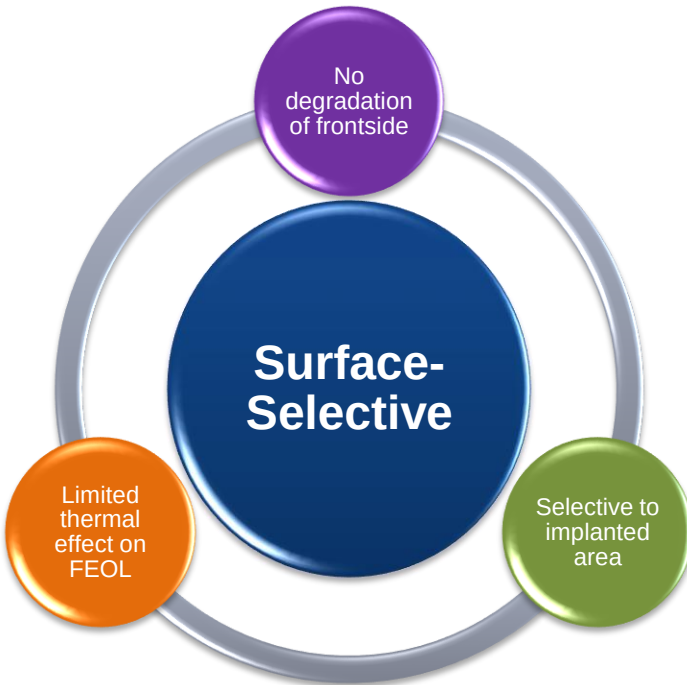
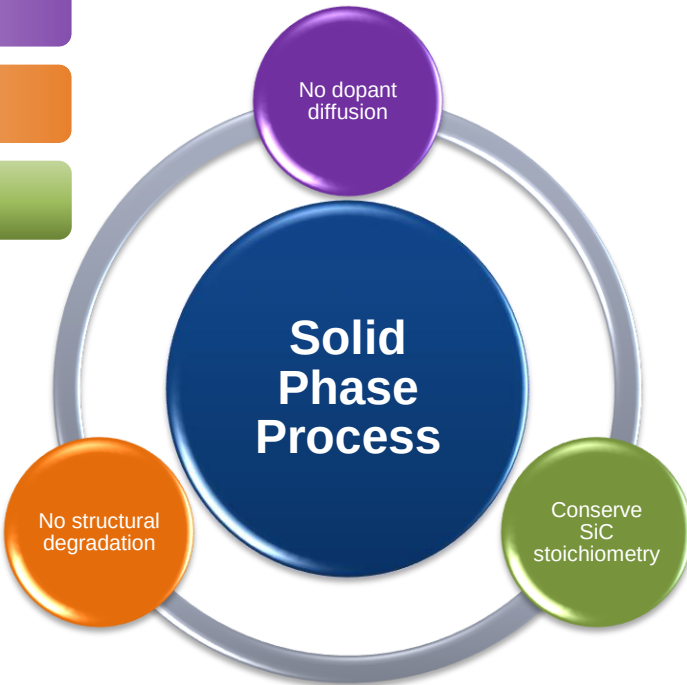
Ultimate control of
temperature profile

Future Challenges of Semiconductor Devices

Si IGBT

Interconnects

SiC MOSFET

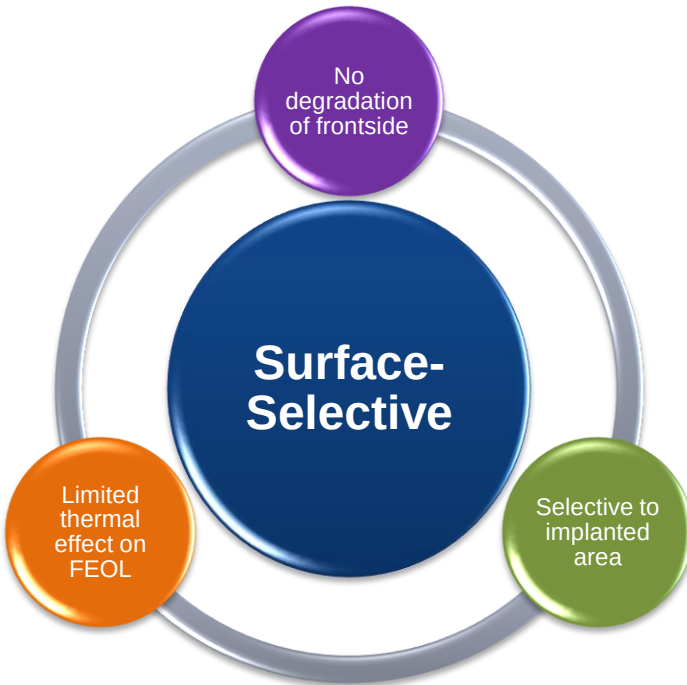
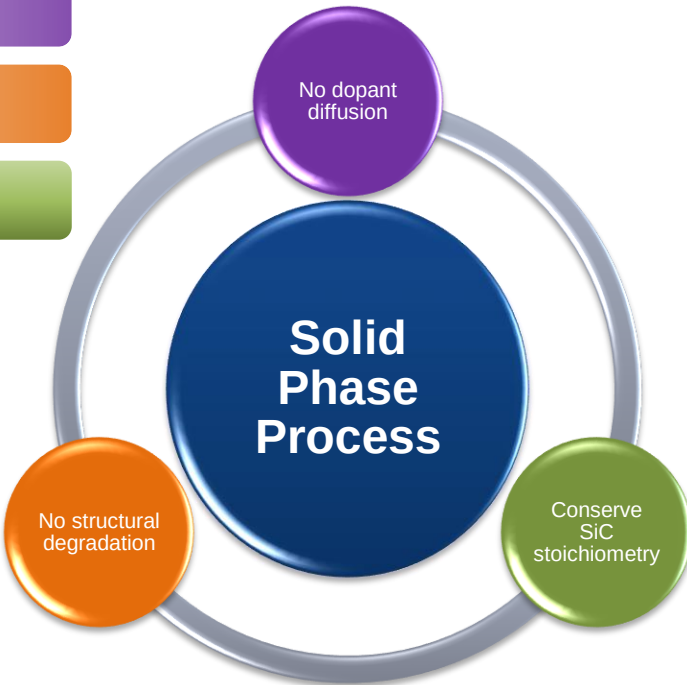


Future Challenges of Semiconductor Devices

Si IGBT

Interconnects

SiC MOSFET



Solid phase process



Surface-Selective



Flexible

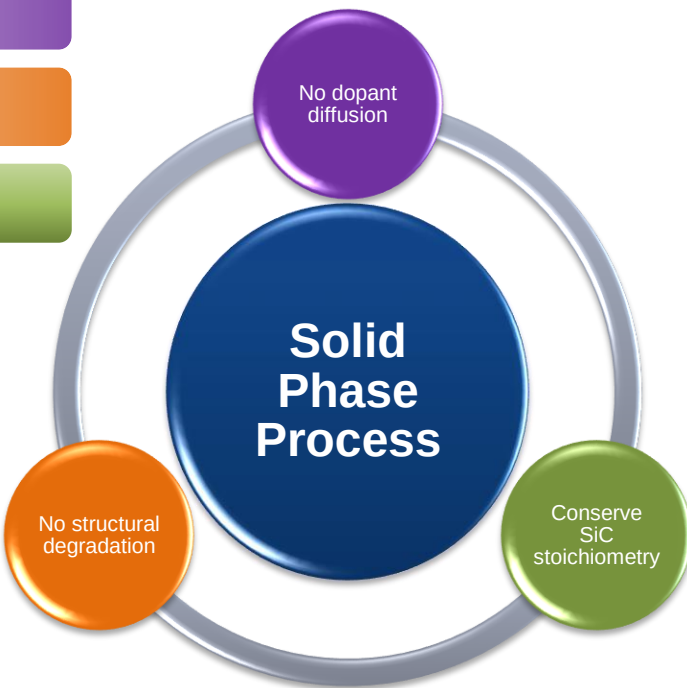


Future Challenges of Semiconductor Devices

Si IGBT

Interconnects

SiC MOSFET



Solid phase process



Surface-Selective



Flexible



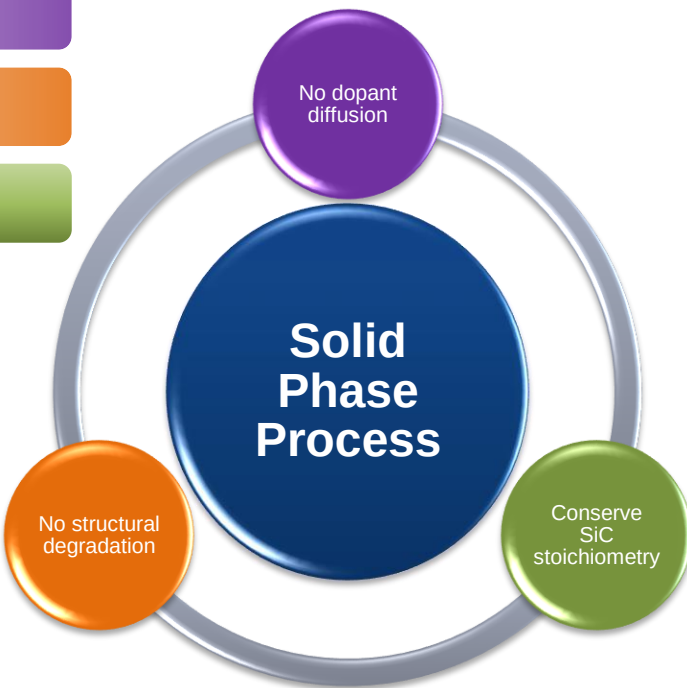
From simulations, this new generation of laser annealer can fulfill all these requirements

Future Challenges of Semiconductor Devices

Si IGBT

Interconnects

SiC MOSFET



Solid phase process



Surface-Selective



Flexible



From simulations, this new generation of laser annealer can fulfill all these requirements



Need to experimentally evaluate this new annealing solution

Results with this new generation of UV- Laser Annealer “UV-LA”

Experimental Results – Si IGBT

Junction Engineering for next generation of Power Devices

Experimental Results – Si IGBT

Junction Engineering for next generation of Power Devices

Challenges:

- High-level activation of back-side deep p/n junction
- No dopant diffusion or B/Ph intermixing
- No degradation on Frontside
- Single anneal process

Experimental Results – Si IGBT

Junction Engineering for next generation of Power Devices

- Si substrate
- Deep Ph ion implantation ($R_p \sim 4\mu\text{m}$)
- B ion implantation ($R_p \sim 0.5\mu\text{m}$)
- UV-LA
- Characterization (*SIMS/SRP*)

↓
Process flow used for this work

Challenges:

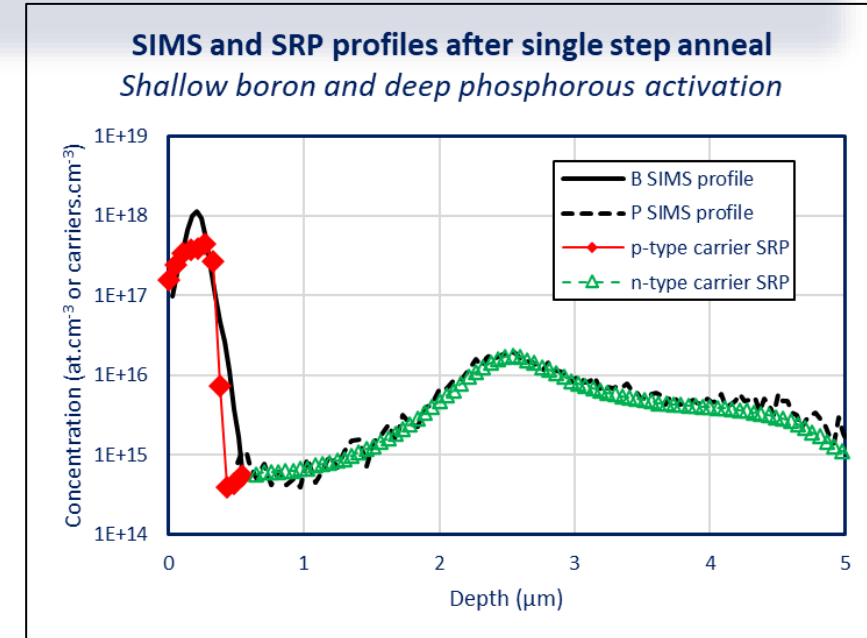
- High-level activation of back-side deep p/n junction
- No dopant diffusion or B/Ph intermixing
- No degradation on Frontside
- Single anneal process

Experimental Results – Si IGBT

Junction Engineering for next generation of Power Devices

- Si substrate
- Deep Ph ion implantation ($R_p \sim 4\mu\text{m}$)
- B ion implantation ($R_p \sim 0.5\mu\text{m}$)
- UV-LA
- Characterization (SIMS/SRP)

Process flow used for this work



Challenges:

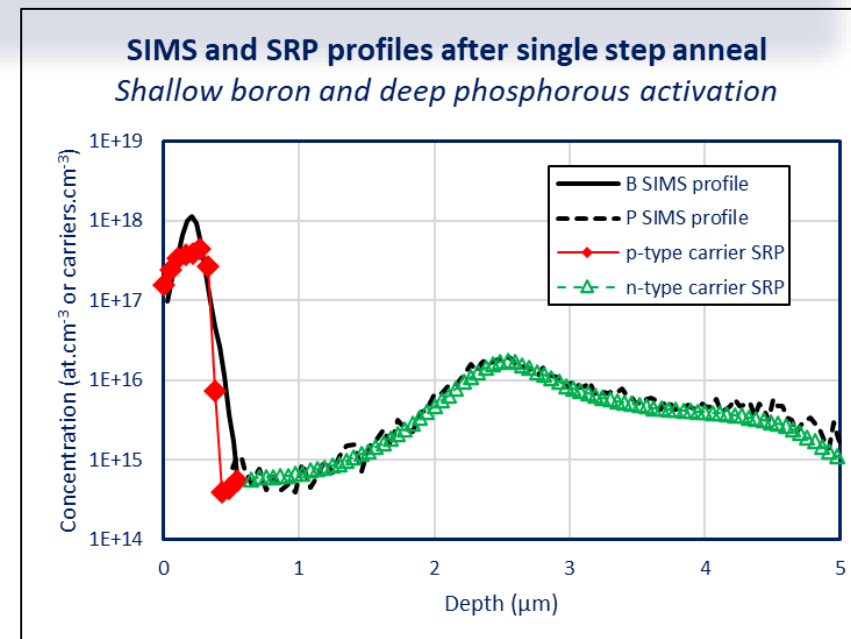
- High-level activation of back-side deep p/n junction
- No dopant diffusion or B/Ph intermixing
- No degradation on Frontside
- Single anneal process

Experimental Results – Si IGBT

Junction Engineering for next generation of Power Devices

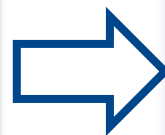
- Si substrate
- Deep Ph ion implantation ($R_p \sim 4\mu\text{m}$)
- B ion implantation ($R_p \sim 0.5\mu\text{m}$)
- UV-LA
- Characterization (SIMS/SRP)

Process flow used for this work



Challenges:

- High-level activation of back-side deep p/n junction
- No dopant diffusion or B/Ph intermixing
- No degradation on Frontside
- Single anneal process



Results:

High Activation ratio for both B and Ph (SRP)
No Intermixing B/Ph observed
No Effect on frontside
Only one single annealing step has been used

Reference: “Single step μs UV laser annealing for Si IGBT back-side activation”, Z. Chehadi, **EMRS2023**

Experimental Results – SiC MOSFET

Junction Engineering for next generation of Power Devices

Experimental Results – SiC MOSFET

Junction Engineering for next generation of Power Devices

Challenges:

- High level of dopant activation
- Curing of defects generated by implantation
- No generation of extending defects during annealing
- Avoid capping layer during the activation process

Experimental Results – SiC MOSFET

Junction Engineering for next generation of Power Devices

- SiC substrate + Epi
- Al Implantation
($R_p \sim 0.2 \mu\text{m}$) $3 \times 10^{16} \text{ at/cm}^2$ & 800°C
- Furnace (w/cap) or UV-LA
- Characterization
TEM/SIMS/Rs/Raman/TW/SMM

Process flow used for this work

Challenges:

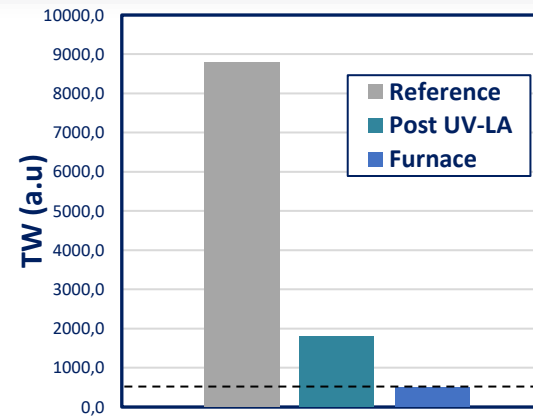
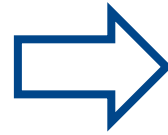
- High level of dopant activation
- Curing of defects generated by implantation
- No generation of extending defects during annealing
- Avoid capping layer during the activation process

Experimental Results – SiC MOSFET

Junction Engineering for next generation of Power Devices

- SiC substrate + Epi
- Al Implantation
($R_p \sim 0.2 \mu\text{m}$) $3 \times 10^{16} \text{ at/cm}^2$ & 800°C
- Furnace (w/cap) or UV-LA
- Characterization
TEM/SIMS/Rs/Raman/TW/SMM

Process flow used for this work



Thermal Wave : Reference vs.
Furnace vs. UV-LA

Challenges:

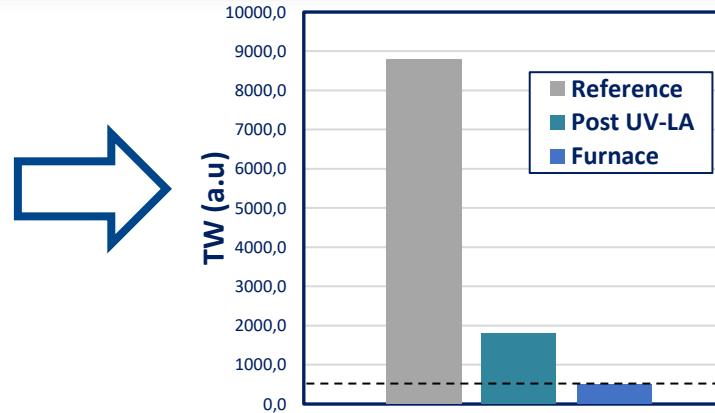
- High level of dopant activation
- Curing of defects generated by implantation
- No generation of extending defects during annealing
- Avoid capping layer during the activation process

Experimental Results – SiC MOSFET

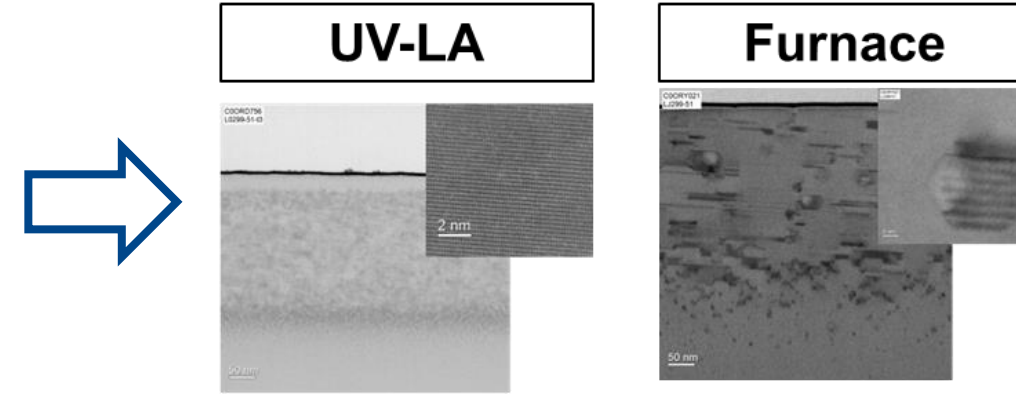
Junction Engineering for next generation of Power Devices

- SiC substrate + Epi
- Al Implantation
($R_p \sim 0.2 \mu\text{m}$) $3 \times 10^{16} \text{ at/cm}^2$ & 800°C
- Furnace (w/cap) or UV-LA
- Characterization
TEM/SIMS/Rs/Raman/TW/SMM

Process flow used for this work



Thermal Wave : Reference vs.
Furnace vs. UV-LA



Cross-TEM: UV-LA vs. Furnace

Challenges:

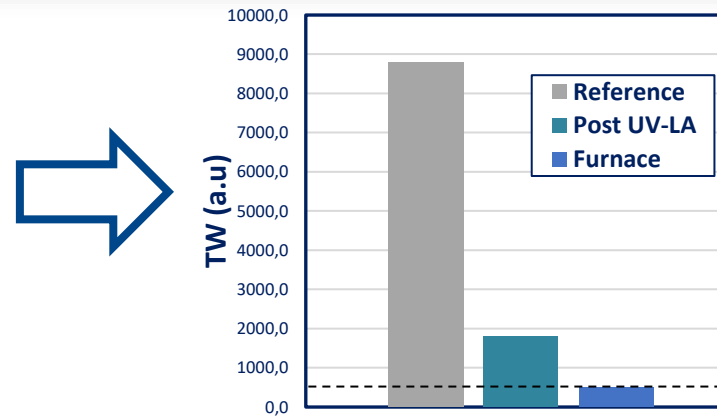
- High level of dopant activation
- Curing of defects generated by implantation
- No generation of extending defects during annealing
- Avoid capping layer during the activation process

Experimental Results – SiC MOSFET

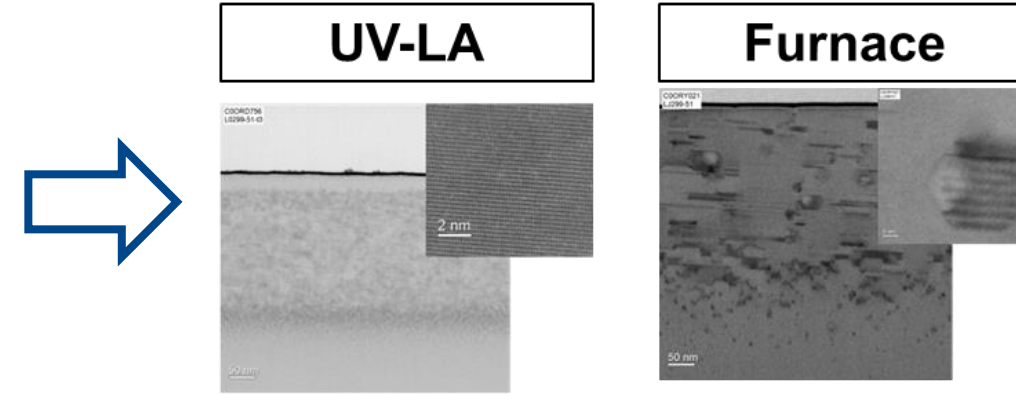
Junction Engineering for next generation of Power Devices

- SiC substrate + Epi
- Al Implantation
($R_p \sim 0.2 \mu\text{m}$) $3 \times 10^{16} \text{ at/cm}^2$ & 800°C
- Furnace (w/cap) or UV-LA
- Characterization
TEM/SIMS/Rs/Raman/TW/SMM

Process flow used for this work



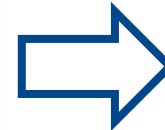
Thermal Wave : Reference vs.
Furnace vs. UV-LA



Cross-TEM: UV-LA vs. Furnace

Challenges:

- High level of dopant activation
- Curing of defects generated by implantation
- No generation of extending defects during annealing
- Avoid capping layer during the activation process



Results:

Sheet Resistance 6 times lower with UV $\mu\text{s-LA}$
 Defect recovery observed by Raman and TW
 No presence of extended defect (TEM)
 No SiC dissociation observed (EDX)

Reference: "Enabling the next generation of SiC devices through low resistivity Al doped layers formed using high dose high temperature Aluminum implants and Laser annealing", F. Mazzamuto, **ICSCRM2023**

Interconnects – Copper

Interconnects for next generation of advanced CMOS

Interconnects – Copper

Interconnects for next generation of advanced CMOS

Challenges:

- Sufficient Grain size enlargement
- No degradation of BEOL structures
- Thermal budget compatible with FEOL constraints

Interconnects – Copper

Interconnects for next generation of advanced CMOS



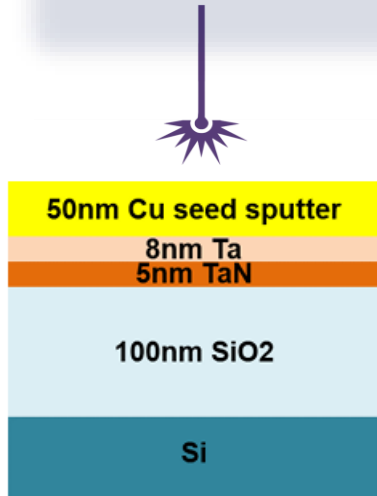
Stack used during this work

Challenges:

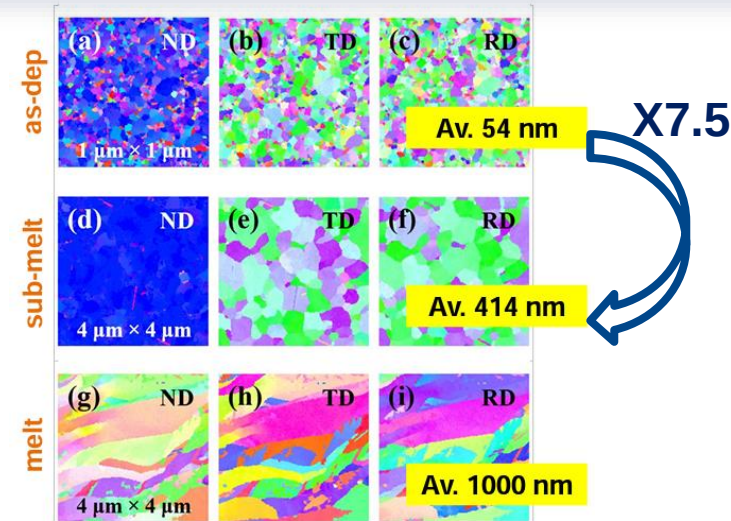
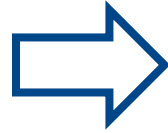
- Sufficient Grain size enlargement
- No degradation of BEOL structures
- Thermal budget compatible with FEOL constraints

Interconnects – Copper

Interconnects for next generation of advanced CMOS



Stack used during this work



Note : $\Sigma 3$ CSL facets considered as grain boundaries.

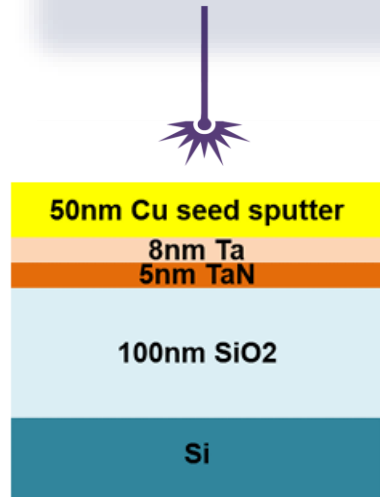
TEM and ED map after UV-LA

Challenges:

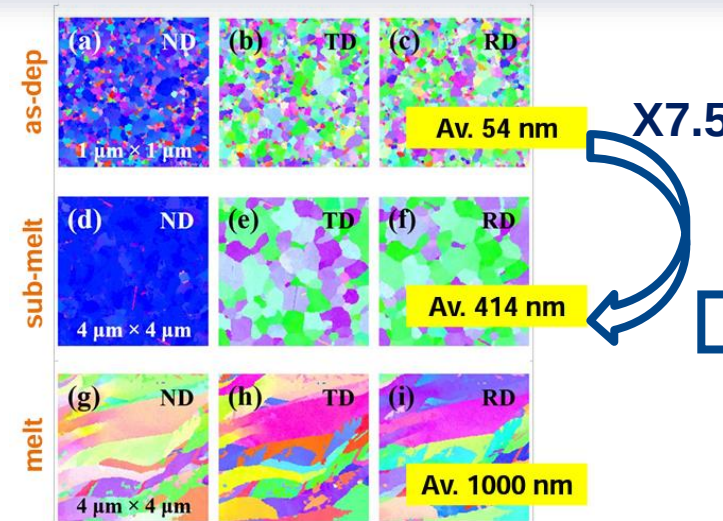
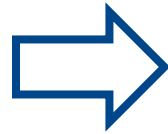
- Sufficient Grain size enlargement
- No degradation of BEOL structures
- Thermal budget compatible with FEOL constraints

Interconnects – Copper

Interconnects for next generation of advanced CMOS



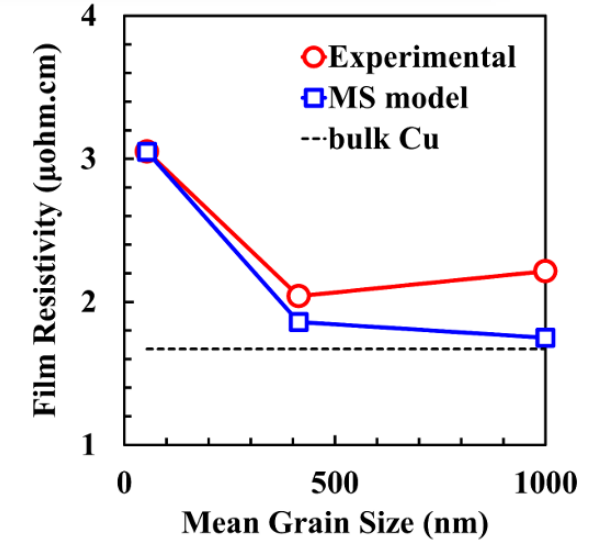
Stack used during this work



Note : Σ 3CSL facets considered as grain boundaries.

TEM and ED map after UV-LA

Almost reach bulk resistivity in submelt regime



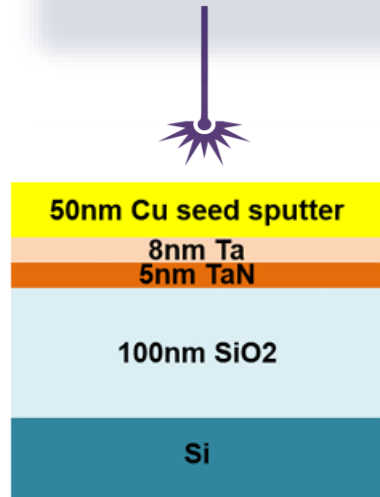
Film resistivity versus grain size after UV-LA

Challenges:

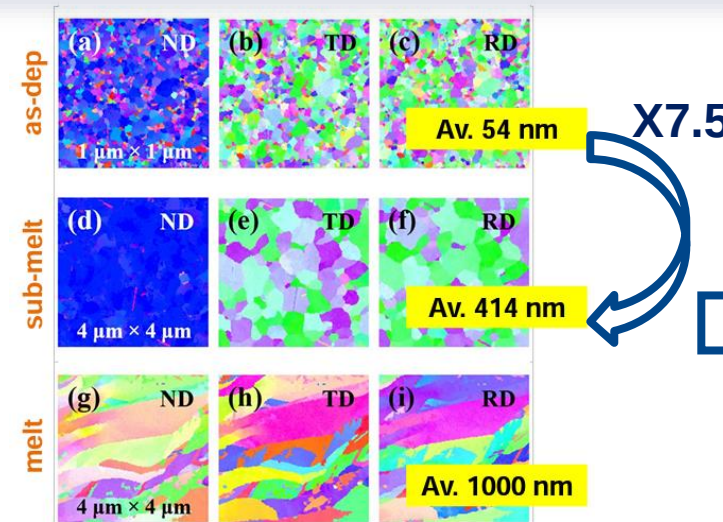
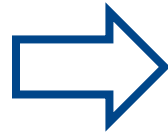
- Sufficient Grain size enlargement
- No degradation of BEOL structures
- Thermal budget compatible with FEOL constraints

Interconnects – Copper

Interconnects for next generation of advanced CMOS



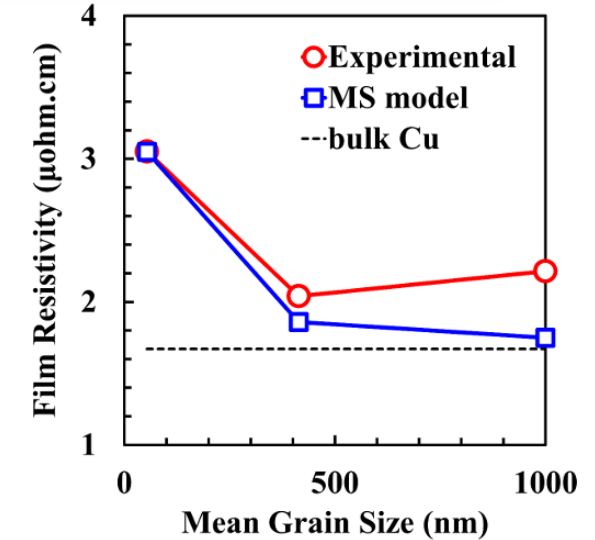
Stack used during this work



Note : $\Sigma 3$ CSL facets considered as grain boundaries.

TEM and ED map after UV-LA

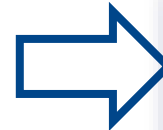
Almost reach bulk resistivity in submelt regime



Film resistivity versus grain size after UV-LA

Challenges:

- Sufficient Grain size enlargement
- No degradation of BEOL structures
- Thermal budget compatible with FEOL constraints



Results:

Grain larger than e-MFP and film thickness
Solid phase confirmed by XRD (no oxidation)
Need to be checked on devices

Reference: "Copper Large-scale Grain Growth by UV Nanosecond Pulsed Laser Anneal", T. Tabata, [IITC2021](#)

Interconnects – Ruthenium

Interconnects for next generation of advanced CMOS

Interconnects – Ruthenium

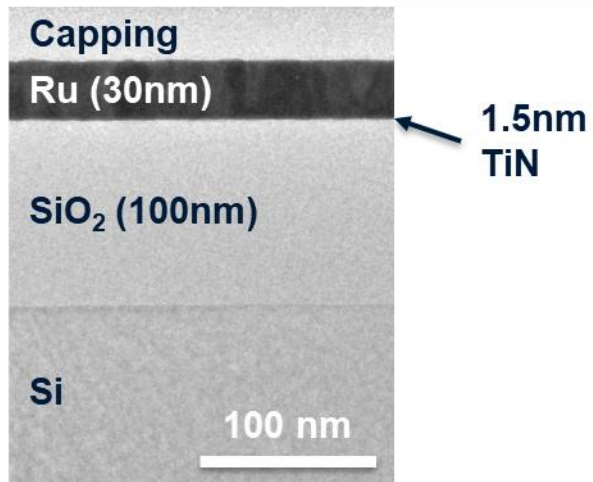
Interconnects for next generation of advanced CMOS

Challenges:

- Sufficient Grain size enlargement
- No degradation of BEOL structures
- Thermal budget compatible with FEOL constraints

Interconnects – Ruthenium

Interconnects for next generation of advanced CMOS



Stack used during this work

Challenges:

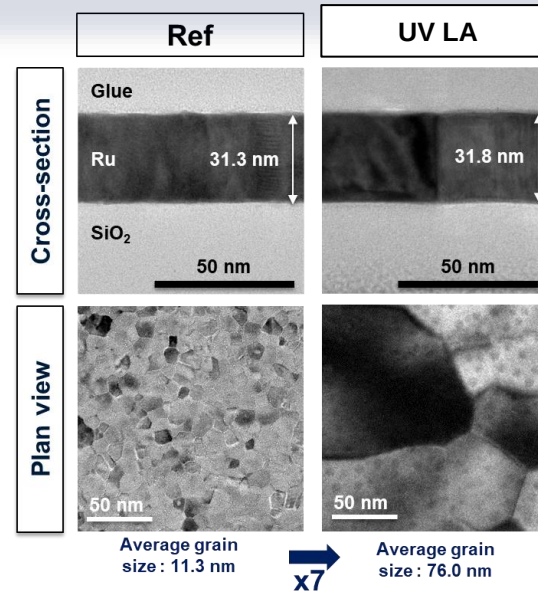
- Sufficient Grain size enlargement
- No degradation of BEOL structures
- Thermal budget compatible with FEOL constraints

Interconnects – Ruthenium

Interconnects for next generation of advanced CMOS



Stack used during this work



TEM Images before and after UV-LA

Challenges:

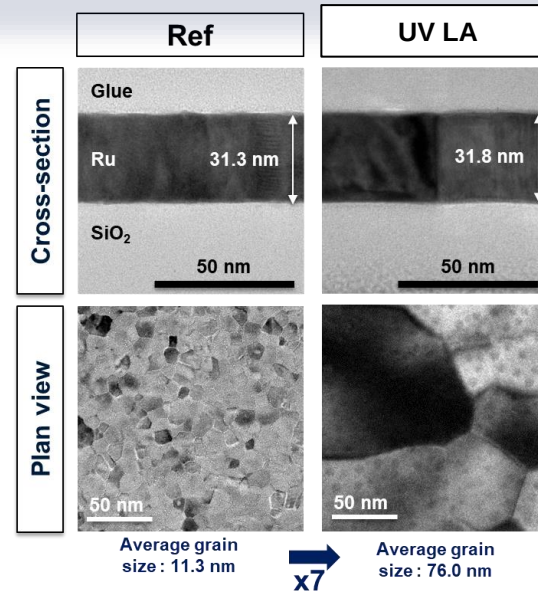
- Sufficient Grain size enlargement
- No degradation of BEOL structures
- Thermal budget compatible with FEOL constraints

Interconnects – Ruthenium

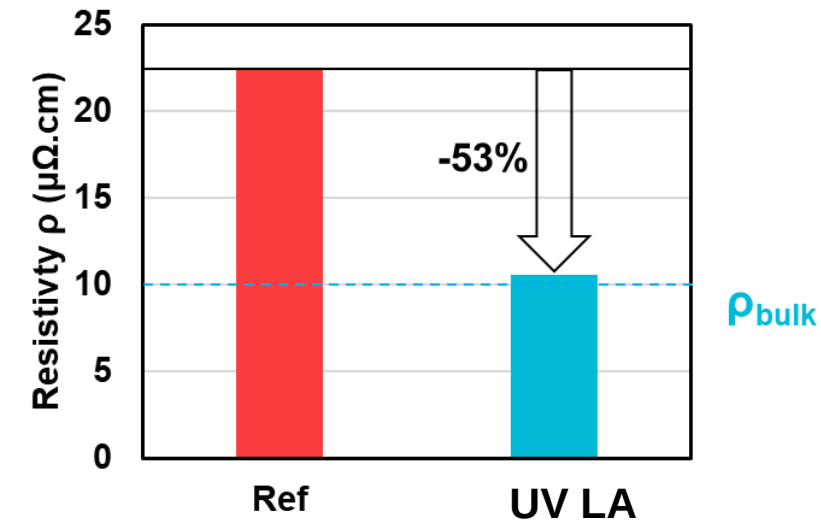
Interconnects for next generation of advanced CMOS



Stack used during this work



TEM Images before and after UV-LA



Film resistivity measured by 4PP before and after UV-LA

Challenges:

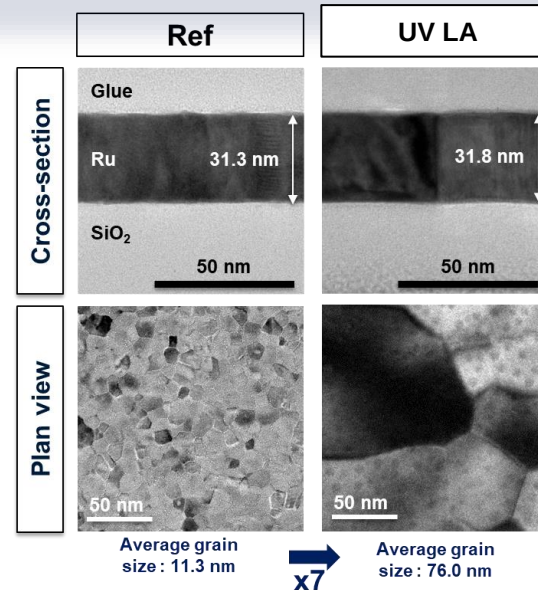
- Sufficient Grain size enlargement
- No degradation of BEOL structures
- Thermal budget compatible with FEOL constraints

Interconnects – Ruthenium

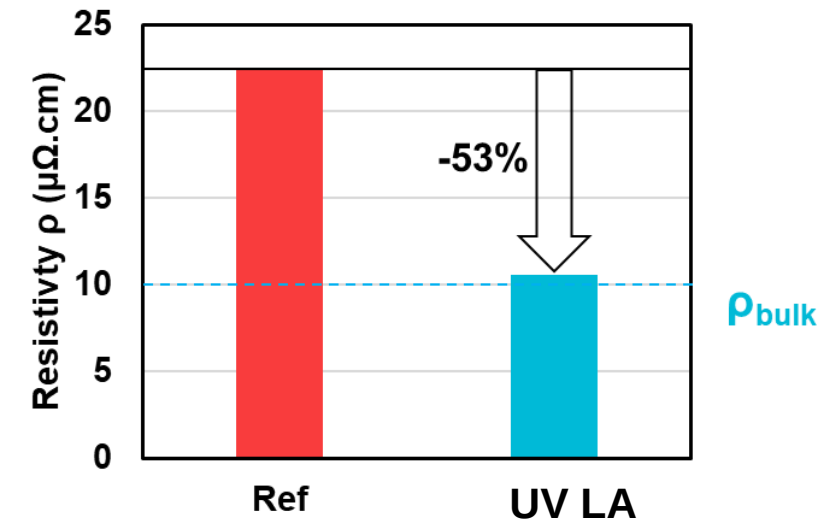
Interconnects for next generation of advanced CMOS



Stack used during this work



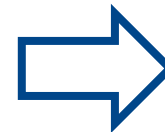
TEM Images before and after UV-LA



Film resistivity measured by 4PP before and after UV-LA

Challenges:

- Sufficient Grain size enlargement
- No degradation of BEOL structures
- Thermal budget compatible with FEOL constraints



Results:

Grain larger than e-MFP and film thickness
Slight degradation, laser conditions to be optimized
Need to be checked on real devices

Reference: "Study of the electrical and structural properties of Ru thin films annealed by Microsecond UV Laser Annealing for future BEOL interconnections", R. Daubiac, **EMRS2023**

Conclusion

Conclusion

Conclusion

- **New annealing solutions will be required to face next generation of semiconductor devices:**
 - *Solid phase process*
 - *Surface-Selective*
 - *Flexible*

Conclusion

- **New annealing solutions will be required to face next generation of semiconductor devices:**
 - *Solid phase process*
 - *Surface-Selective*
 - *Flexible*
- **UV new laser annealer emerges as a promising solution to face these challenges:**
 - *Long enough to allow solid-phase process*
 - *Surface-Selective thanks to μ s-timescale and shallow UV-light absorption*
 - *Ultimate thermal budget control thanks to common optimization of ED and irradiation time*

ADVANCING
TECH & INNOVATION

SCREEN Semiconductor Solutions Co., Ltd.

Innovation for a Sustainable World

SCREEN