



SOI & ADVANCED SUBSTRATES NEWS

ACCELERATING INDUSTRY GROWTH | Bi-Weekly Newsletter

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DEVELOPMENT OF SILICON-ON-INSULATOR DIRECT ELECTRON DETECTOR WITH ANALOG MEMORIES IN PIXELS FOR SUB-MICROSECOND IMAGING

In this study, researchers have developed a high-speed recordable direct electron detector based on silicon-on-insulator (SOI) technology. The detector has sixteen analog memories in each pixel to record sixteen images with sub-microsecond temporal resolution.

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SHALLOW TRENCH ISOLATION PATTERNING TO IMPROVE PHOTON DETECTION PROBABILITY OF SINGLE-PHOTON AVALANCHE DIODES INTEGRATED IN FD-SOI CMOS TECHNOLOGY

The Single-Photon Avalanche Diode (SPAD) Fully Depleted Silicon-On-Insulator (FD-SOI) concept is particularly useful for backside illumination in the near-infrared range after the device has been thinned. Nevertheless, in this study, researchers demonstrate that the SPAD FD-SOI is promising for frontside illumination (visible or near-infrared light).

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VERTICAL INTEGRATION OF KTN ON SOI WAFER

A fabrication methodology for wafer-scale vertical integration of potassium tantalate niobate (KTN) material onto silicon-on-insulator (SOI) wafers is described in this study, which provided a first insight into the feasibility of wafer-scale integration of KTN waveguides onto a silicon photonics platform and lays the initial groundwork for realising high-speed and efficient optical modulators.

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DESIGN AND RELIABILITY ASSESSMENT OF AN ULTRA-THIN BODY ELECTROSTATICALLY DOPED BIPOLAR TRANSISTOR FOR MIXED SIGNAL APPLICATIONS

A solution to scale down physical base length of symmetric lateral doping-free BJT by shrinking the silicon layer is proposed. The proposed device evinces six times higher gain and two times cut-off frequency compared to previously reported doping-free BJTs. This enhancement was possible because of complete use of silicon-on-insulator (SOI) thickness.

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SOI ECOSYSTEM NEWS

X-FAB AND SOITEC TEAM UP TO OFFER SMARTSIC™ AT LUBBOCK PLANT

This collaboration follows the successful completion of the assessment phase, during which silicon carbide (SiC) power devices were manufactured at X-FAB Texas on 150mm SmartSiC™ wafers. Soitec will offer X-FAB's customers easy access to the SmartSiC™ substrate through a joint supply chain consignment model.

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CRUCIAL ROLE FOR IMEC IN EU CHIPS ACT

Imec will host the beyond 2nm SoC R&D pilot line and participate in the pilot lines on low power FD-SOI and on heterogeneous system integration. In line with the Chips Act vision, imec and its partners will collaborate with European and global equipment and material suppliers to set up a one-of-a-kind beyond 2nm SoC R&D pilot line.

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HIGH-EFFICIENCY SELF-FOCUSING METAMATERIAL GRATING COUPLER IN SILICON NITRIDE WITH AMORPHOUS SILICON OVERLAY

While state-of-the-art grating couplers have been developed for SOI waveguides, the moderate index contrast of silicon nitride (SiN) presents an outstanding challenge for implementing efficient surface grating couplers on this platform. This work presents a novel grating coupler architecture for silicon nitride photonic integrated circuits that utilizes an amorphous silicon overlay.

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BROADBAND, HIGH-REFLECTIVITY DIELECTRIC MIRRORS AT WAFER SCALE: COMBINING PHOTONIC CRYSTAL AND METASURFACE ARCHITECTURES FOR ADVANCED LIGHTSAILS

By pioneering a bilayer membrane structure using a silicon nitride photonic crystal atop a flat silicon layer, researchers approach the material and design challenges associated with laser-driven lightsails, drawing inspiration from the high reflectivity exhibited by conventional photonic crystal devices and the enhanced functionality and tunability offered by metasurface devices.

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COMPOUND SEMICONDUCTOR

STMICROELECTRONICS TO BUILD THE WORLD'S FIRST FULLY INTEGRATED SILICON CARBIDE FACILITY IN ITALY

It is noted that this will achieve a first of a kind in Europe for the mass production of 200mm silicon carbide (SiC) wafers with each step of the process – substrate, epitaxy & front-end, and back-end – using 200 mm technologies for enhanced yields and performances.

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INFINEON ANNOUNCES NEXT GEN COOLGaN

Infineon has announced two new generations of high voltage and medium voltage CoolGaN devices which now enable customers to use GaN in voltage classes from 40 V to 700 V in a broader array of applications. The two product families are manufactured on 8-inch in-house foundry processes in Kulim (Malaysia) and Villach (Austria).

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HIGH TEMPERATURE STABILITY OF REGROWN AND ALLOYED OHMIC CONTACTS TO ALGAN/GAN HETEROSTRUCTURE UP TO 500 °C

For high-temperature applications like Venus exploration, researchers have recently turned their interests to gallium nitride. In a recent study published in Applied Physics Letters, scientists from MIT and elsewhere found that extreme temperatures didn't cause significant degradation to the gallium nitride material or contacts.

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ENTANGLED PHOTON PAIR GENERATION IN AN INTEGRATED SiC PLATFORM

Recent breakthroughs in generating entangled photons on SiC microchips mark a significant step toward unlocking its capabilities for practical quantum applications. In this study, researchers demonstrate for the first time an entangled photon source in an integrated silicon carbide platform.

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SEMI BLOG

GLOBAL SEMICONDUCTOR INDUSTRY OUTLOOK – TAKING UNPRECEDENTED ACTION TO OPTIMIZE GROWTH, ADDRESS CHALLENGES

The global semiconductor industry is expanding production capacity to support the proliferation of AI and a diverse range of disruptive technologies and emerging applications. However, Talent Gap, Sustainability Pressure, Supply Chain Disruptions and the Geopolitical and Regulatory Landscape continue to remain top of mind for industry CEOs. Ajit Manocha, President and CEO of SEMI, gave an update on the industry's outlook through the first quarter and SEMI member-led programs to pave the way to \$1 trillion and beyond.

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SEMI NEWS HIGHLIGHT

SEMI AND ENERGY COLLABORATIVE SPONSORS MEET WITH SOUTH KOREA MOTIE OFFICIALS TO PRESENT RECOMMENDATIONS ON EXPANDING RENEWABLE ENERGY

As part of its Energy Collaborative (EC) Initiative, SEMI and EC Sponsors met with South Korea's Ministry of Trade, Industry and Energy to discuss the EC analysis, recommendations and solutions to expanding access of the region's semiconductor ecosystem to renewable energy – a critical factor for the chip supply chain to meet its net zero goals.

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