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From Advanced SiC to UWBG Devices: A Research Perspective

SEMICON Europa Executive Forum
Electrification and Power Semiconductors
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Overview

Advanced SiC concepts

- FinFET structures in Power MOSFETs
- Super-Junction Drift Regions

UWBG Approaches

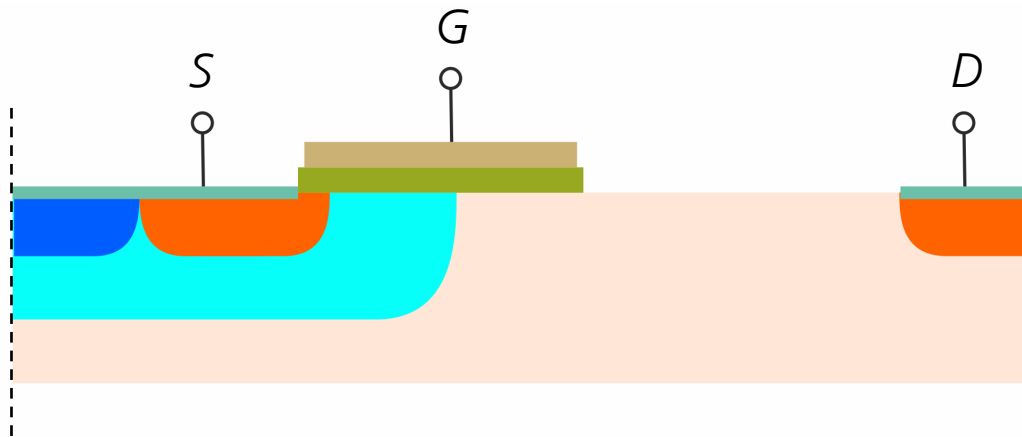
- Laboratory Pilot Line for AlN Devices

Conclusion

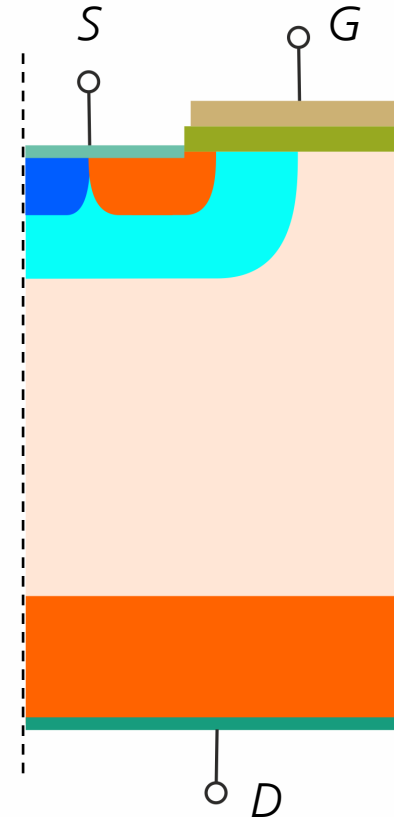
Motivation for Advanced SiC Concepts

Power MOSFET Evolution: Planar to Vertical

Lateral DMOS – LDMOS



Vertical DMOS – VDMOS

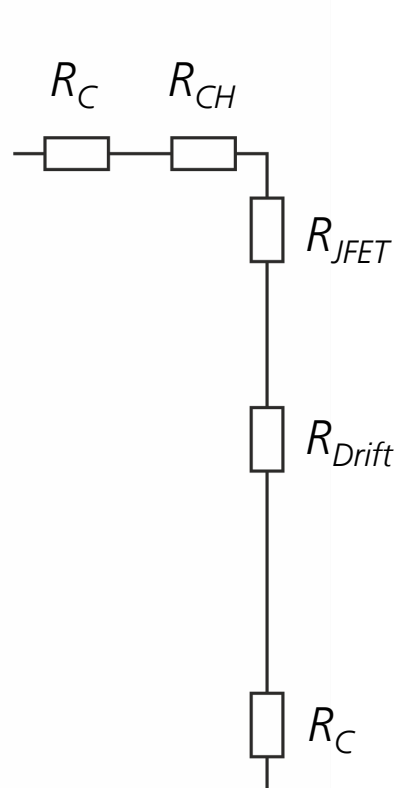
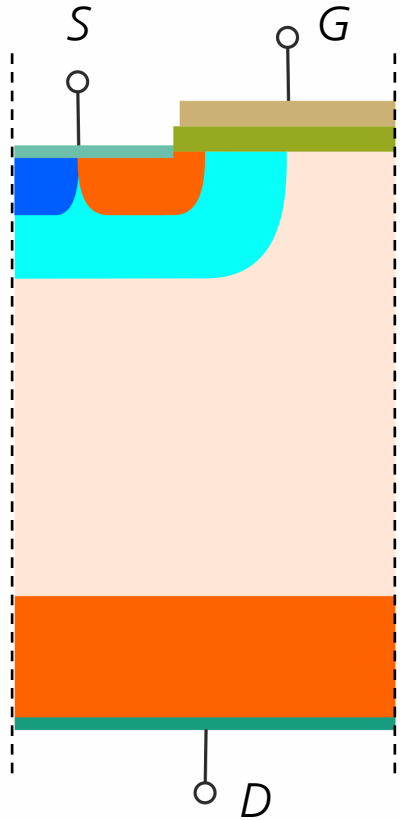


- Vertical drift layer saves area
- Large drain contact simplifies wiring pattern
- Maximum field in blocking mode is shifted from channel edge > JFET region

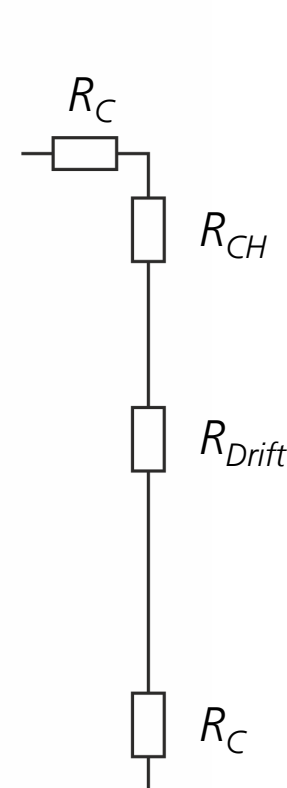
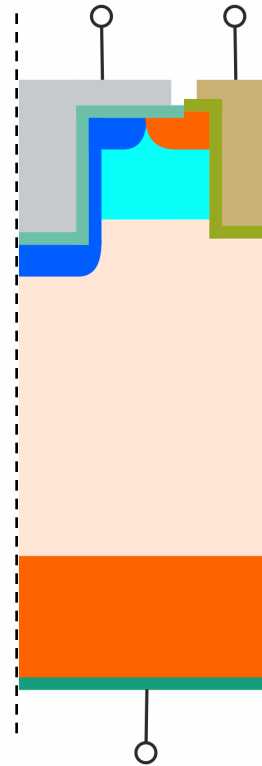
Motivation for Advanced SiC Concepts

Resistance contributions in improved architectures

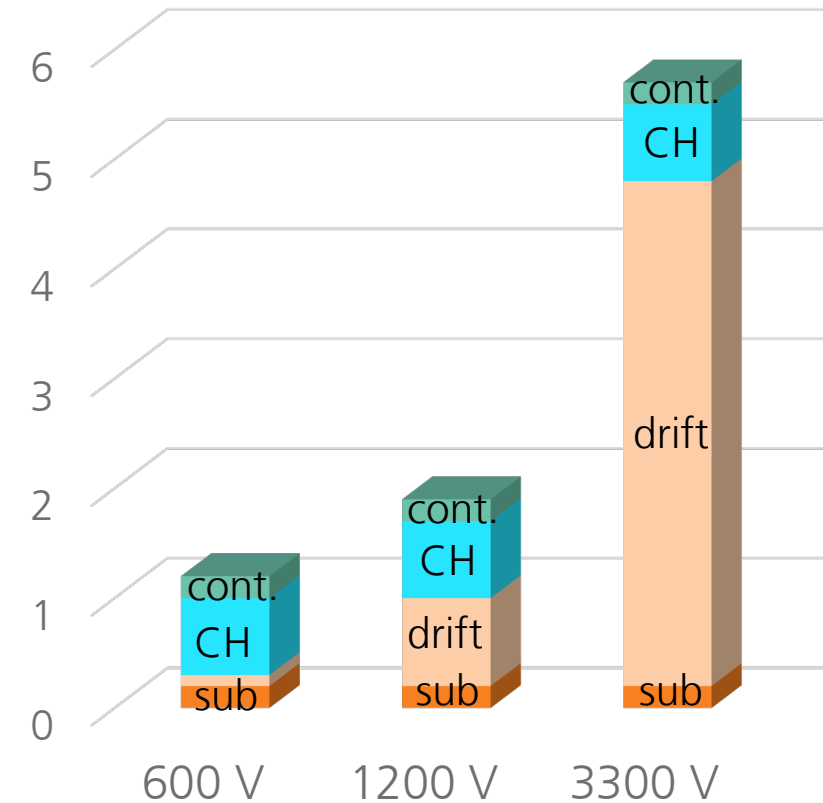
Vertical DMOS – VDMOS



Trench MOSFET – UMOS



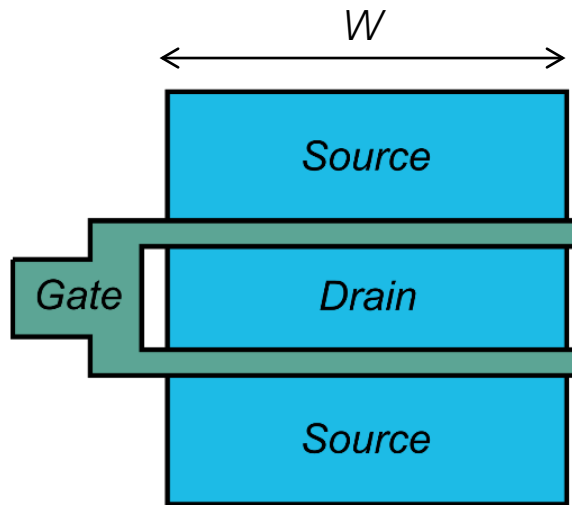
Specific on-resistance in $\text{m}\Omega\text{cm}^2$



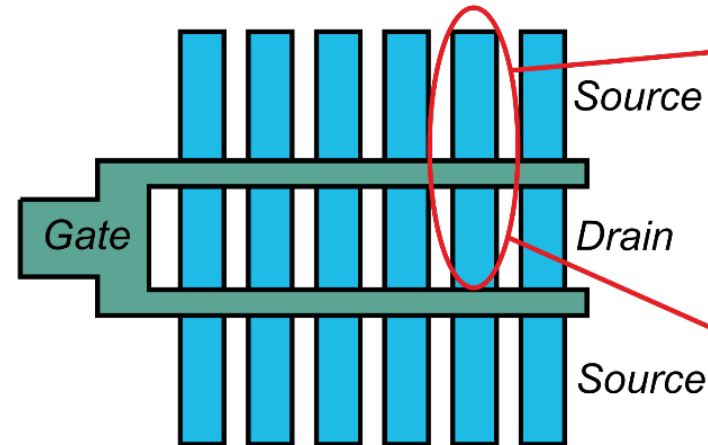
Improvement of Channel Resistance

Advanced Channel Architectures to Improve Channel Width

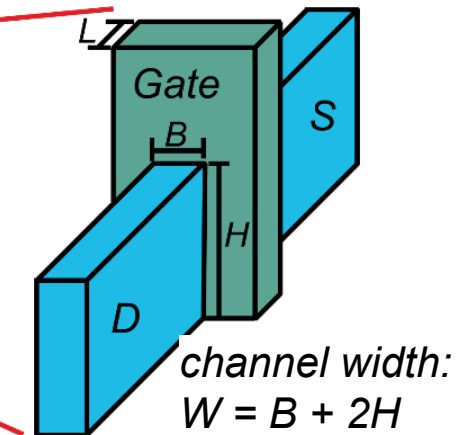
FinFET principle for enhancement of channel width



planar MOSFET



Multi Fin FET



FinFET: side view of single fin

- Gate width and respective drain current can be increased significantly

Improvement of Channel Resistance

Integration of FinFET Approach with Power MOSFETs

FinFET principle for enhancement of channel width

- Picture removed for copyright reasons
- Please refer to Pamamurthy et. al., EDL, 42(1)2021, p. 90, Fig. 1

- Reduction of channel resistance to 28%
- Reduction of on-resistance by ~50% in a 760 V SiC MOSFET

- Picture removed for copyright reasons
- Please refer to Shimizu et. al., ISPSD 2023, Tomoka et al., ISPSD 2024, Fig. 2

- Reduction of on-resistance by 15% even in 3.3 kV VDMOS
- Further reduction by 20% in 3.3 kV TrenchMOS architecture

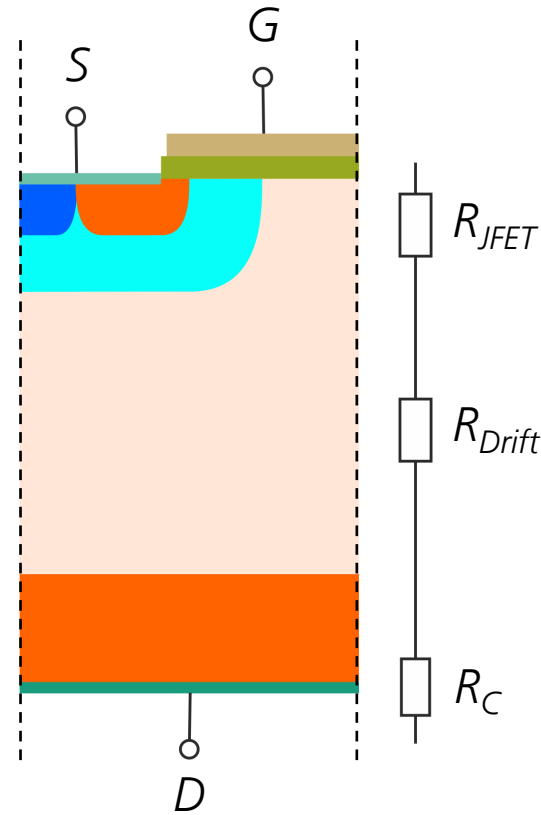
Superjunction Principle

Fighting the trade-off between Blocking Voltage and Drift Resistance

Blocking voltage depends on the net charge in the drift zone

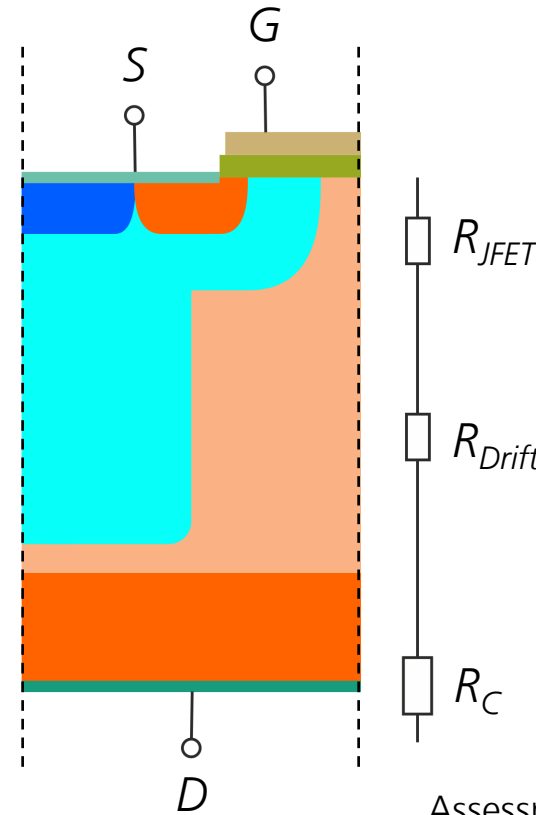
$$R_{Drift} \sim BV^{2.4}$$

- High conduction loss at elevated temperatures
- Limited to low current densities... $< 50 \text{ A/cm}^2$
- Marginally better than incumbent Si IGBTs in high-frequency switching applications



$$R_{drift} \sim BV^{1-1.3}$$

- SJ p-pilars allow for higher doped drift layer
- limited to low current densities... $< 50 \text{ A/cm}^2$
- Marginally better than incumbent Si IGBTs in high-frequency switching applications

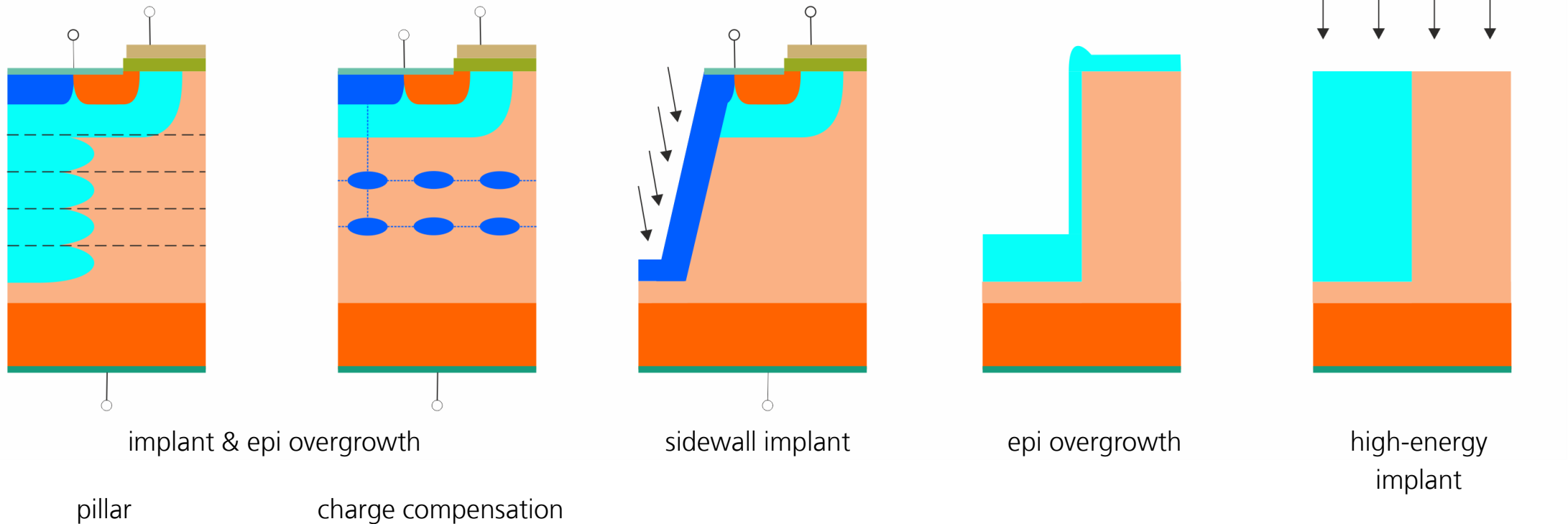


Assessment following R. Ghandi, ICSCRM 2024

Superjunction Fabrication

Fighting the trade-off between Blocking Voltage and Drift Resistance

Approaches for realisation of SJ drift layers



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Ultra Wide Band Gap Semiconductors

Basic parameters of (U)WBG materials

Material	$E_C @ N_D=10^{16} \text{ cm}^{-3}$ (MV cm ⁻¹)	Electron drift mobility (cm ² V ⁻¹ s ⁻¹)	p-doping	Thermal conductivity (W m ⁻¹ K ⁻¹)	BFOM = $\frac{1}{4} \epsilon \mu E_C^2$ (10 ⁶ V ² Ω ⁻¹ cm ⁻²)
Si	0.3	1240	yes	145	8.8
4H-SiC	3.1	980	yes	370	6270
GaN	4.9	1000	yes	253	27 900
AlN	15.4	426	poor	319	336 000
β-Ga ₂ O ₃	10.3	150	no	27	36 300
c-BN	17.5	825	deep acc.	940/2145	695 000
Diamond	13.0	2000	moderate	2290/3450	554 000

heterostructures
favorably

needs efforts for
structural cooling

Data source: J. Y. Tsao, Adv. Electron. Mater. 2018 (4) 1600501

AlN Devices on Native Substrates

Beneficial Materials Properties transfer into Device Quality

- Picture removed for copyright reasons
- Please refer to Y. Zhang, IEDM 2015

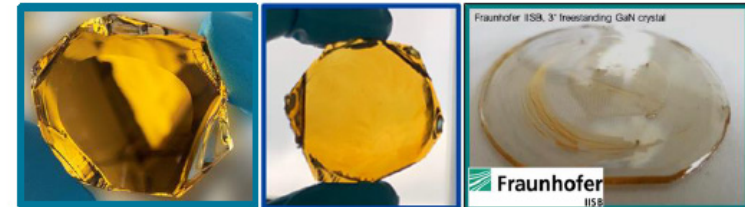
The electrical performance of a device can be strongly compromised by the substrate

Off-state leakage currents depend on substrates

Homoepitaxy preferred

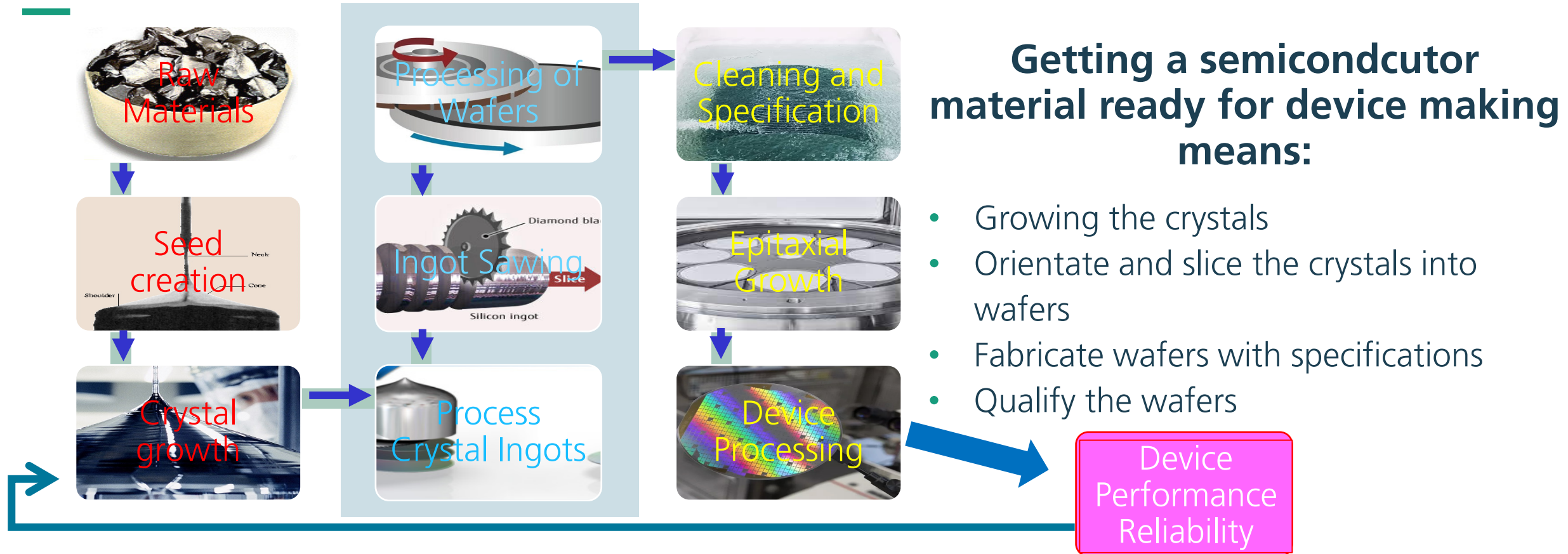


Crystals required



Launching a semiconductor material for electronic device fabrication

From theory to practical wafer and device making

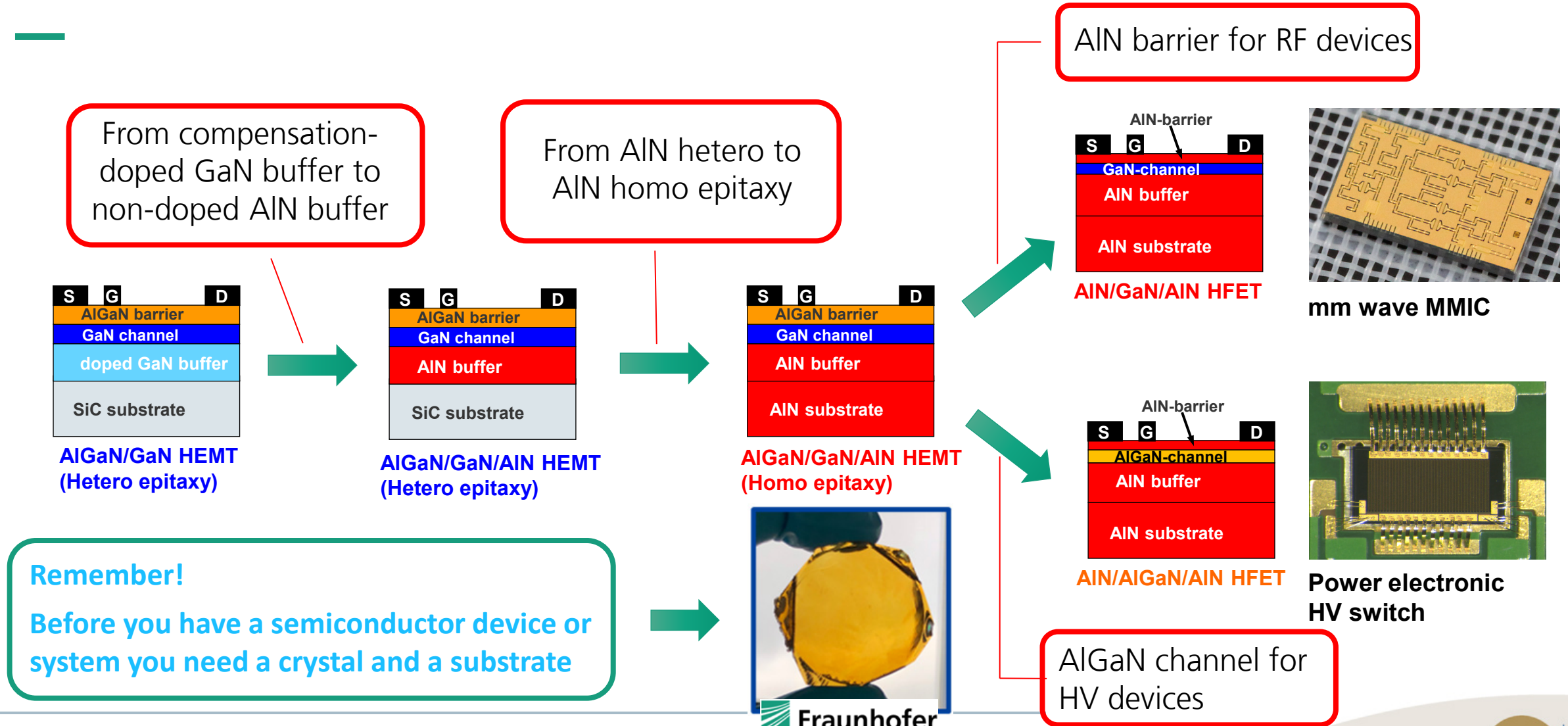


Relate device performance to crystal growth and substrate wafers

Wafers must be suitable for processing with repeatable specification

Towards Aluminum Nitride Based Electronic Devices on native substrates

Collaboration between Fraunhofer IISB and FBH



Lab-pilotline for AlN power electronic devices in Germany

From crystal to device – joint forces



For the successful production of devices, wafers must have the following parameters defined:

- Defined geometry
- Major and minor flat
- *No bow now warp*
- Trimmed edges
- Low surface roughness
- 90% usable area
- Clean surface
- Low dislocation density
- *No lattice bow*
- *Controlled off-cut*

High technological effort for R&D
→ Strategic partnerships needed

Conclusion

Advanced SiC Concepts

- next steps in resistance optimization involve
 - multichannel options, especially for low-voltage designs and
 - super-junction drift regions for high-voltage applications
- also used as general approaches for reduction of $R_{on} \times A$ in medium voltage classes

Novel Ultra-Wide Band Gap Materials

- AlN and Ga₂O₃ under investigation for their availability and processability
- Hetero-structure approaches for 2D carrier assemblies and replacement of p-doping
- IISB established a AlN lab pilot line for AlN HEMTs employing AlGa_N / GaN / AlN heterostructures on native substrates together with partner Ferdinand Braun Institute, Berlin

Check out IISB capabilities at https://www.iisb.fraunhofer.de/en/research_areas/semiconductor_devices.html

Fraunhofer IISB

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