

Atomic Layer Etching of SiO_2 with SF_6

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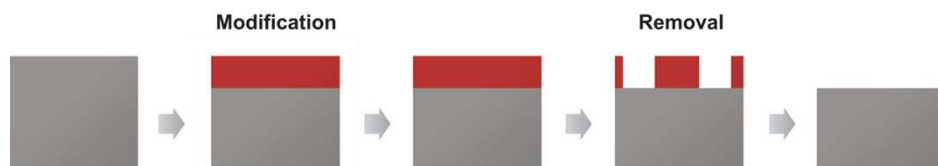
Contact: rzierold@physnet.uni-hamburg.de



ALE & Semiconductor Industry

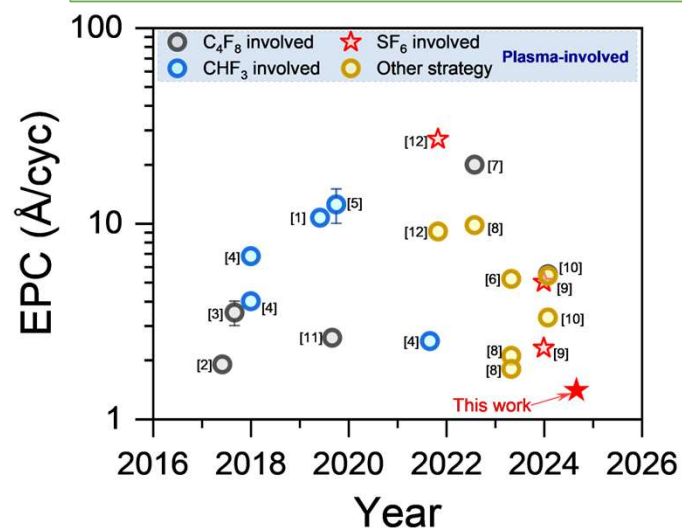


Generic ALE cycle

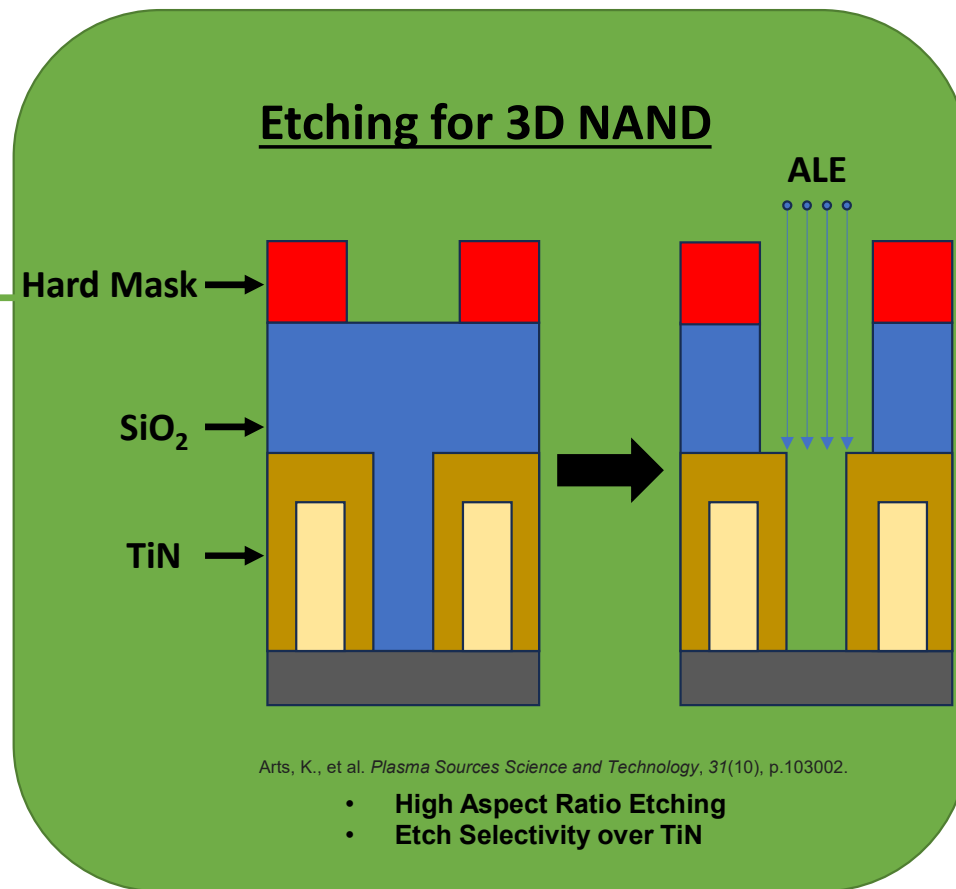


K. J. Kanarik et al., *Journal of Vacuum Science & Technology A* **33**, 020802 (2015).

Comparison of our work with others

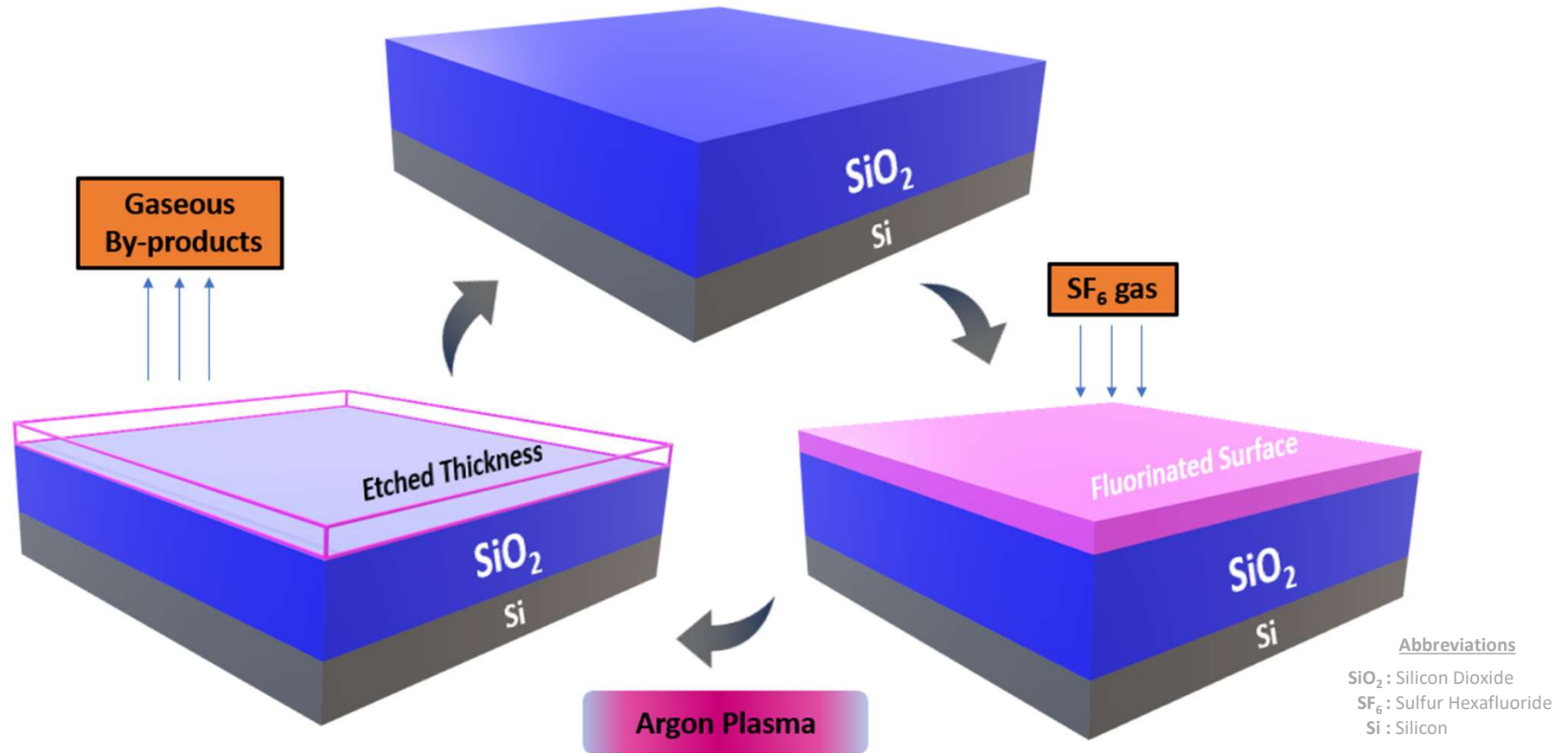


Peng, J.; Venugopal, R.; Blick, R.; Zierold, R. Atomic layer etching of SiO₂ via Ar and SF₆ plasma. (Under Review)

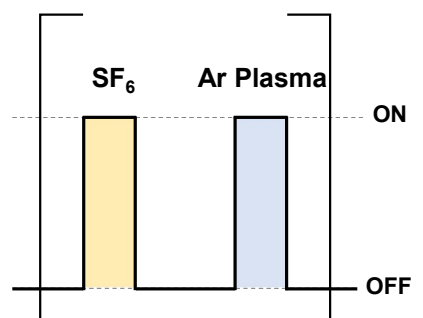


Arts, K., et al. *Plasma Sources Science and Technology*, 31(10), p.103002.

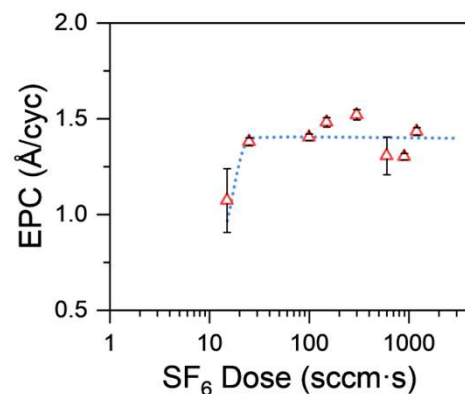
Atomic Layer Etching Process



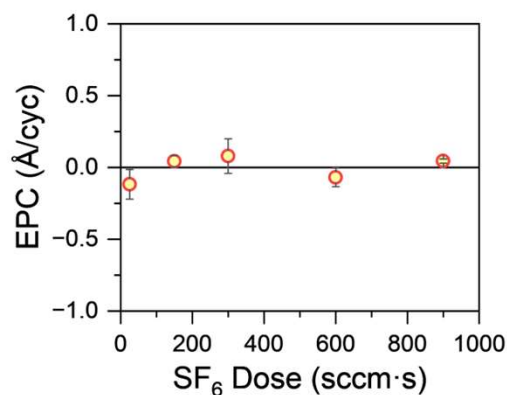
Control Experiments and Consistency of EPC



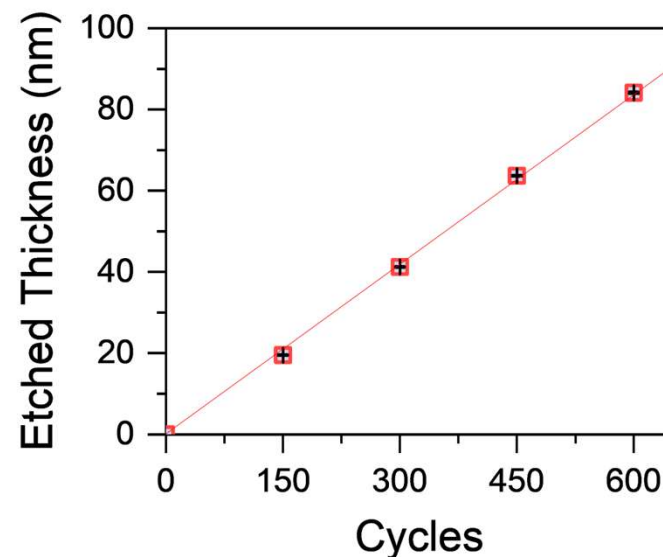
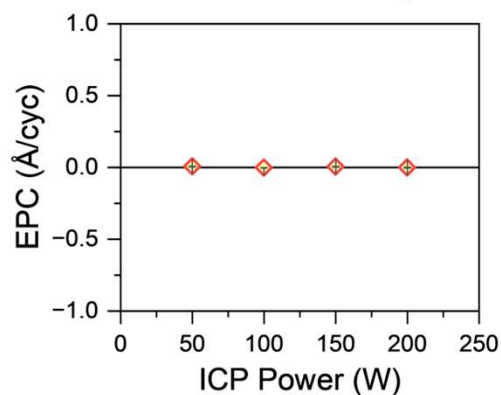
Schematic of the Cyclic ALE Process



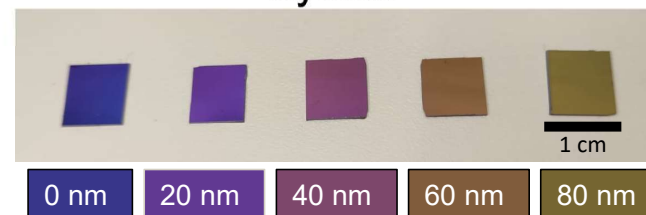
Control 1: No ICP Plasma



Control 2: No SF₆

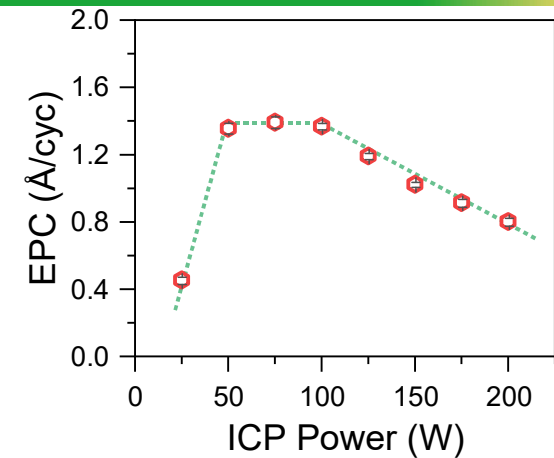
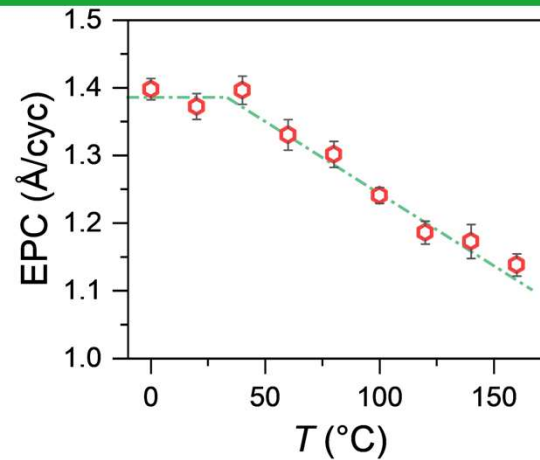
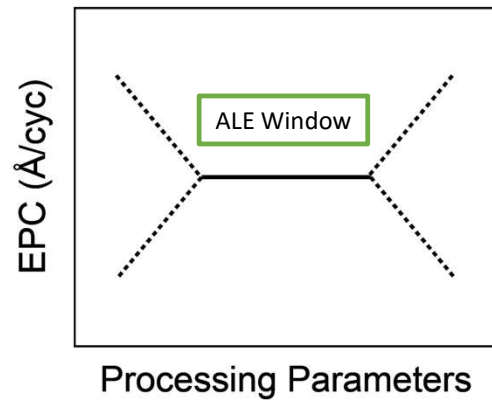


Etched Thickness



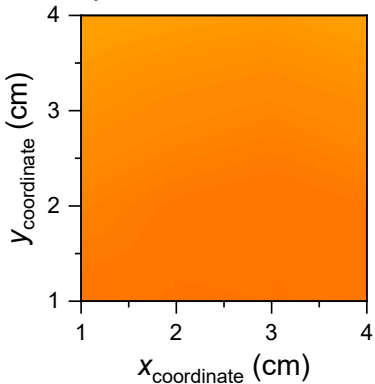
$$\text{Etch Per cycle (EPC)} : \frac{\text{Thickness Etched}}{\text{Cycles}} = 1.4 \pm 0.1 \text{ Å/cycle}$$

ALE Window & Uniformity Test

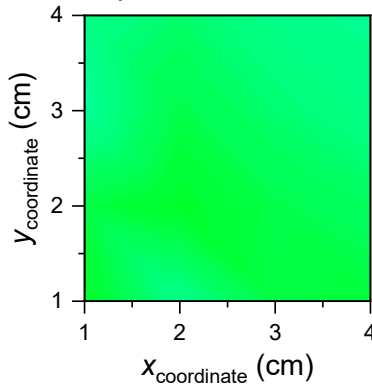


Uniformity Test

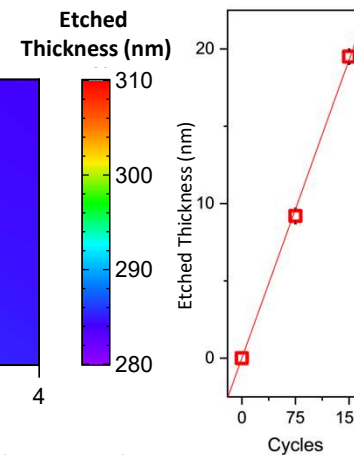
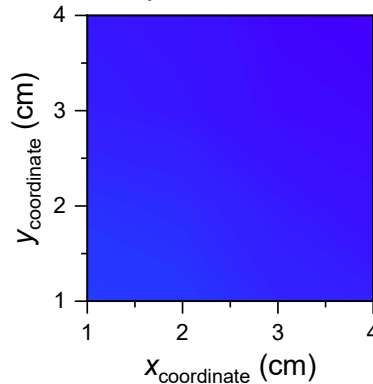
a) 0 cycles



b) 75 cycles

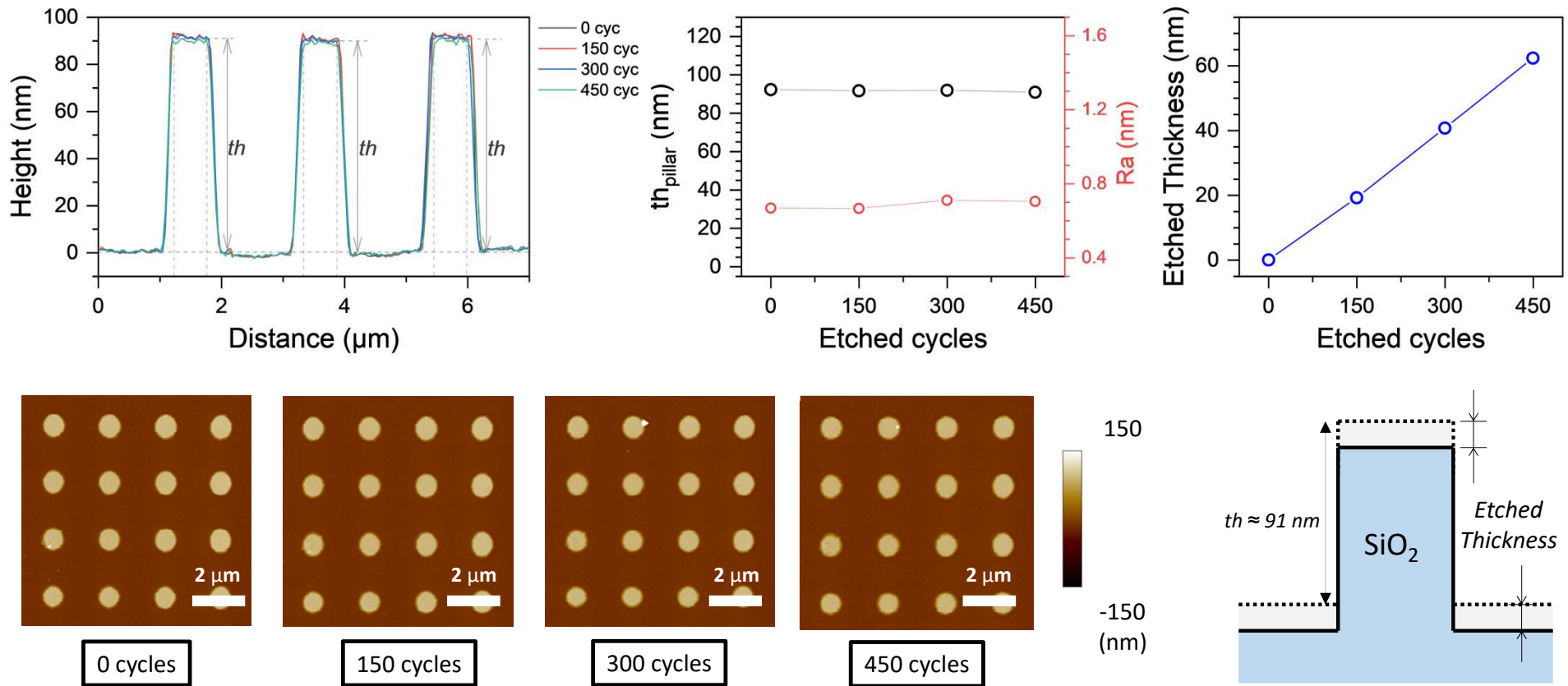


c) 150 cycles



- ❖ Low Temperature
- ❖ Scalable Uniform Etching

Anisotropic Etching (Directional ALE)



Thank you!

Take-home message:

- Reliable and scalable ALE for SiO₂ using sequential SF₆ and Ar plasma
- Etch Rate of $\sim 1.4 \pm 0.1$ Å/cycle
- Uniform etching over large scale substrates
- Low temperature
- High Aspect Ratio Directional etching

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References



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