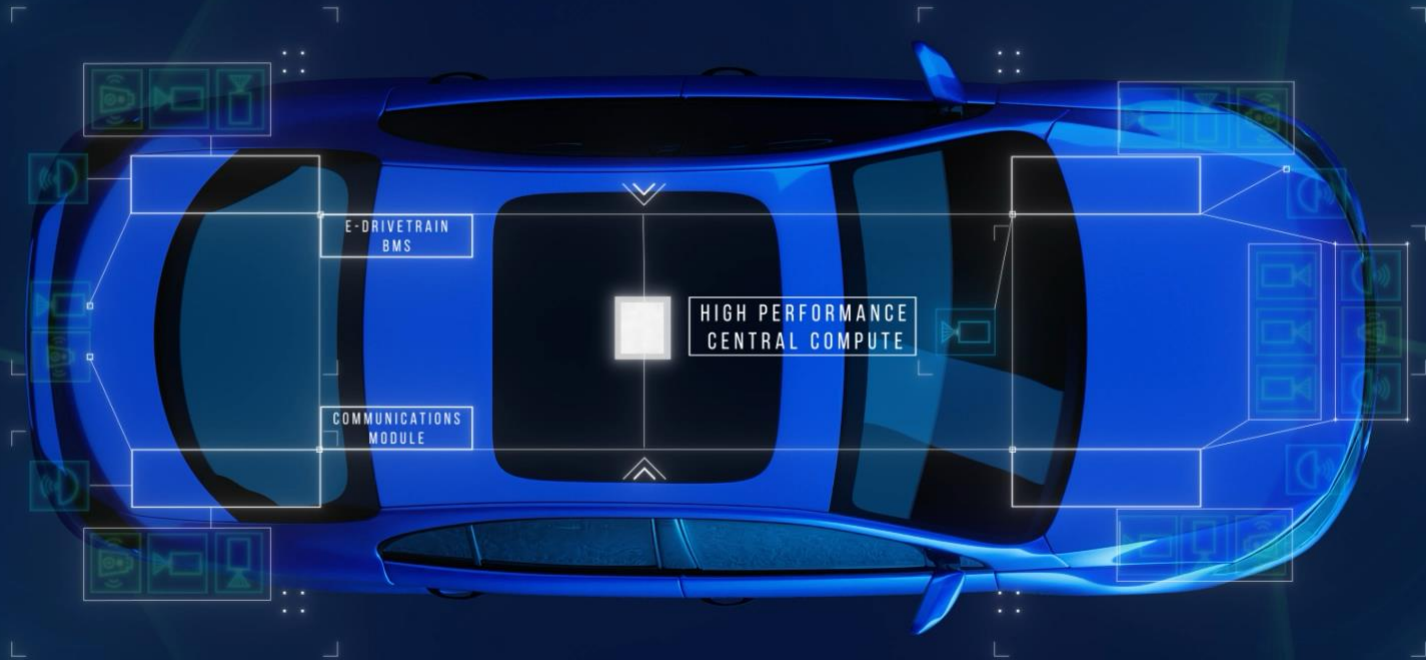


Challenges in the land of Automotive High-Performance Computing: Chiplets to the Rescue

Bart Plackle – Vice President Automotive, imec

Automotive focus: processing more



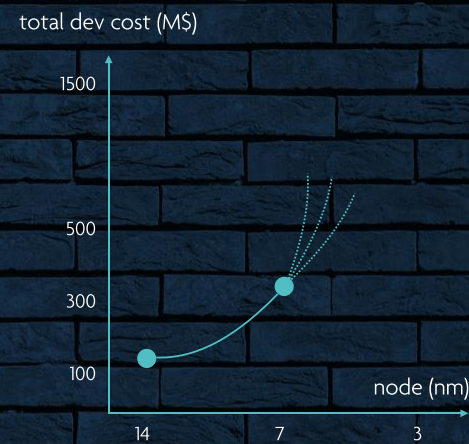
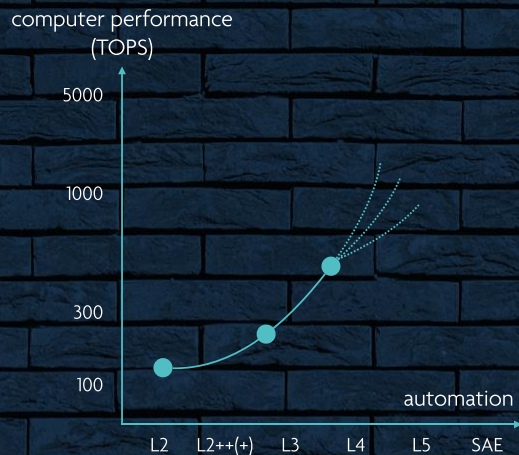
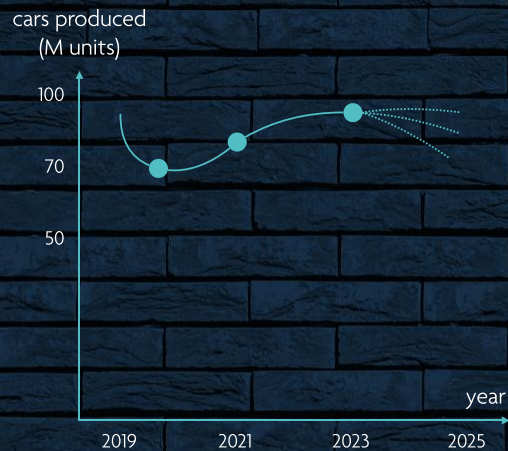
High Performance Central Compute

IMEC R&D's Valuable Contributions

	High-k	FinFET	EUV	Nano-sheet	Backside Power	CFET	High NA
							
IMEC R&D	2001	2004	2006	2014	2017	2020	2024
Industry	2007	2012	2018	2024	2026		

ITF WORLD

40



Exponential growth of performance requirements

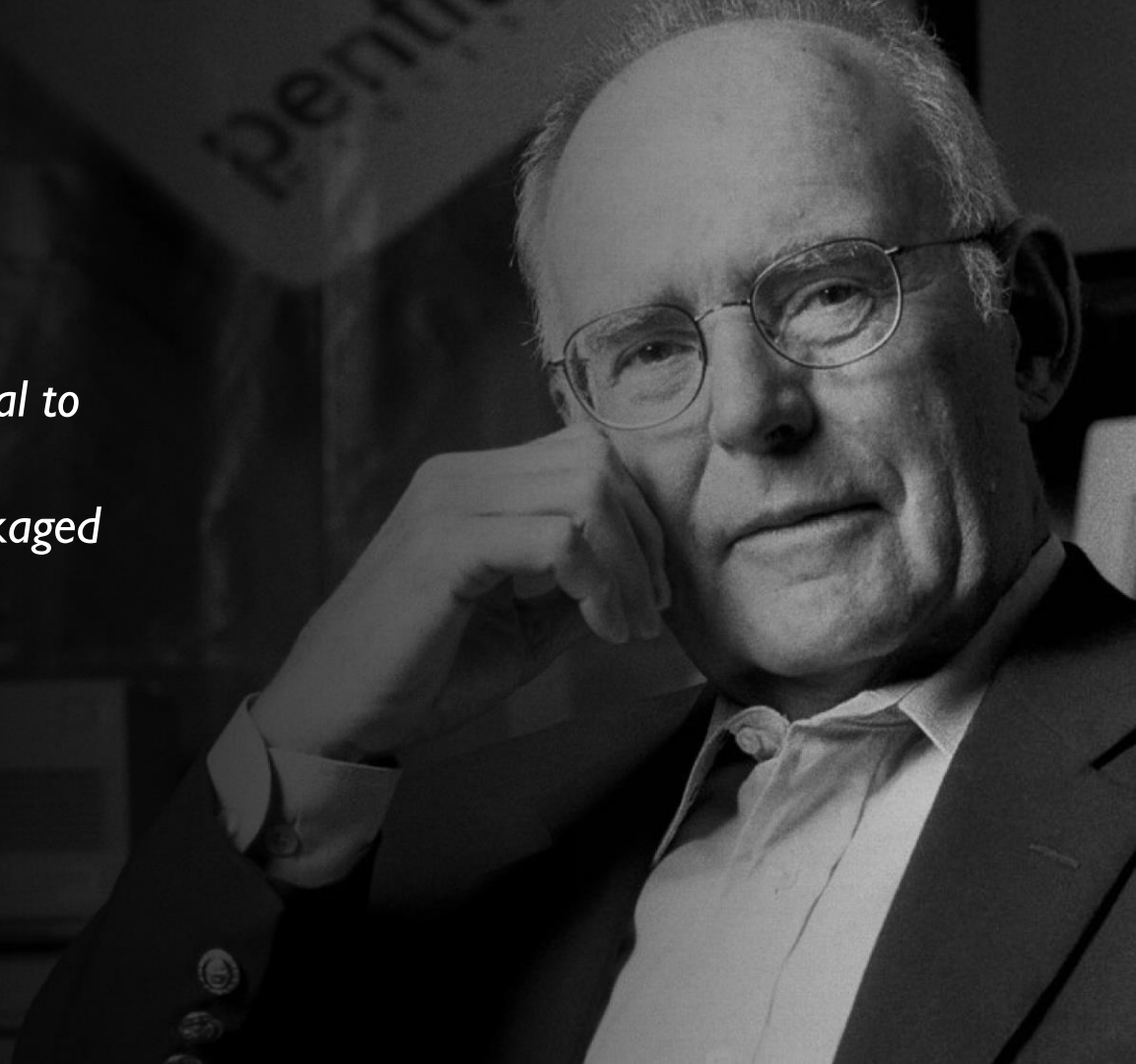
Designs close or exceeding reticle

Transistor scaling slowing down

Price / transistor increasing

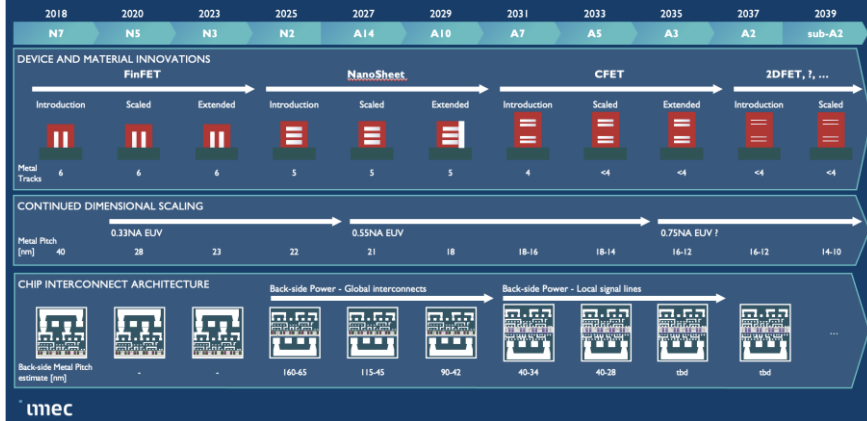
Moore's law alive?

“It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected.”

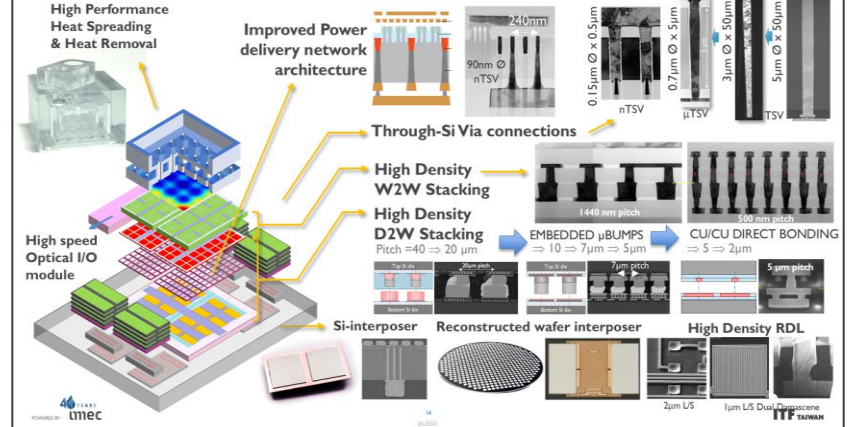


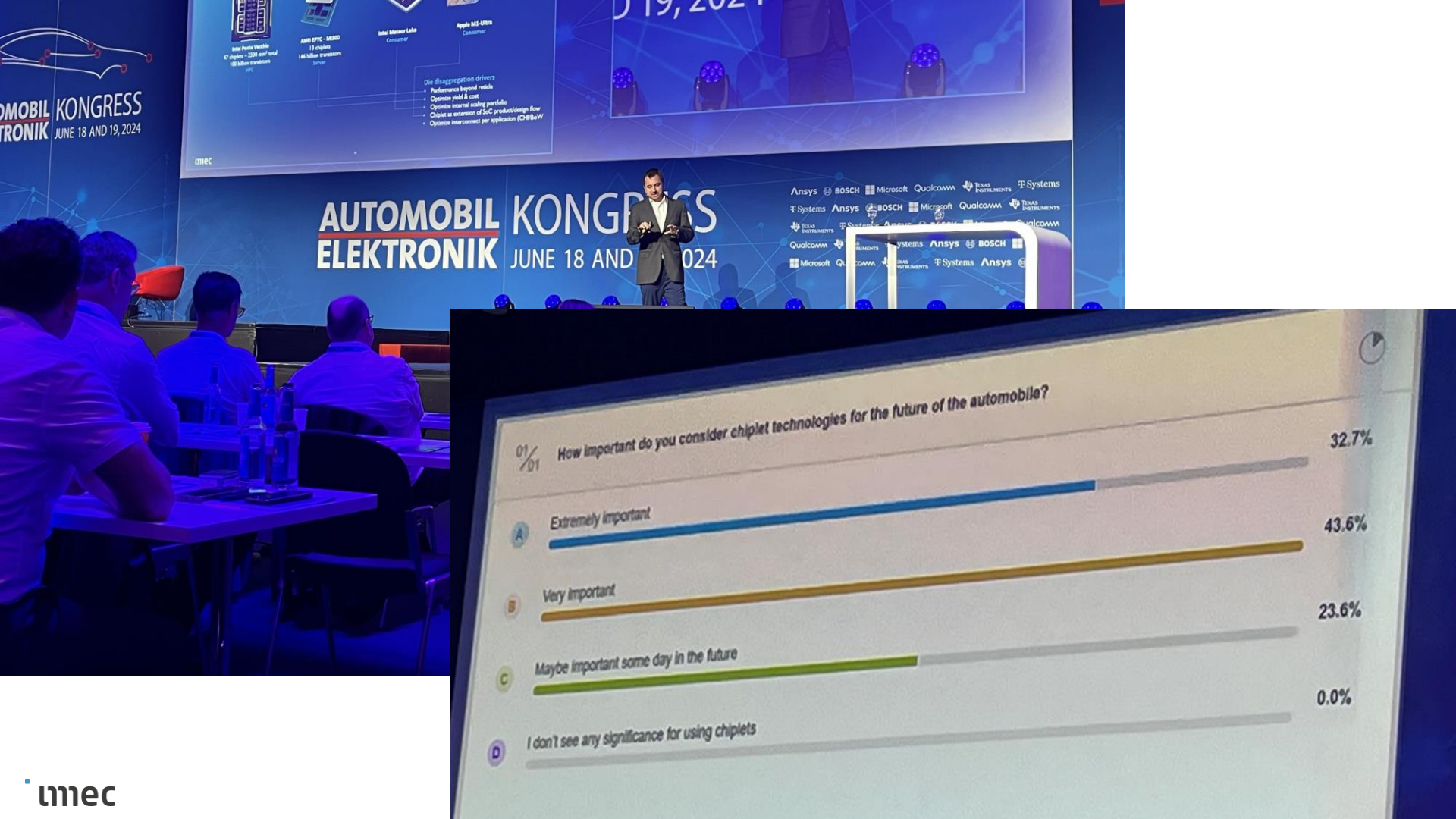
Future = process scaling + advanced packaging

Options extending the roadmap



Imec 'family picture' Chiplet System Integration





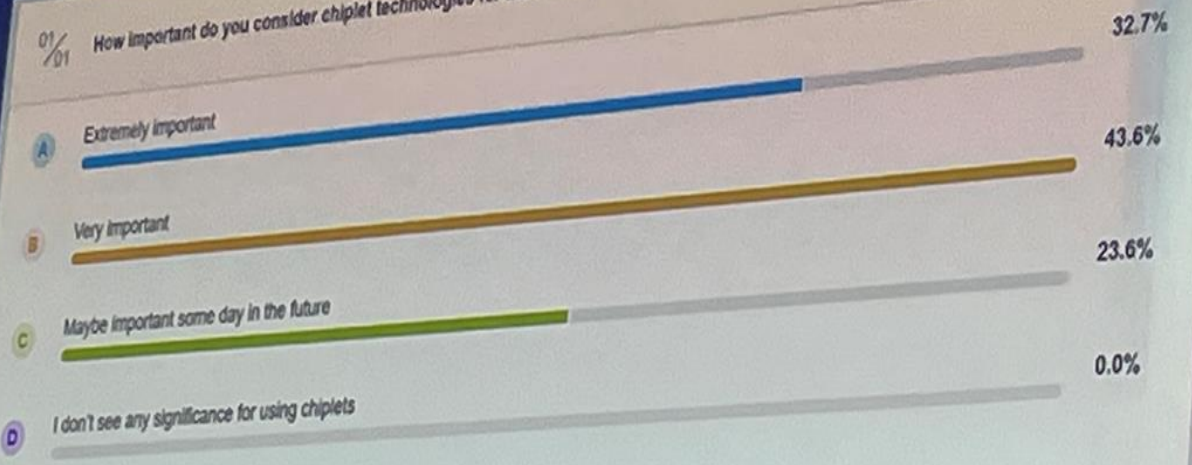
AUTOMOBIL KONGRESS

ELEKTRONIK

JUNE 18 AND 19, 2024

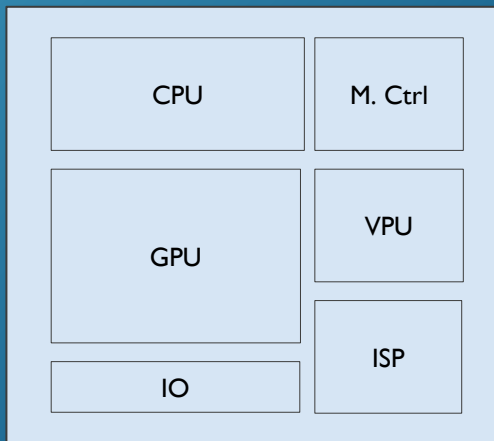
Ansys Bosch Microsoft Qualcomm Texas Instruments F Systems
F Systems Ansys Bosch Microsoft Qualcomm Texas Instruments
Texas Instruments Bosch F Systems Ansys Bosch
Qualcomm Texas Instruments F Systems Ansys Bosch
Microsoft Qualcomm Texas Instruments F Systems Ansys

01/01 How important do you consider chiplet technologies for the future of the automobile?



Chiplet in a nutshell

Monolithic die



Monolithic integration of all subsystems on the same die, same process.

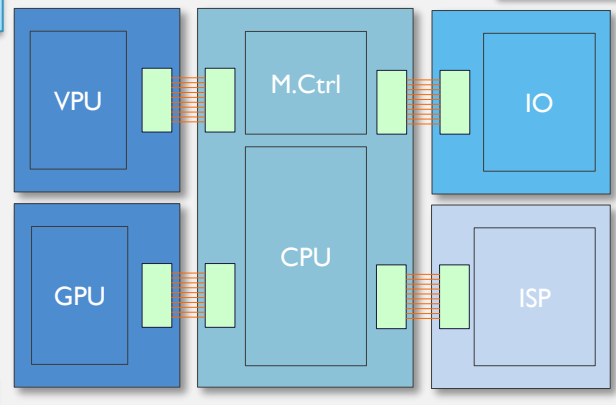
Performance and power optimization

- Integration of newest IP
- Best process for IP

Composable & reusable

- 3rd party chiplets
- SKUing

Chiplet Heterogeneous integration



Shorter TTM

- Chiplet re-use
- Independent validation
- Decoupled stepping's

Higher Yield

- Small die with better yield
- Known Good Die

Performance Scaling

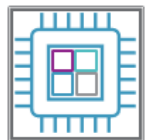
- **beyond full reticles** (max die size)
- Architecture scaling (low to Premium) by selective assembly

Path to Open chiplet market

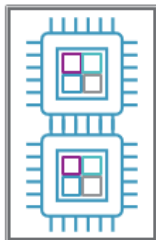
2024

2030

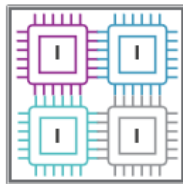
2035



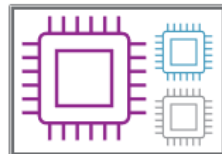
System-on-chip



Homogeneous chiplets



Heterogeneous chiplets
Closed ecosystem



Hybrid chiplets

CPU

GPU

MEM

AI

Interoperability

SW

System

Protocol

PHY

Power

Manufacturing / DFX

Heterogeneous chiplets
Open chiplet market

Vibrant ecosystem OEM/T1/T2 allowing
rapid hardware upgrades & differentiation
STANDARDIZATION A MUST

Automotive chiplets: A two-pronged approach

Automotive
Chiplet Forum

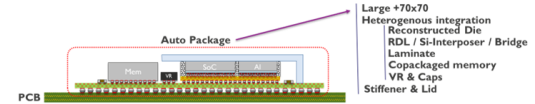
sitor launched
by imec

**Broad industry
Alignment**

Imec's **Automotive
Chiplet Program (ACP)**

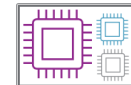
Quality and Reliability

what package technology can be made automotive compliant?



Architecture

what architecture supports multi party chiplets?



UCle
Universal Chiplet
Interconnect Express

e.g. OEM differentiation through 3th party NPU

**Pre-competitive research Program
To Accelerate & Derisk
Automotive chiplet**

Bringing the automotive chiplet ecosystem together



ITF World announcement
May '23
20 companies



2nd ACF
Leuven, October '23
50 companies



4th ACF
Ann Arbor, October '24
130+ registrants (US, EU, JP, TW)

Call to action
March '23
White paper



1st ACF
Leuven, June '23
30 companies



3rd ACF
Munich, March '24
60 companies – 120+ participants



Next ACF
April 1-2 2025
ARM Cambridge, UK





semiconductor
talent technologies
automotive research

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Automotive Chiplet Program

Accelerate & Derisk Automotive Chiplet Introduction

Quality and Reliability

Which package technology can be made automotive compliant?

Architecture

How should a scalable chiplet architecture look like

Scope

Focused on High performance central compute

Affordability

How to ensure chiplets fit automotive cost targets

Standardization

How to create path to interoperable chiplet ecosystem

Pre-competitive

Shared research platform across the eco-system

Announcing First Automotive Chiplet Program partners

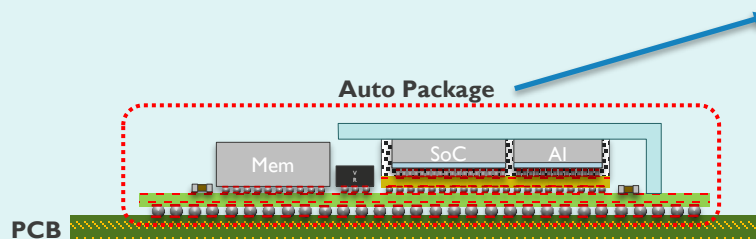


tenstorrent



Automotive Chiplet Program

Track A: QnR



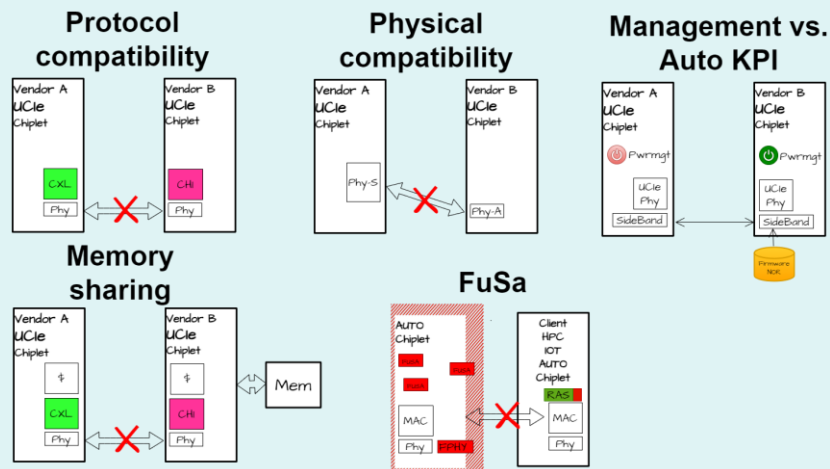
Complex & large package

Heterogenous integration
Reconstructed Die
RDL / Si-Interposer / Bridge
Laminate
Copackaged memory
VR & Caps
Stiffener & Lid

ACP Research

- WP0 – Requirements – **L size** / qualification
- WP1 – **2D/2.5D** Materials for auto
- WP2 – **Prototype build** – Large – **PTCQ+**
- WP3 – **Reliability** modeling – **Aging**
- WP4 – Manufacturing – Assembly – **Repair**
- WP5 – Automotive Qualification – **AECQ**
- WP6 – **Memory** co packaging
- WP7 – **Thermal** management

Track B: Arch



- WP11 – Die-Die interfaces – **UCIe AUTO**
- WP12 – **FuSa**
- WP13 – **Testability**
- WP14 – System manageability
- WP15 – **Predictive Failure**
- WP16 – **Digital Twin** modeling
- WP17 – Software

Chiplets , time to hit the road

