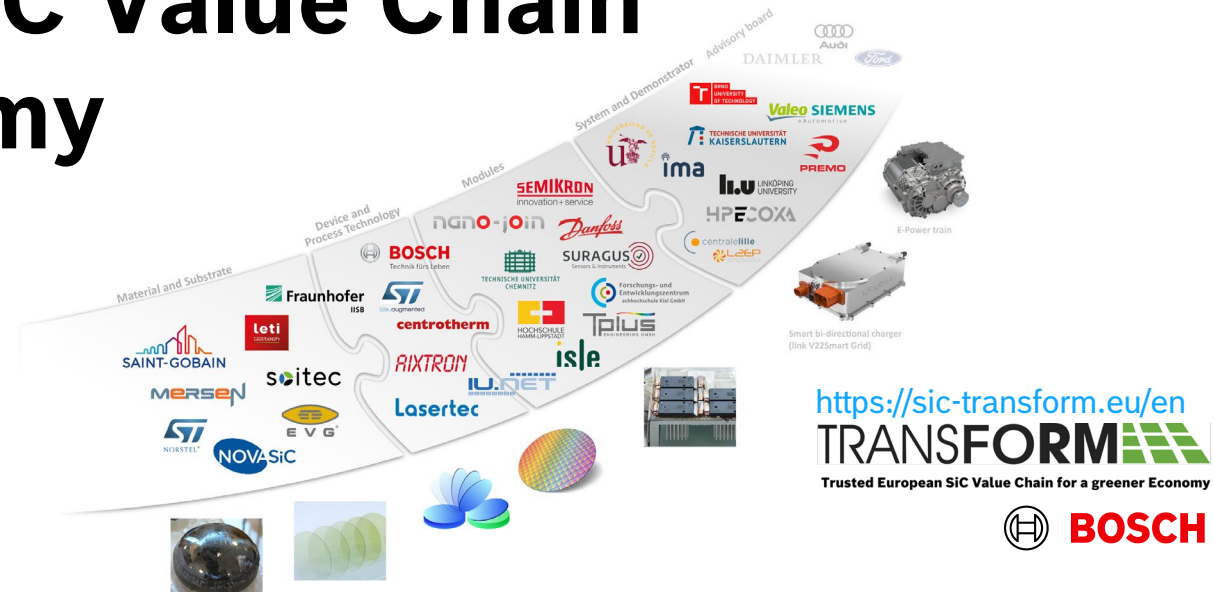


TRANSFORM: Trusted European SiC Value Chain for a greener Economy

Metin Koyuncu
Robert Bosch GmbH
Reutlingen, Germany



Trusted European SiC Value Chain for a greener Economy

Outline

- The European Consortium for SiC value chain
- SiC Engineered Substrates
- Cu based AIT
- Advanced Power Modules
- Applications in Use Cases
- Summary and Conclusion

01

A European Consortium for a complete and competitive SiC value chain

The European Consortium European SiC Value Chain

TRANSFORM
Trusted European SiC Value Chain for a greener Economy
<https://sic-transform.eu/en>

KDT JU
KEY DIGITAL
TECHNOLOGIES
JOINT UNDERTAKING



Key Digital Technologies Joint Undertaking
(KDT JU) Grant Agreement No 101007237



34 Partners

from 7 European Countries

4 RTOs, 7 Universities, 6 SMEs, 17 Industrial Partners

April 2023 to October 2024

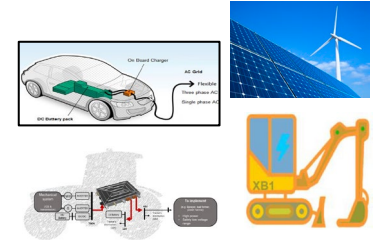
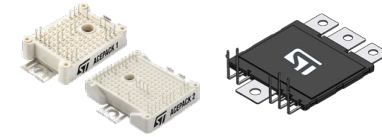
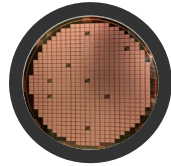
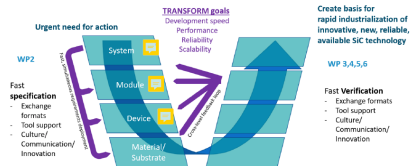


Demonstrate a European SiC Value Chain with Innovations



The European Consortium

The SiC Value Chain



Requirements

Materials & Advanced Substrates

SiC MOSFET Technologies

Power Modules and Reliability

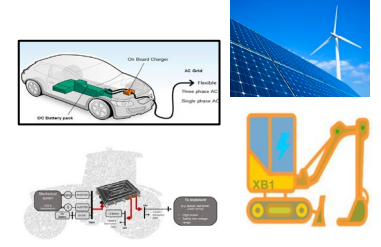
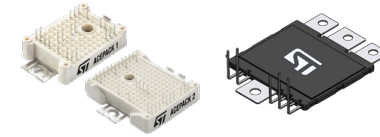
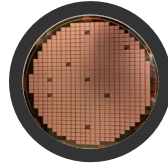
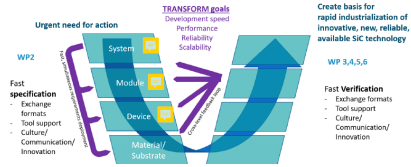
System Demonstrators



The European SiC value chain is established from materials to system demonstrators in 4 key application areas, with innovations in SiC substrates, equipment technology, devices, power modules, ...

The European Consortium

The SiC Value Chain



Requirements

V-methodology
System to substrate level
Based on use cases in 4 application fields

Materials & Advanced Substrates

150 mm, 200 mm substrate techn.
▶ SmartCut Process
Pilot line → manufacturing line
Donor wafers
Handle wafer prod. techn.
Metrology
150 mm, 200 mm

SiC MOSFET Technologies

Trench MOSFET techn.
Planar MOSFET techn.
200 mm planetary epi-reactor
200 mm activator
Substrate/ epi-layer characterization

Power Modules and Reliability

SIC device charact. methods
Gate driver optimization
▶ Cu-based AIT
Power module design
▶ Power module manuf. techn.
Power module reliability
Digital twins
Standardization
Testing services

System Demonstrators

▶ Automotive traction inverter
V2x bidirectional charger
Converters for actuators in agriculture
Industrial battery charger
PV string converter

Benchmarking in the value chain compared to the baseline technologies and SotA

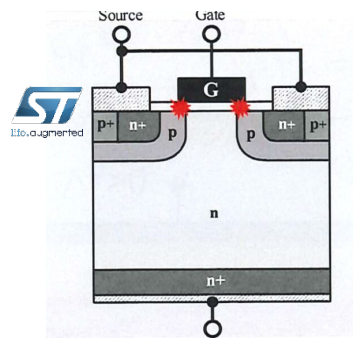
02

SiC Engineered Substrates

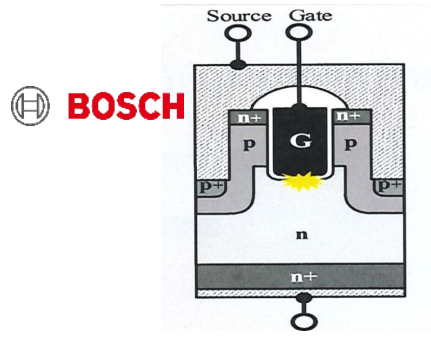
SiC Engineered Substrates

Technology and Benchmarking to SotA

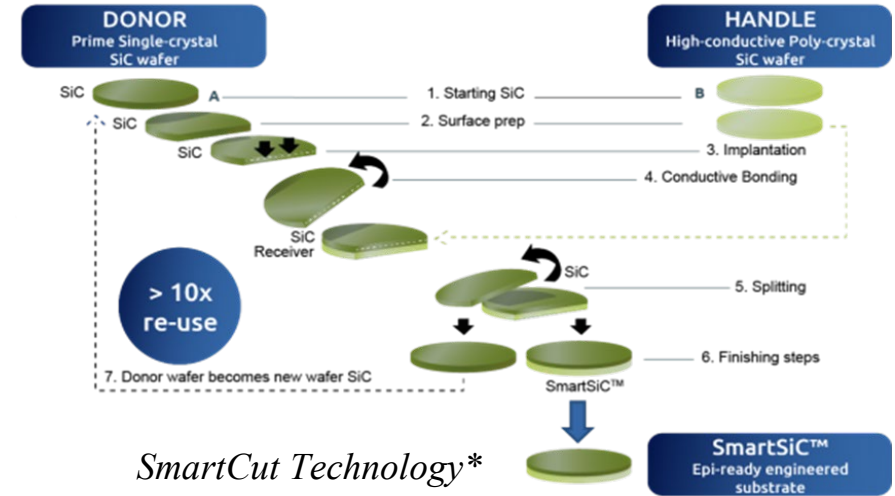
- SmartCut™ technology*: Integration of high quality thin (350-800nm) mono-SiC layer onto a 350μm thick low resistivity poly-SiC handle wafer (< 10mOhm.cm)
- Device processing at series manufacturing line
 - Two technology paths: Planar and Trench MOSFETs at STMicroelectronics and Bosch, respectively.



Planar MOSFET
@ STMicroelectronics,
Italy



Trench MOSFET
@ BOSCH,
Germany



SmartCut Technology*

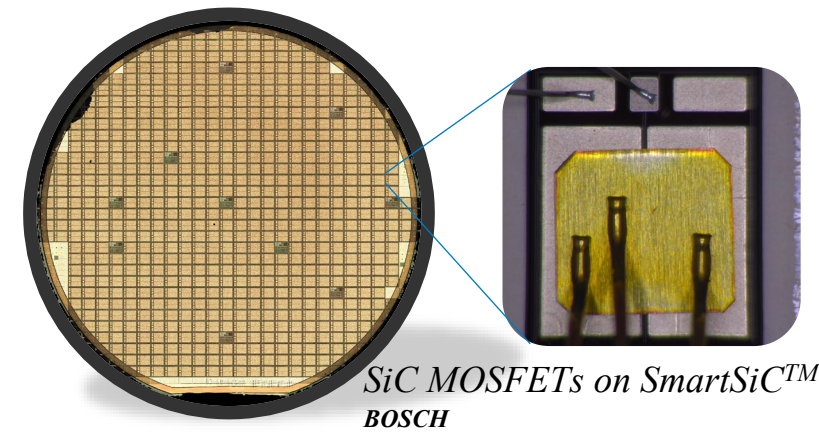
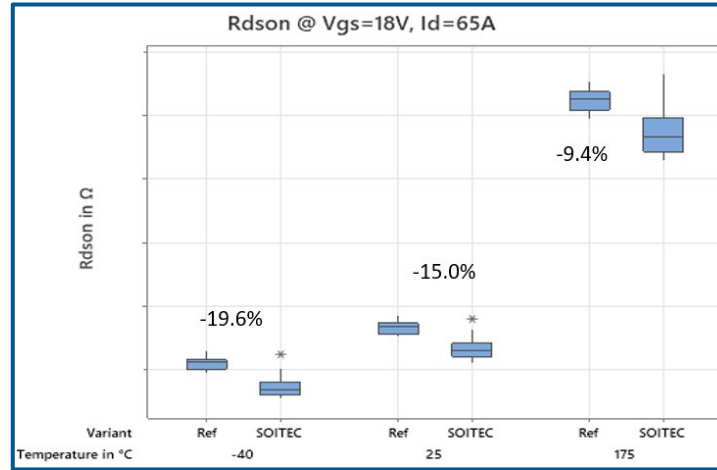
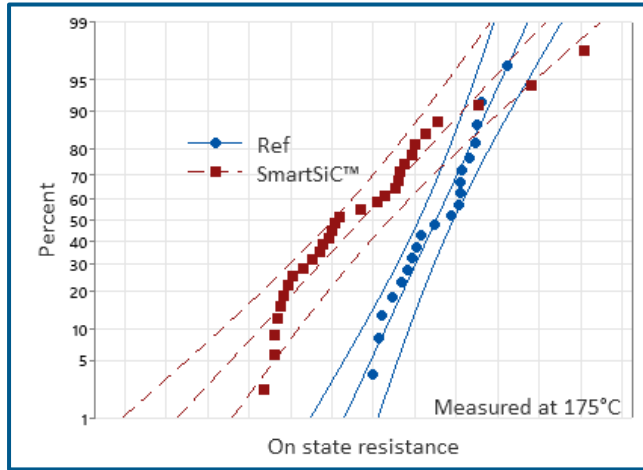
SmartSiC™ wafers*



* E. Guiot *et.al.*, "SmartSiC™ 150 & 200 mm Engineered Substrate: Enabling SiC Power Devices with Improved Performances and Reliability," ICSCRM 2024, Rayleigh, USA, 2024

SiC Engineered Substrates

Technology and Benchmarking to SotA



Parameter	Comparison SmartSiC™ vs. Reference	
I_{DSS} & I_{GSS}	No Increased leakage observed	Green
V_{BRDSS}	Approx. 50 V lower	Light Green
V_{Th}	Slightly lower	Light Green
$R_{DS,On}$	~10-20% lower; temp. dependent	Dark Green
Short circuit	Critical destruction energy reduced	Yellow

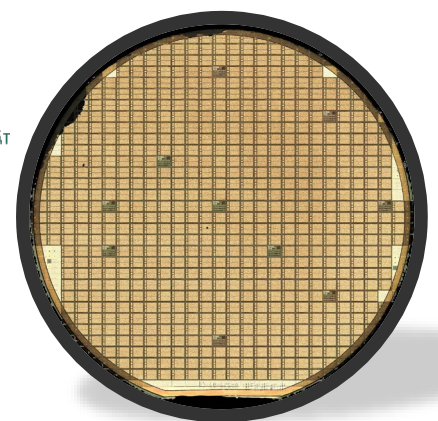
➤ Manufacturability challenges:

- Optical properties
- Bow & warp

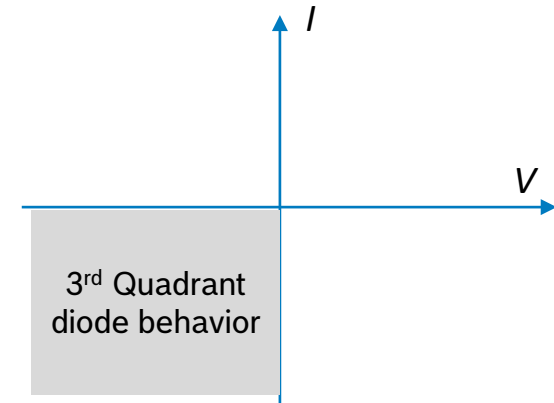
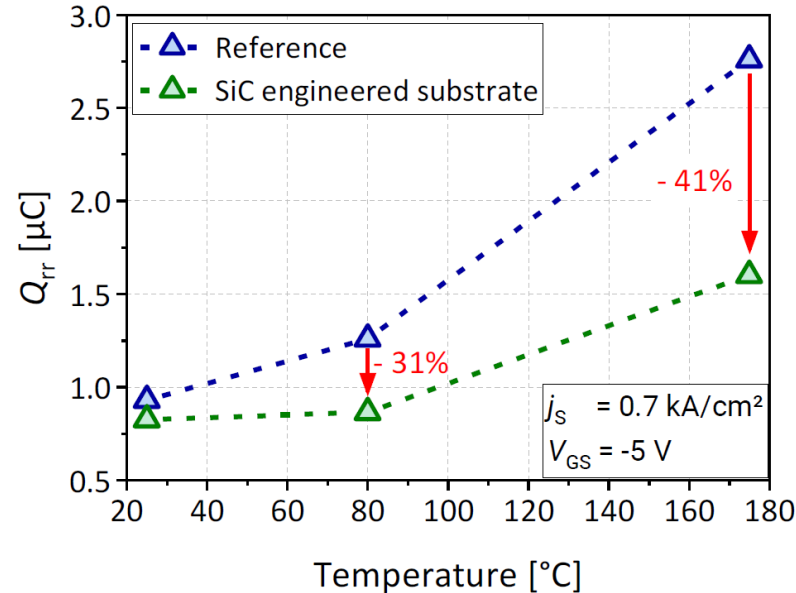
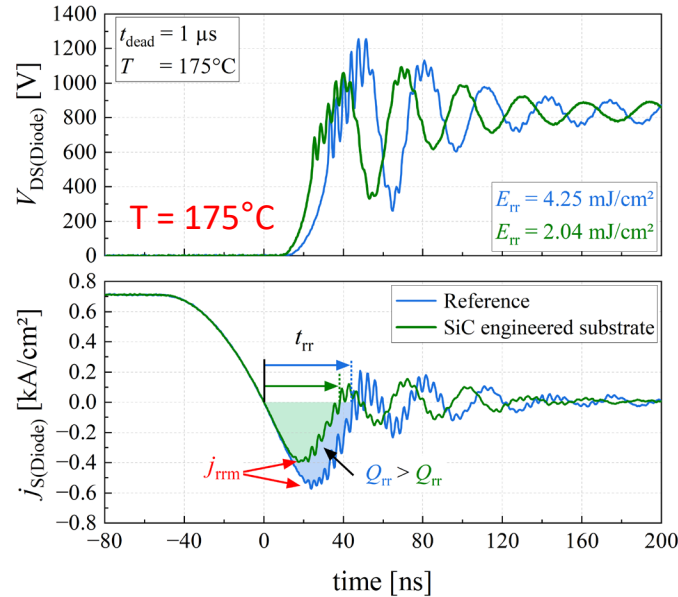
➤ Devices on SmartSiC™ exhibit 10-20% lower $R_{DS,ON}$ depending on temp., but with higher spread

SiC Engineered Substrates

Technology and Benchmarking to SotA



$V_{DS} = 850 \text{ V}$, $V_{GS}(\text{Diode}) = -5 \text{ V}$ and $j_S = 0.7 \text{ kA/cm}^2$

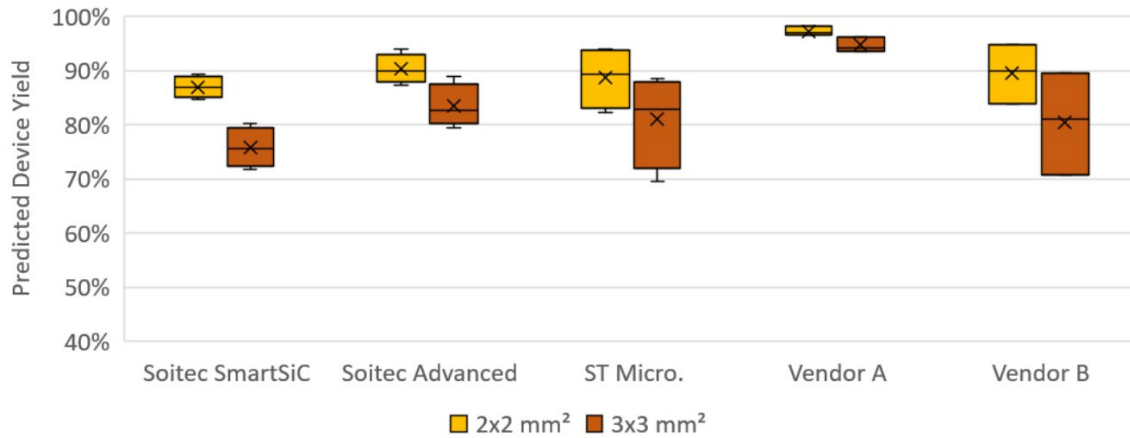


- Q_{rr} (reverse recovery charge) is reduced by increasing temperature for devices based on SiC engineered substrates, reason still in investigation

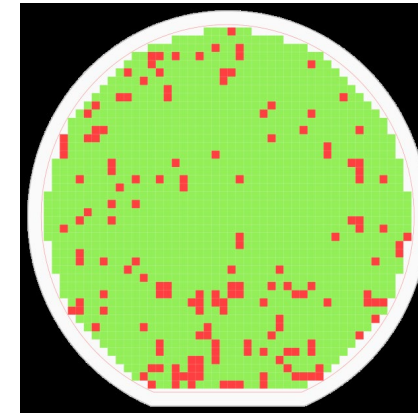
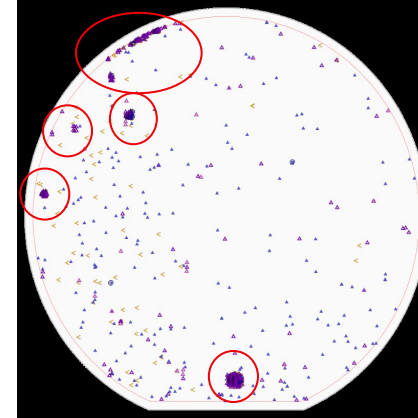
M. Alaluss *et. al.*, "Dynamic Characterization and Robustness of SiC MOSFETs Based on SmartSiC™ Engineered Substrates," *ICSCRM 2024*, Rayleigh, USA, 2024

SiC Engineered Substrates

Technology and Benchmarking to SotA *RIXTRON*



- Still some bonding failures leading to localized polycrystalline growth in the epi process.
- Nr. of killer defects vs yield is inconsistent.
- Continuous yield improvement with further generations of SiC Engineered Substrates.



False defect recognition at bonding defects cause high numbers for killer defects



Defect numbers from automatic count are not representative



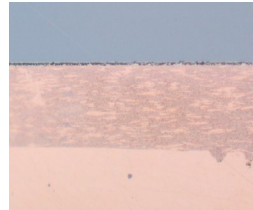
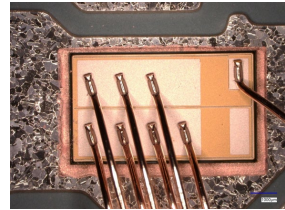
But only a small area is affected by clusters

03

Cu-based Assembly and Interconnection Technology (Cu-AIT)

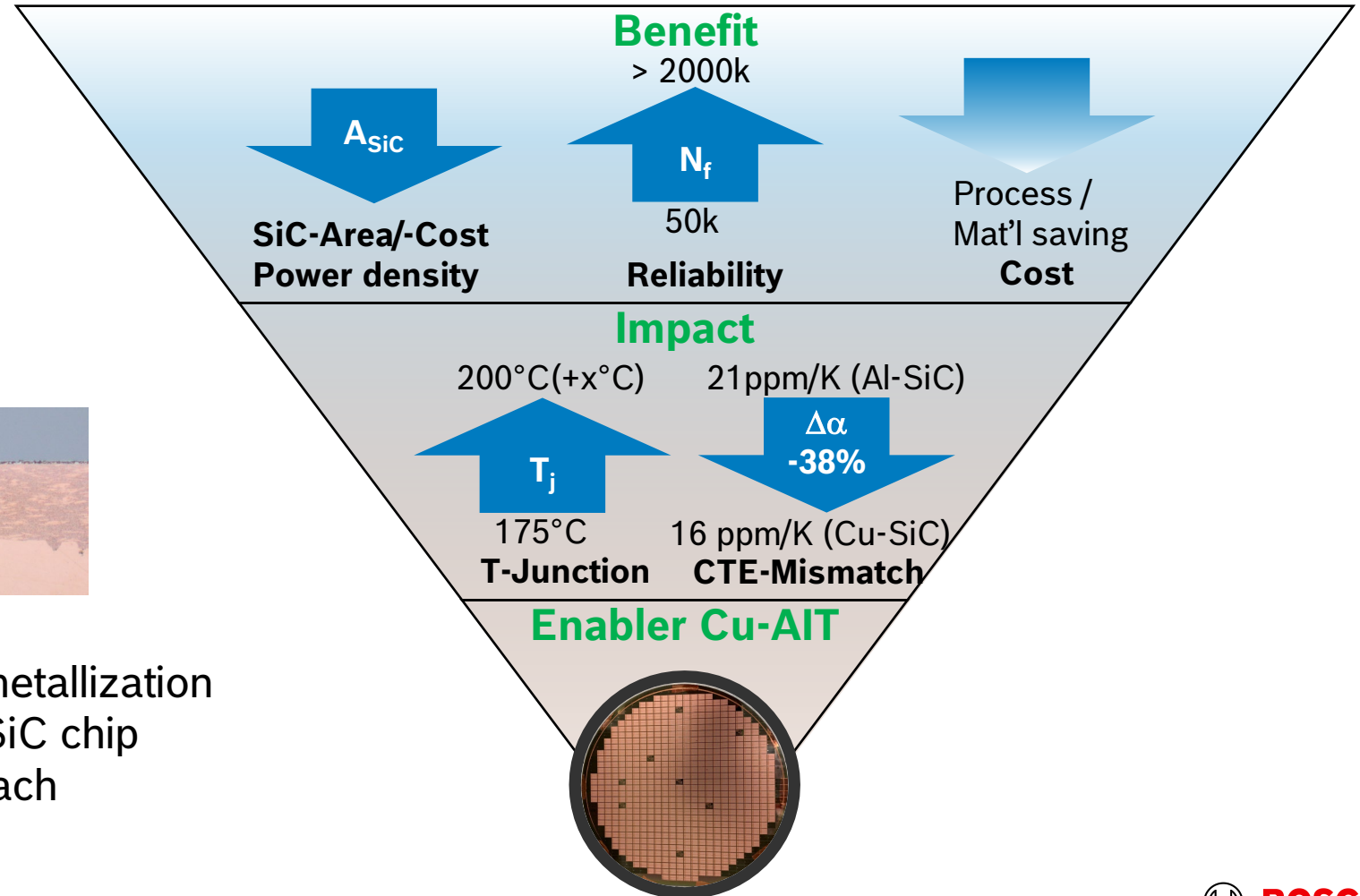
Cu-AIT

Strong contribution to Electrification



Cu-AIT:

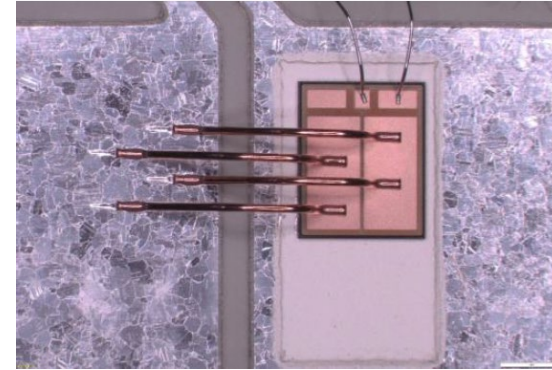
- SiC with Cu top-side metallization
- Cu-bonds directly on SiC chip
- Cu sintering as die attach



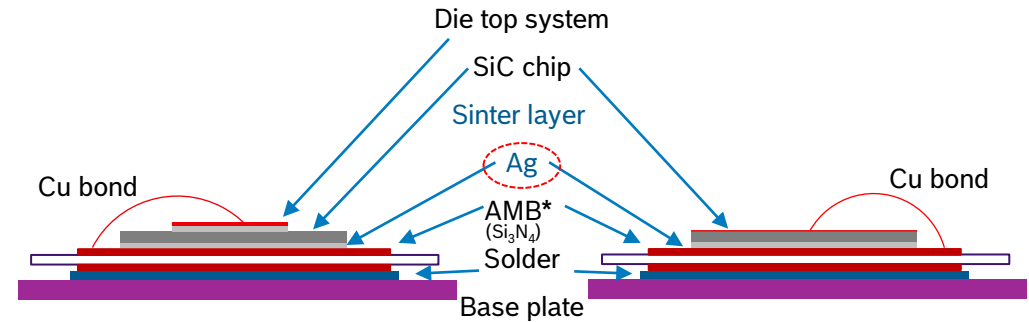
Cu-AIT

Test assembly - 1

- Cu based AIT for automotive applications
 - Cu bonding directly onto SiC MOSFET with Cu top-side metallization
 - Ag sintering
-
- Test Chip 1200V MOSFET
 - Chip size: 24 mm²
 - Chip thickness: 300 μm
-
- Package
 - Unmolded test vehicle



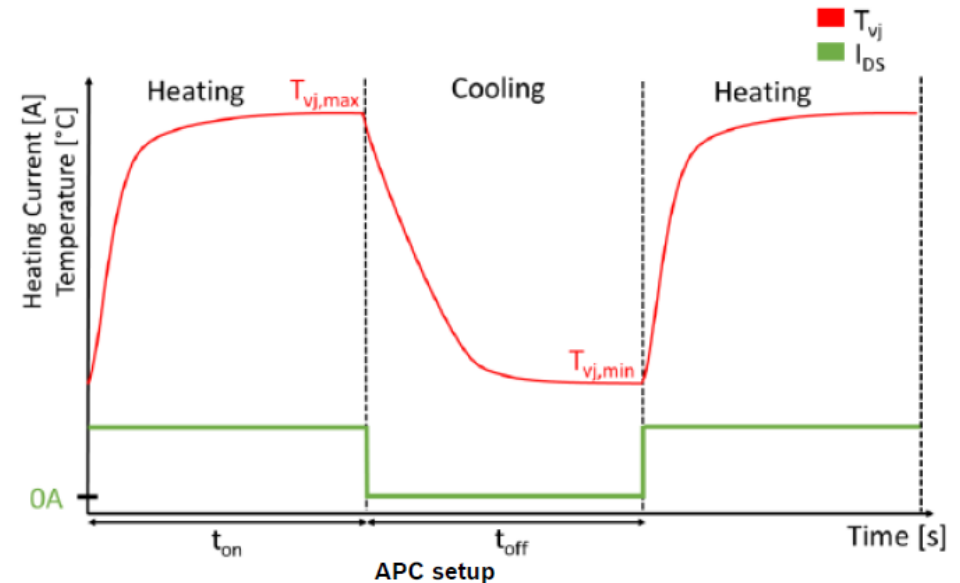
*Test assembly - 1, BOSCH
(Chip on substrate)*



Cu based AIT

pCT Test Conditions – Test Assembly -1

Parameter	Value
ΔT_j [K]	130 / 150 / 170
t_{on} [s]	2
t_{off} [s]	3
$V_{GS(on)}$ [V]	12-20
$V_{GS(off)}$ [V]	-10
T_{cooler} [C]	55 / 45 / 35



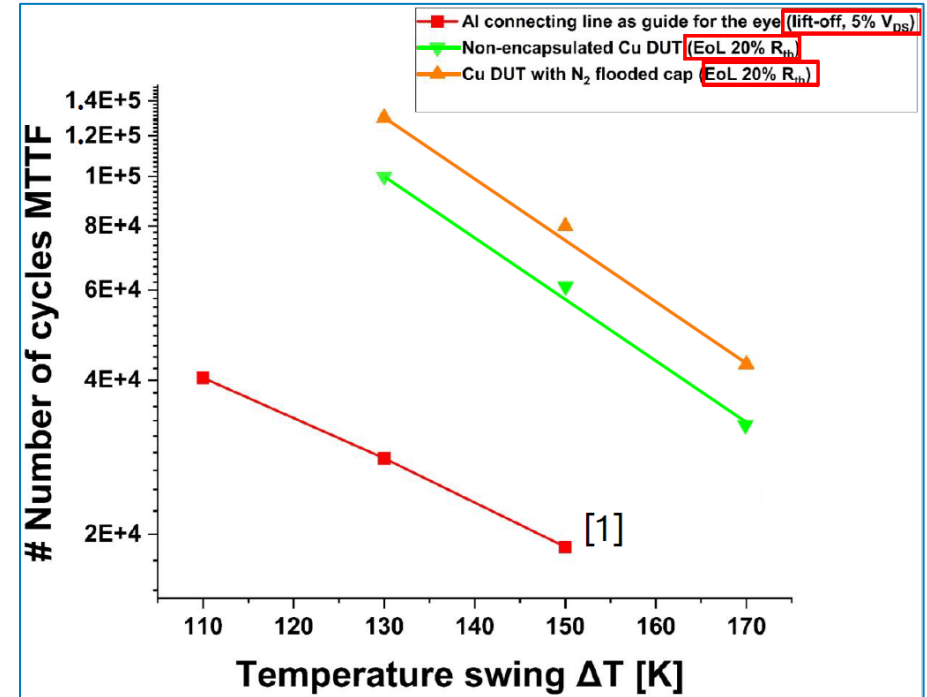
Schematics of test conditions

➤ Tests were executed under ambient and N_2 atmosphere to observe the effect of oxidation.

Cu-AIT

Results – Test Assembly - 1

- >3x reliability improvement at $\Delta T = 130$ and 150 K compared to Aluminum-AIT
- Reliability improvement under N_2 atmosphere in general
- Failure mode (Cu-AIT): R_{th} increase > 20% due to **degradation of Ag sinter layer** under chip



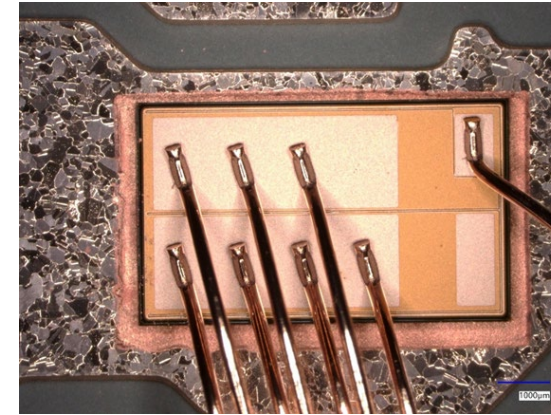
[1] R. Sankari *et al.*, "Degradation Mode Analysis of Different Bonding Technologies of SiC Power Semiconductors Stressed by Active Power Cycling," *PCIM Europe 2024*, Nürnberg, Germany, 2024, doi: 10.30420/566262024

R. Sankari *et al.*, „Degradation Mode Analysis of Cu Bondwires on Cu plated SiC Power Semiconductors Stressed by Active Power Cycling,“ *ESREF 2024*, Parma, Italy, 2024

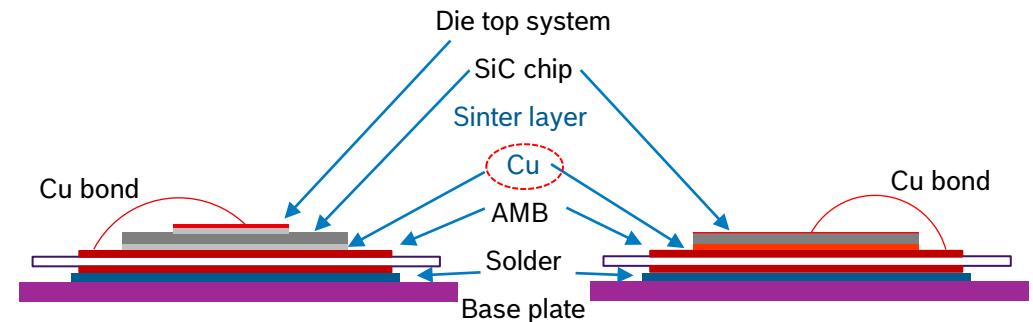
Cu-AIT

Test Assembly - 2

- Cu based AIT for Automotive applications
- Cu bonding directly onto SiC chip with Cu top-side metallization
- Cu sintering
- Test Chip 1200V MOSFET
 - Chip size: 31 mm²
 - Total chip thickness: 370 um
- Package
 - Molded and unmolded power modules



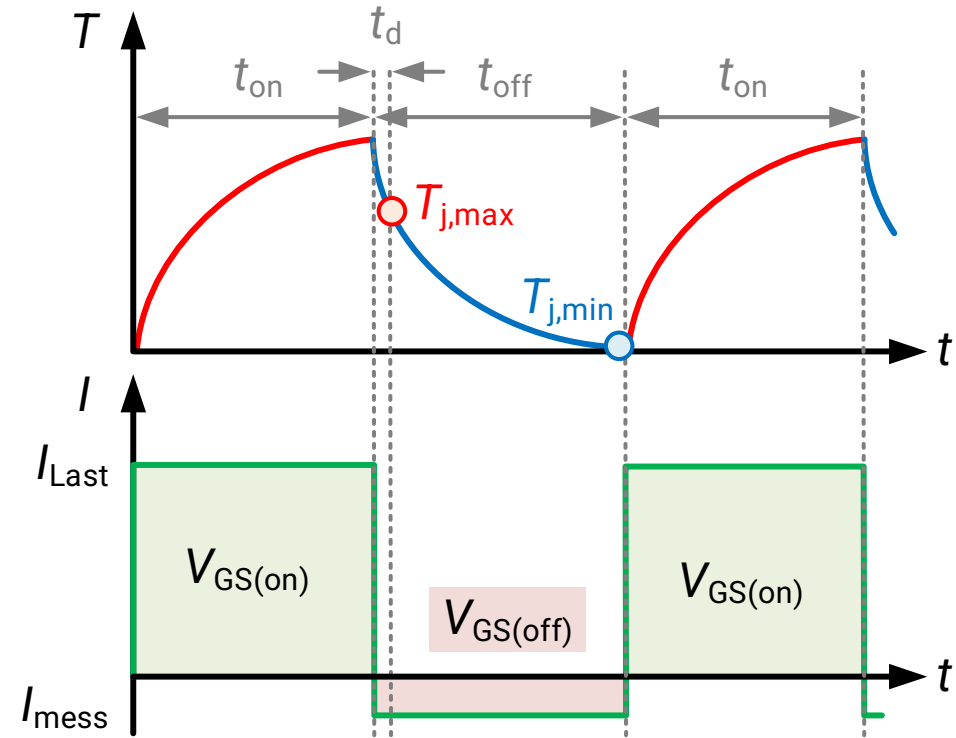
*Test assembly – 2
(power module)*



Cu-AIT

pCT Test Conditions - Test Assembly - 2

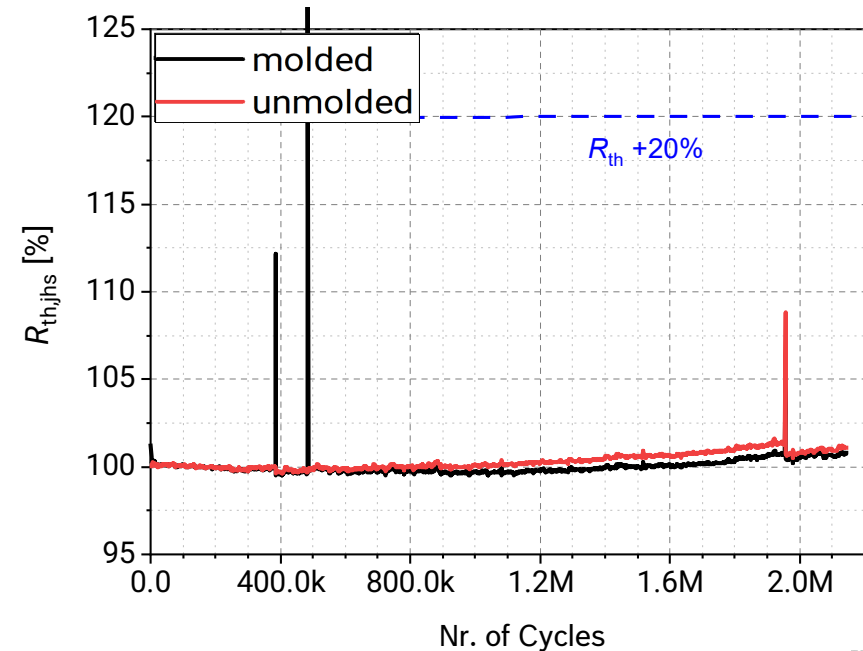
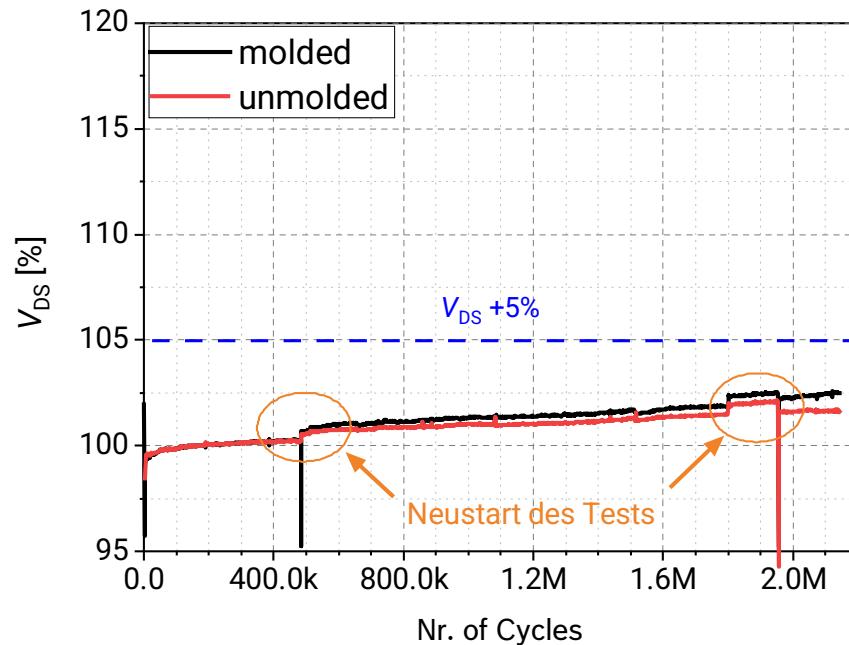
Parameter	Value
$T_{j,max}$ [°C]	175
ΔT_j [K]	110
I_{Last} [A]	105
t_{on} [s]	1
t_{off} [s]	2
$V_{GS(on)}$ [V]	12-20
$V_{GS(off)}$ [V]	-10
T_{inlet} [°C]	59
t_d [μs]	200



Schematics of test conditions

Cu-AIT

Results - Test Assembly - 2



- End-of-Life criterium ($R_{DS(on)} / R_{TH}$) **not reached at ~2.2 Mio. cycles!**
- Testing was stopped before EoL criterium was reached.

M. Alaluss et al., "Vorder- und Rückseitige Kupfer-AVT für SiC MOSFETs in Automotive Leistungsmodulen," *Halbleiterkolloquium 2024*, Freiburg, Germany 2024

04

Advanced Power Modules

Advanced Power Modules

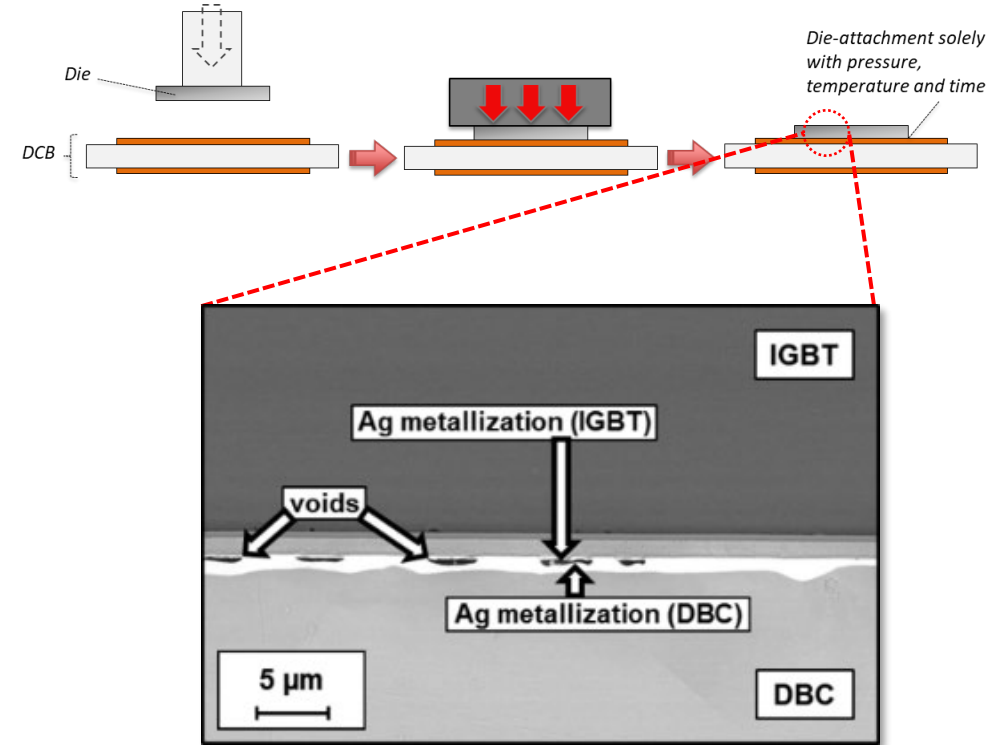
Direct Bonding – A New Die Attach Technology (HSHL)

Approach and Motivation

- Silver sintering suffers from complex process and costly materials and equipment
- Potential reduction of process complexity and material costs by **omitting sinter paste** and directly bonding die BSM and substrate metallization: *Direct Bonding*!

First Steps

- Investigation on effect of chip metallization (Ag, Pd, Au) on joint formation
- Bonding strength depends on combination of metallization for same process parameters
- *Best: Ag/Ag*



Advanced Power Modules

Direct Bonding – A New Die Attach Technology (HSHL)

Reliability of Direct Bonded **IGBT** in Power Cycling Test (PCT)

- 20 samples (Ag/Ag) in PCT upto 651,000 cycles @ $\Delta T=100$ K...125 K before EOL
- Using 125 μm Al-bonds reliability exceeds conventional power modules with sintering & thick Al-bonds
- Three failure mechanisms:
 - a) Degradation of the Al wire bonds
 - b) Delamination within the backside metallization of chip
 - c) Delamination of DBC-copper

None of them occur at the direct bonding interface

Reliability of Direct Bonded **SiC** Diodes in PCT

- Again using 125 μm Al-bonds for top-side interconnect, best sample reached >600,000 cycles @ $\Delta T \approx 100$ K
- But: several samples failed <50k cycles with failure (b)

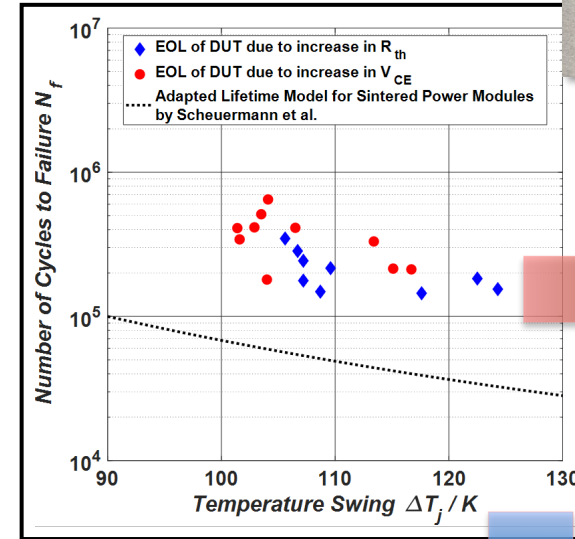
Curkin *et al.* "Effect of Chip Metallization and Process Parameters on the Die Attach Properties of Direct Bonded Power Devices," ECTC 2023, Orlando, USA, 2023

Köhler *et al.* "Reliability and Failure Mechanisms of Direct Bonded Power Semiconductor Devices in Power Cycling Test," ISPSD 2024, Bremen, Germany, 2024

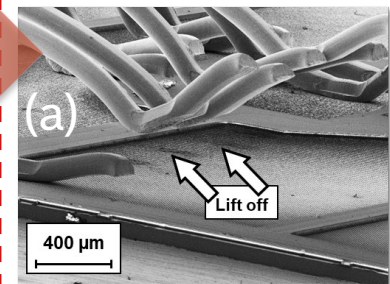
PCT Sample



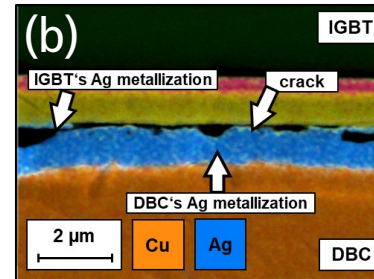
PCT Results



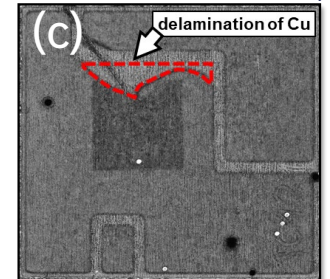
SEM: wire bond lift off



EDX: crack formation within BSM



SAM: delamination of DBC-copper

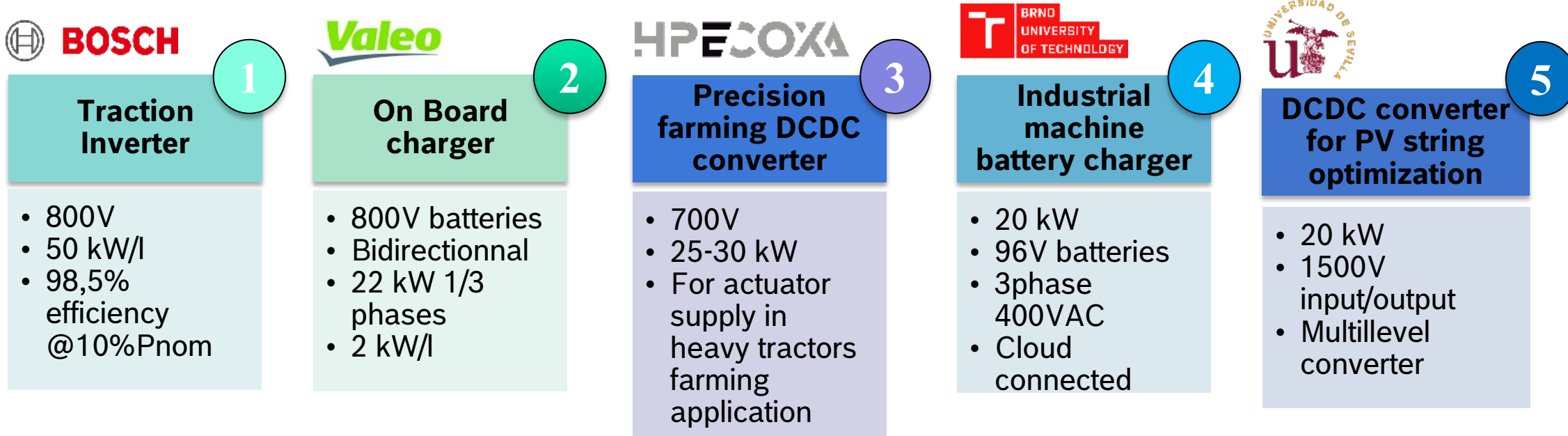


05

Applications in Use Cases

Applications in Use Cases

5 technical demonstrators in 4 key application areas

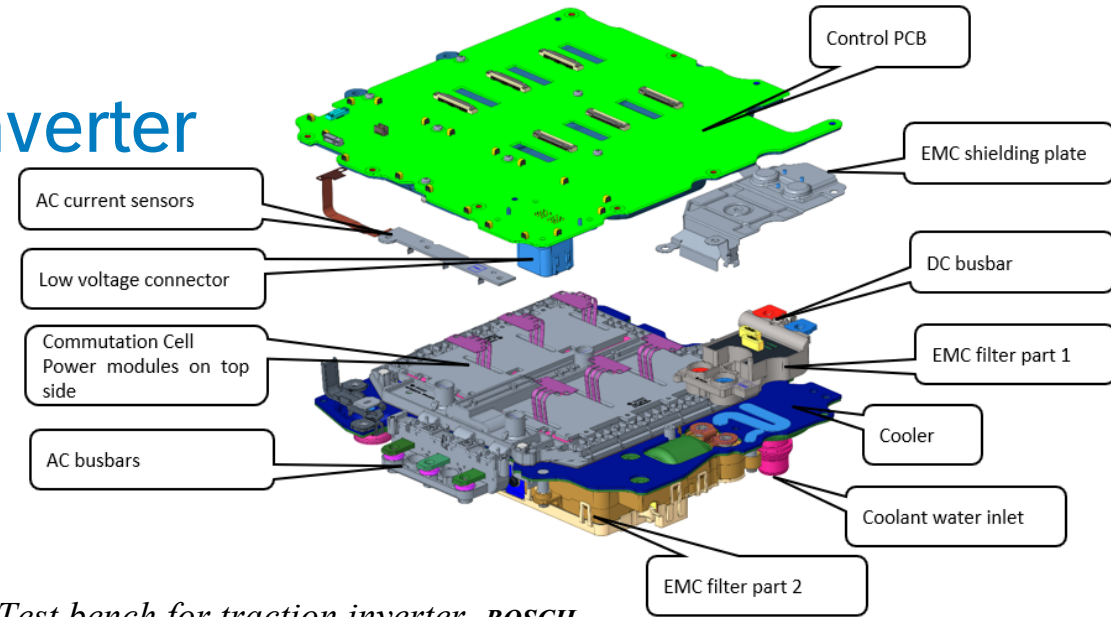


Benefit of SiC semiconductors, SmartSiC™, Cu-ALT technology was demonstrated with 5 different use cases in 4 key application domains.

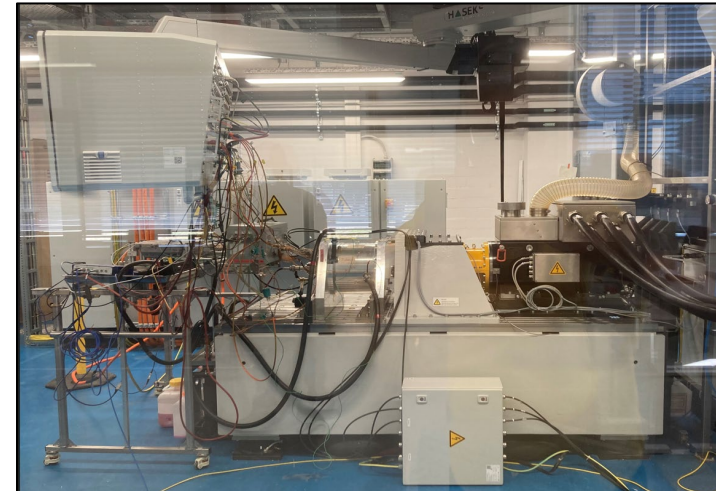
Applications in Use Cases

Use Case: Automotive Traction Inverter

- Automotive inverter using power module in **Cu based assembly and interconnection technology**
- Peak power (600 A) and continuous (300A) operation @ 835V are proven at test bench and under climatic conditions
- Power density of 50 kW/l
- Efficiency > 98.5% at 10% rated power is achieved



Test bench for traction inverter, BOSCH



*Traction inverter with Power modules in Cu-AIT
BOSCH*

06

Summary and Conclusion

Summary and Conclusion

Summary and further Collaboration

- TRANSFORM consortium has built up and demonstrated a complete European SiC value chain from substrate materials to system level.
- Engineered SiC wafers were evaluated and benchmarked to standard mono-SiC wafers:
 - 10-20 % advantage on $R_{DS,ON}$ depending on temperature
 - Decreased Q_{rr} hence decreased switching losses
 - Still some challenges on MOSFET fabrication
- Cu-based AIT provides significantly increased reliability and potential for cost effective products:
 - Demonstrated in automotive traction inverter under real application conditions
- New manufacturing technologies such as direct bonding offer more efficient manufacturing for power modules.
- Developed innovations are implemented in demonstrators in further application areas such as industry, agriculture and renewables.
- European value chain collaboration is continued in further projects.

ACKNOWLEDGEMENTS



This work has been carried out within TRANSFORM project which has received funding from the Key Digital Technologies Joint Undertaking (KDT JU) under Grant Agreement No101007237. The JU receives support from the European Union's Horizon 2020 research and innovation program and Germany, France, Italy, Sweden, Austria, Czech Republic, Spain.