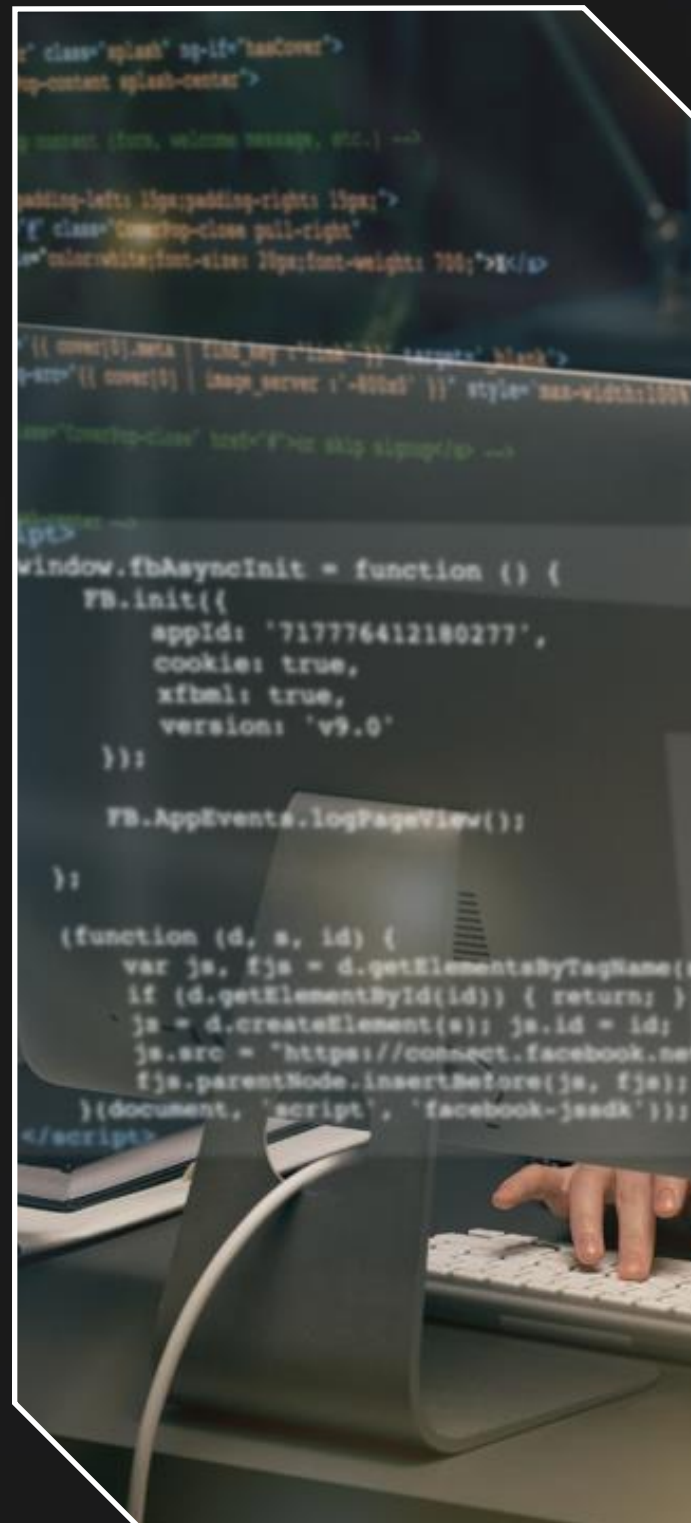


Cross-Language Code Synthesis for Hardware SoC Development



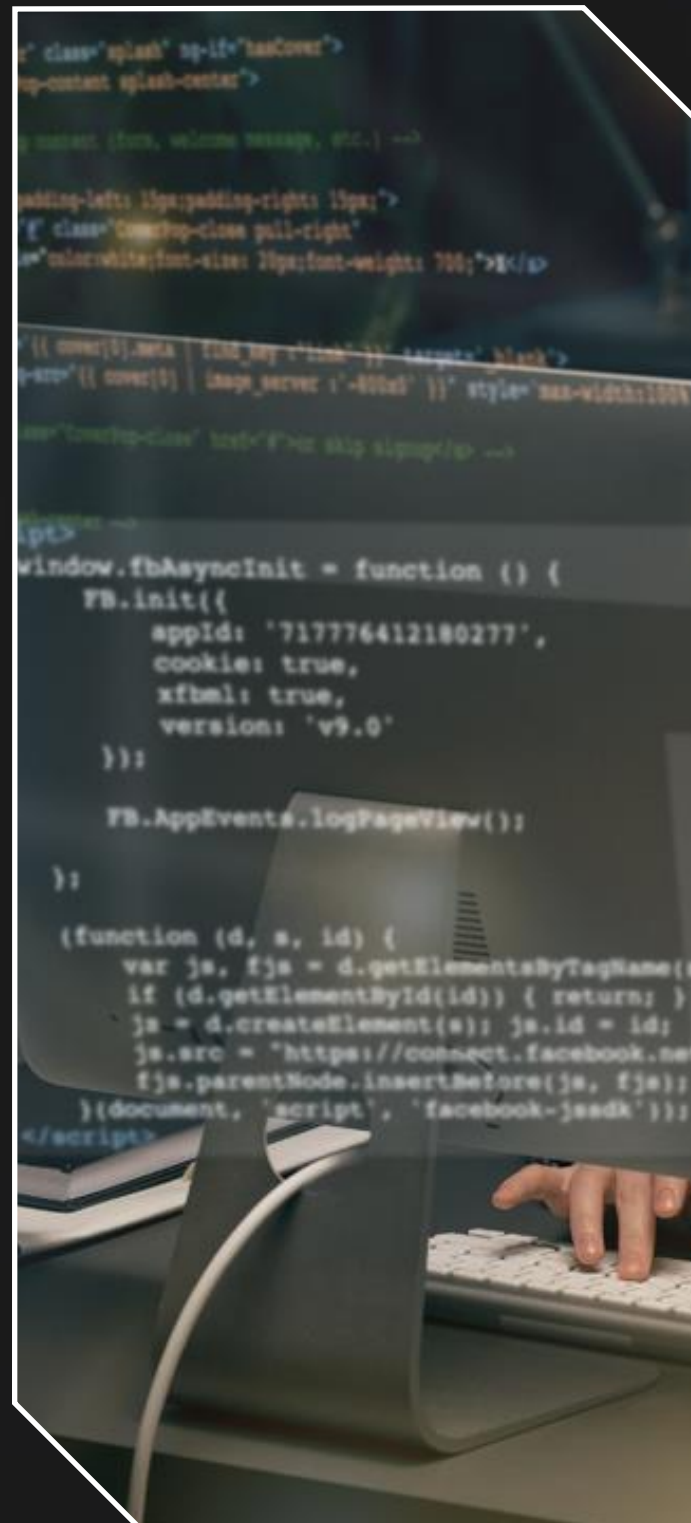
Platform X



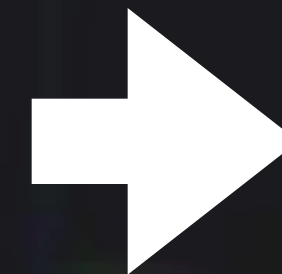
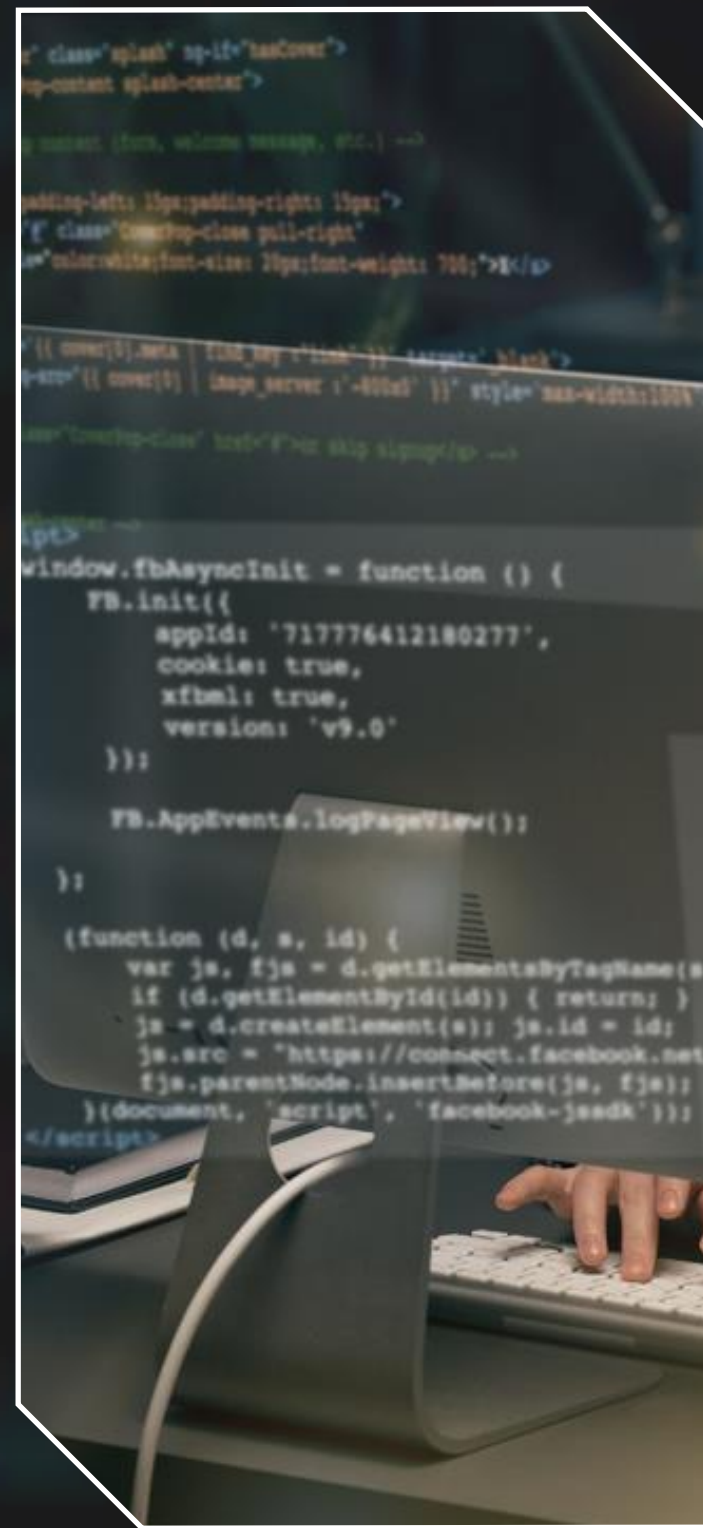
Application Developer



Platform Y



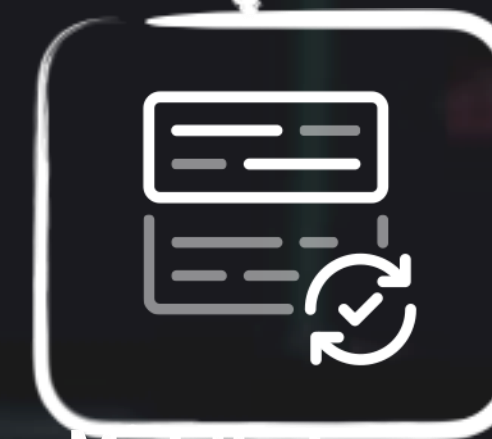
Framework Architecture



Python Code for Conversion



Python Framework



Middle Layer Interface



AI-Transformer



Code Optimiser



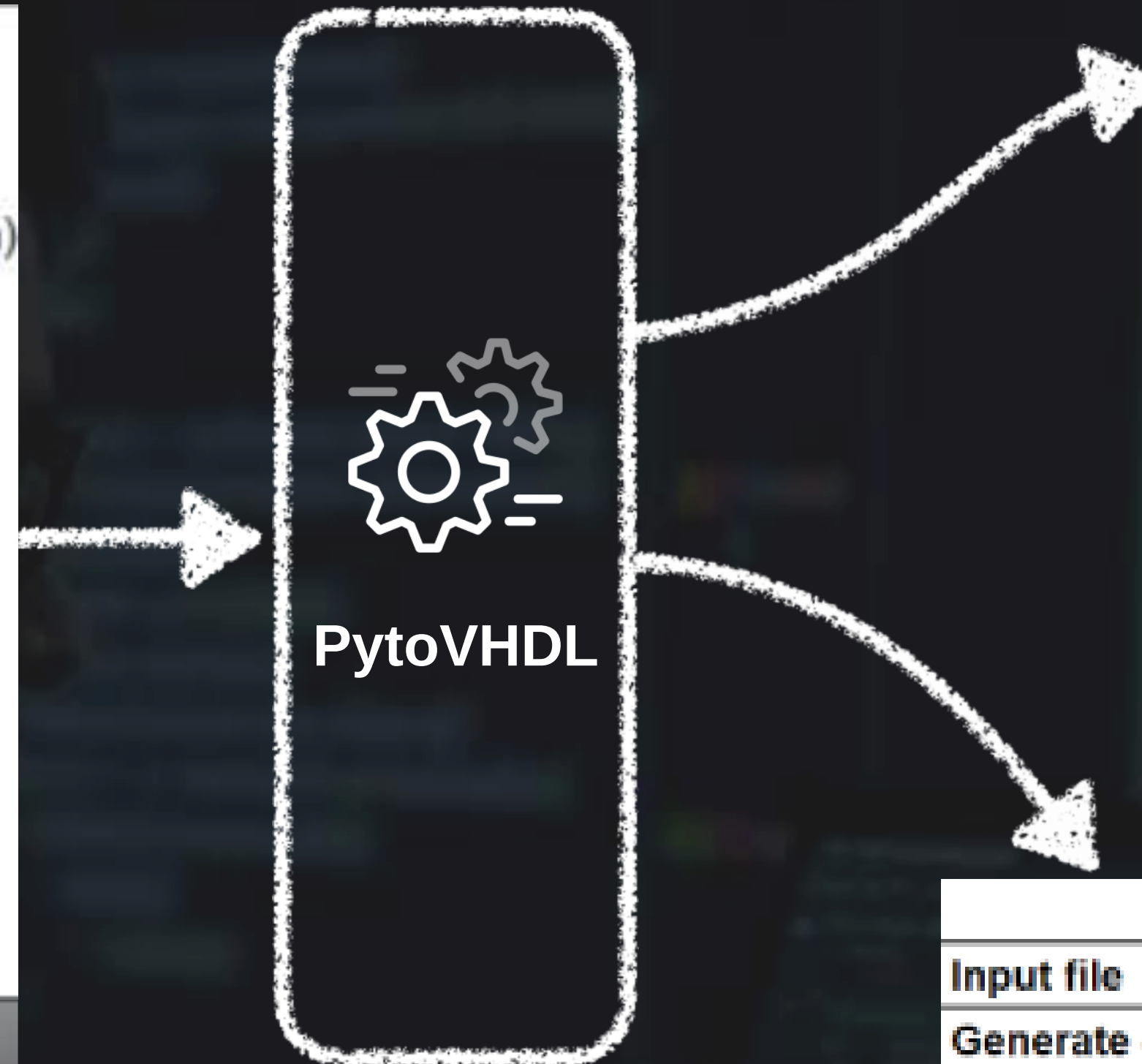
Final VHDL Code

Observed Results

```

1 from Classes.py2vdl import *
2 def Behavioral(sum,cout,x,y,cin):
3     sum = x ^ y ^ cin
4     cout = (x and y) or (x and cin) or (y and cin)
5
6 Entity(
7     name_entity= "add_1_bit",
8     port=[
9         Port("x,y,cin",IN, STD_LOGIC),
10        Port("sum,cout",OUT, STD_LOGIC),
11    ],
12    architecture=[
13        Body(Behavioral),
14    ]
15 )
16 )
17 ]
18 Body(Behavioral)
19 architecture=[
20     Port("sum,cout",OUT, STD_LOGIC)

```



```

1 : library IEEE;
2 : use IEEE.STD_LOGIC_1164.ALL;
3 :
4 : entity add_1_bit is
5 :     port (
6 :         x : in std_logic;
7 :         y : in std_logic;
8 :         cin : in std_logic;
9 :         sum : out std_logic;
10 :        cout : out std_logic
11 :    );
12 : end entity add_1_bit;
13 :
14 : architecture Behavioral of add_1_bit is
15 : begin
16 :     sum <= x xor y xor cin;
17 :     cout <= (x and y) or (x and cin) or (y and cin);
18 : end architecture Behavioral;

```

Generated VHDL Code

	Slice Luts	Slice Registers	IOB	BUFGCTRL
Input file	115	56	18	1
Generate 4	115	64	18	1
Generate 7	90	55	18	1
Generate 10	90	55	18	1
Generate 14	115	64	18	1
Generate 17	90	55	18	1
Generate 20	90	55	18	1

Resource Utilisation per N code generation

Thank you for your attention!

Our team at coffee break session:



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