



CONNECTS

Heterogeneous Integration for
Connectivity and Sustainability



Heterogeneous Integration Concepts for improved signal integrity performance

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Chapter

01 Motivation

02 Miniaturization & Modularization

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04 Heterogeneous Integration applied on CPO Demonstrator

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Motivation

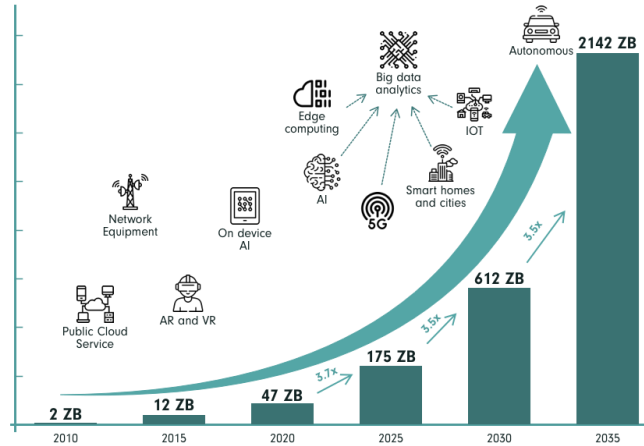
Increased data volumes
need to be transmitted,
stored and processed



Needed:

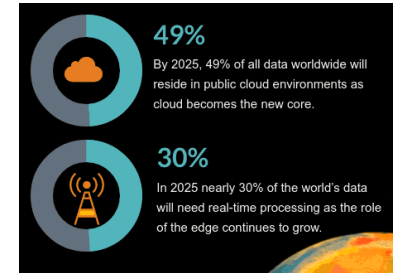
- Higher **Bandwidth**
- Lower **Latency**
- Higher **Energy** efficiency

Target applications



Source: Statista Digital Economy Compass 2019

1 ZB = 10^{21} Bytes
1 ZB = trillion GB



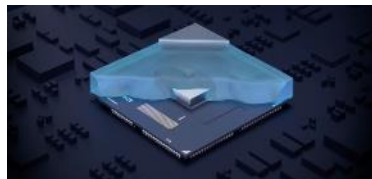
Source: IDC & Seagate Data Age 2025

DATA VOLUME is GROWING EXPONENTIALLY
Moving towards mmWave drives Miniaturization & Modularization

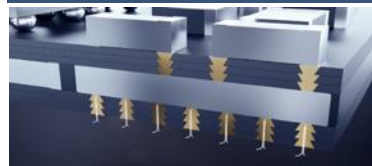
Miniaturization & Modularization



High-end PCB



IC substrate



Advanced Packaging

Used in nearly all electric devices

Consumer and Industrial electronics, Datacenter and Infrastructure, Medical

For miniaturization and performance

Mobile devices and wearables, computing, Advanced driver assistant systems, infotainment, sensors, patient care

High-end interconnects for AI

Optical modules, ultra-efficient power supply infrastructure and chiplet-ready substrates that create high-performance computing clusters for state-of-the-art AI applications

Packaging providing a value add

Heterogeneous integration, System in Package, Embedding, Improve Signal Integrity performance



Server & cloud



Automotive



HPC, AI, edge, IoT



5G / Networking



Client computing



Mobile Devices



Industrial



Aerospace



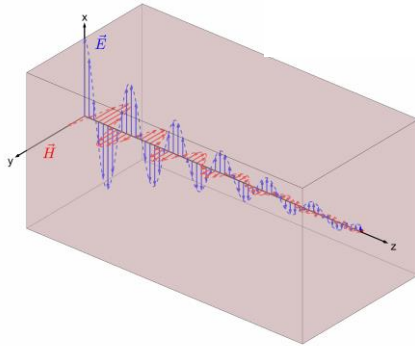
Medical

MINIATURIZATION & MODULARIZATION FOR BETTER SIGNAL INTEGRITY

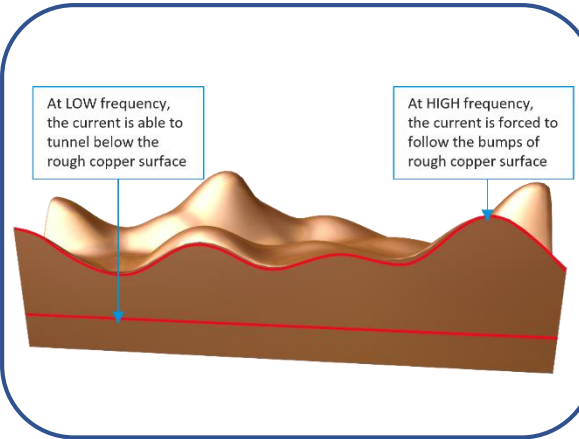
Signal Integrity - Influencing Parameter

What drives signal integrity?

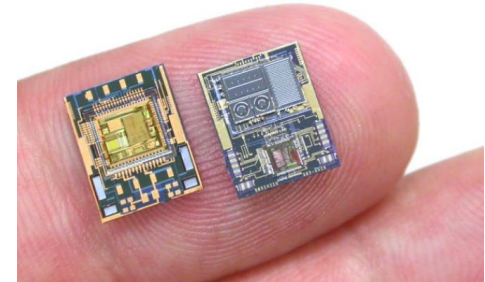
Dielectric Losses
Substrate materials



Conductor losses
Copper traces & patches



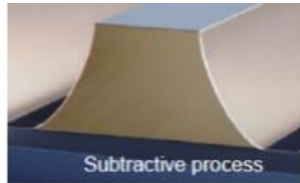
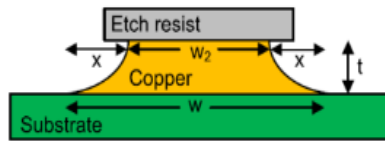
Design
Miniaturization & Modularization



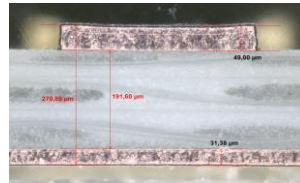
Design optimization – Structuring

Subtractive Etching vs. mSAP (modified Semi Additive Process)

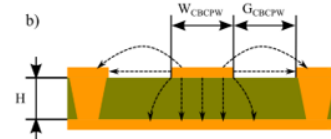
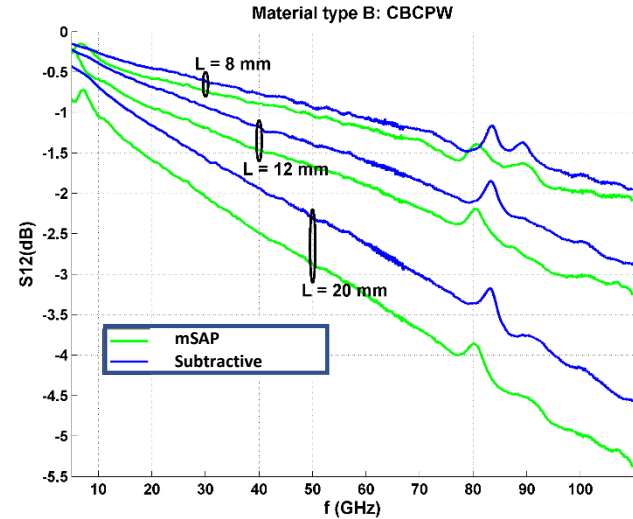
Subtractive Etching



mSAP



Impact on Signal Loss

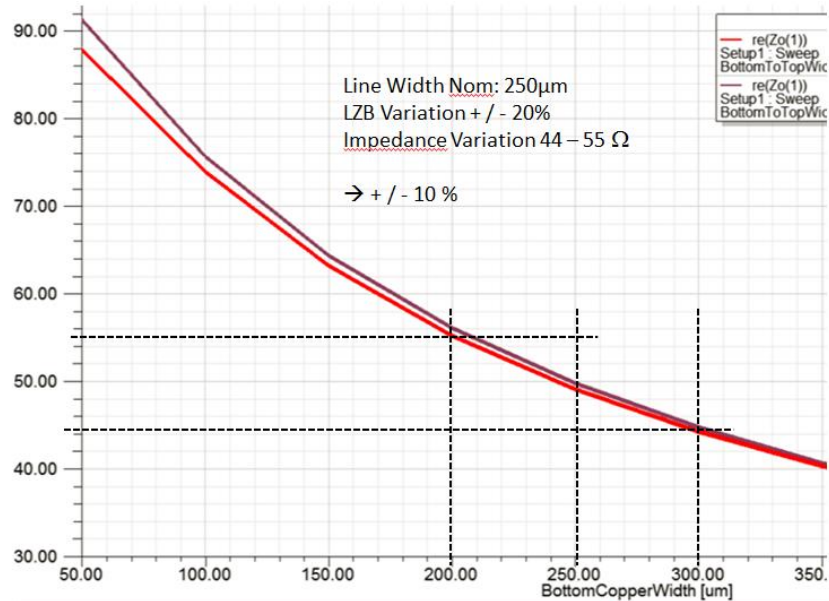


Line width mSAP: 250µm +/- 4%

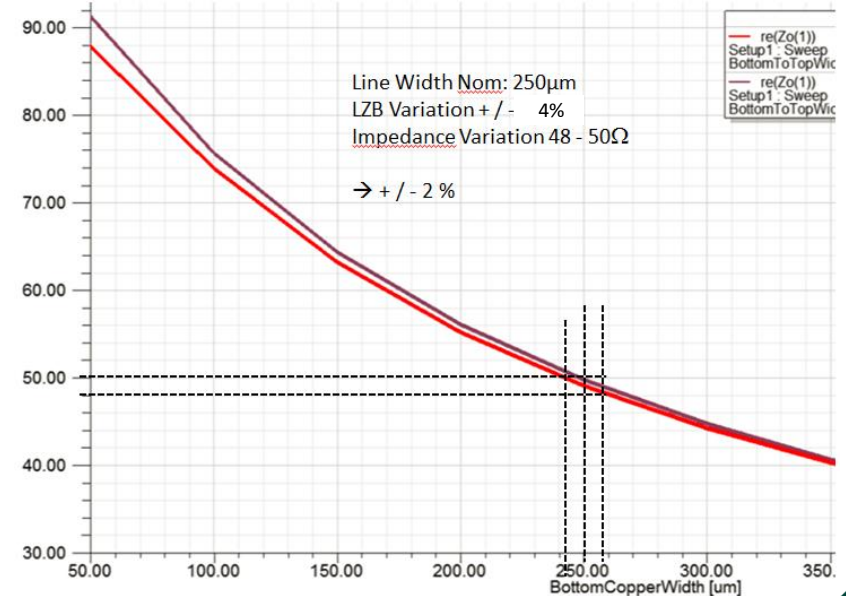
Line width Panel Plating: 250µm +/- 20%

Designoptimization - Structuring

Impedance Variation - Subtractive Structure



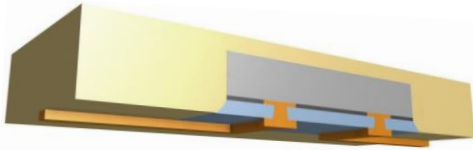
Impedance Variation - mSAP Structure



Embedding of components

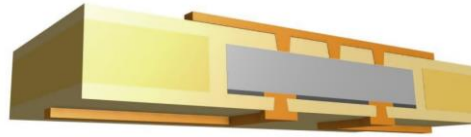
ECP®

The first choice for cost-efficient packaging of passive and small-size active components



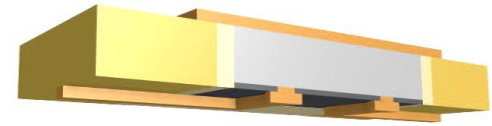
CENTER CORE EMBEDDING

The preferred packaging technology for power applications with double-sided component connection



PARSEC²

The thinnest possible embedded package for active component with a wide range of metallization types



Integrate active and passive Components

- Bare dies
- Single / double sided connected
- Si / GaAs / GaN ...
- Pad termination: Copper, Au, Al

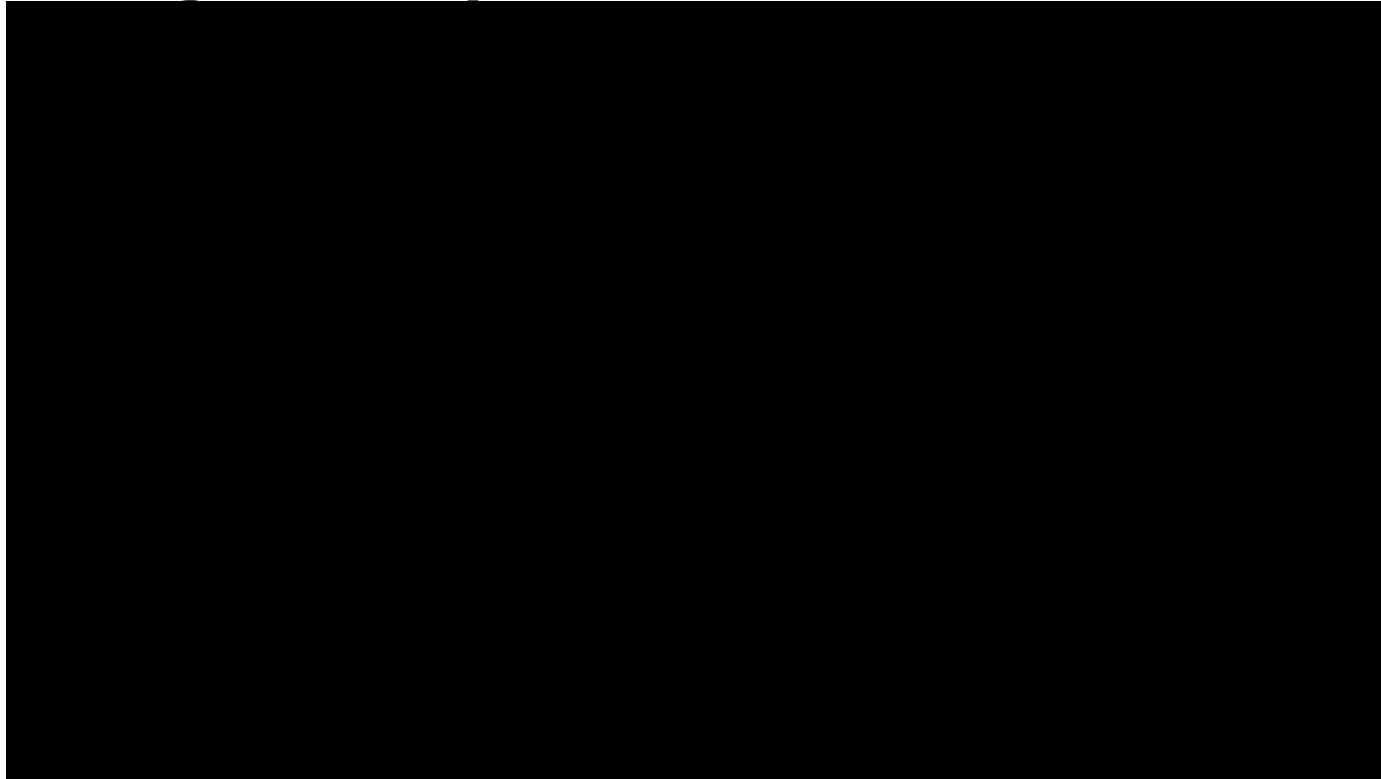
Performance Benefits

- Reduce Transmission losses
- Minimize Feeding Network length
- Split of Signal Path and Thermal Path
- More accurate Signal Path due Micro Via interconnection

Additional Benefits

- High Reliable Performance
- Stable against vibration
- Increase Packaging density
- Reduce weight
- Reverse Engineering protection

Embedding of components



Embedding of components

Center Core Embedding – Cross Section

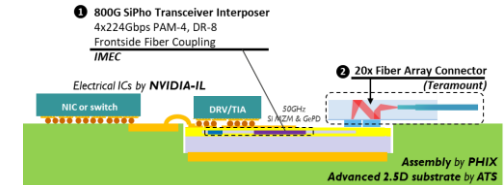
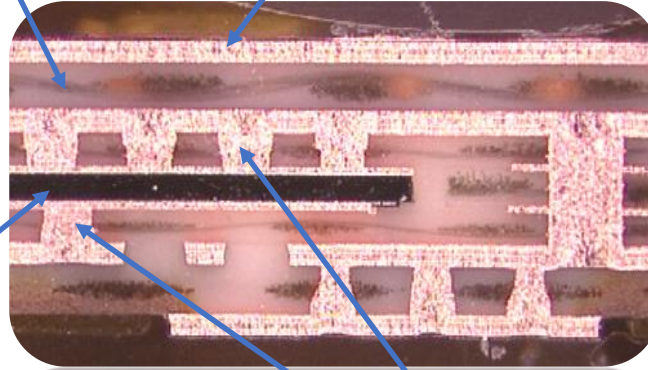
Prepreg

Copper foil + Galvanic Copper

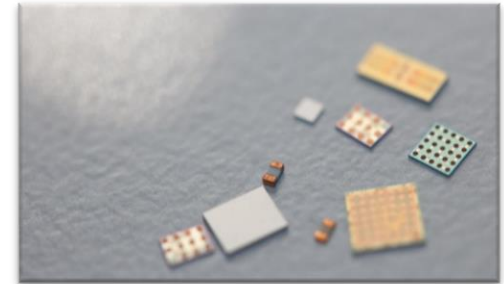
Interposer / PCB

Bare Die (single / double sided interconnected)

Laser Via / Galvanic Copper



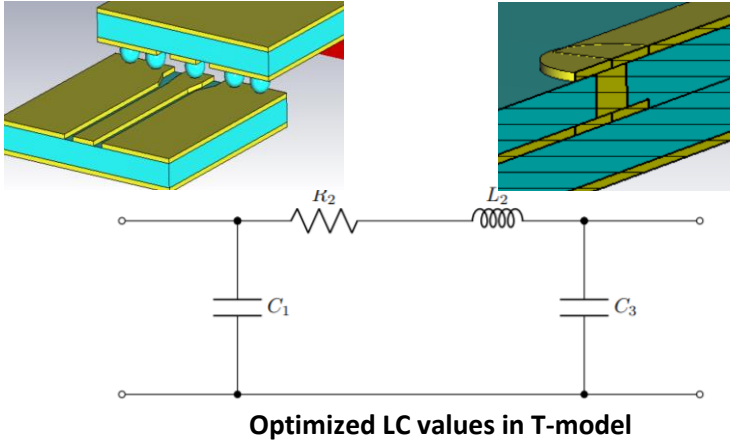
Embedding Concept in HiConnects



Pictures of IC-embedded package

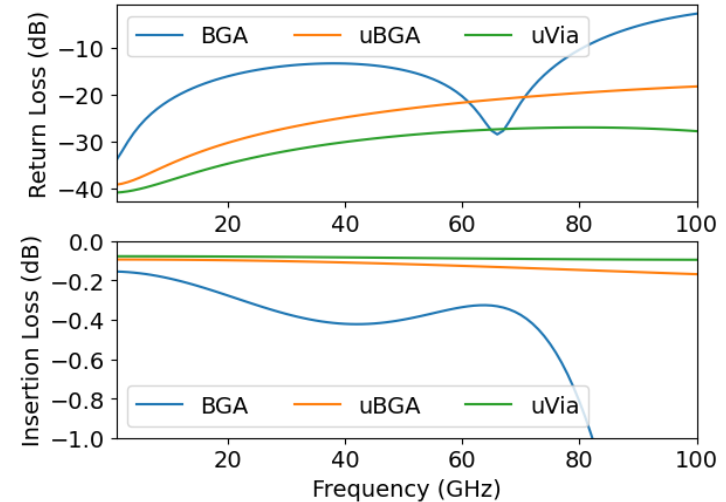
Embedding of components

Transition Analysis of Embedded Dies



	Diameter [μm]	C1 (C3), fF	L2, pH	R2, Ohm
BGA	Φ 100	52 (52)	200	1.8
Microvia1	Φ 100	12 (12)	47	0.9
μ BGA	Φ 30	10.6 (10.6)	30	1.09

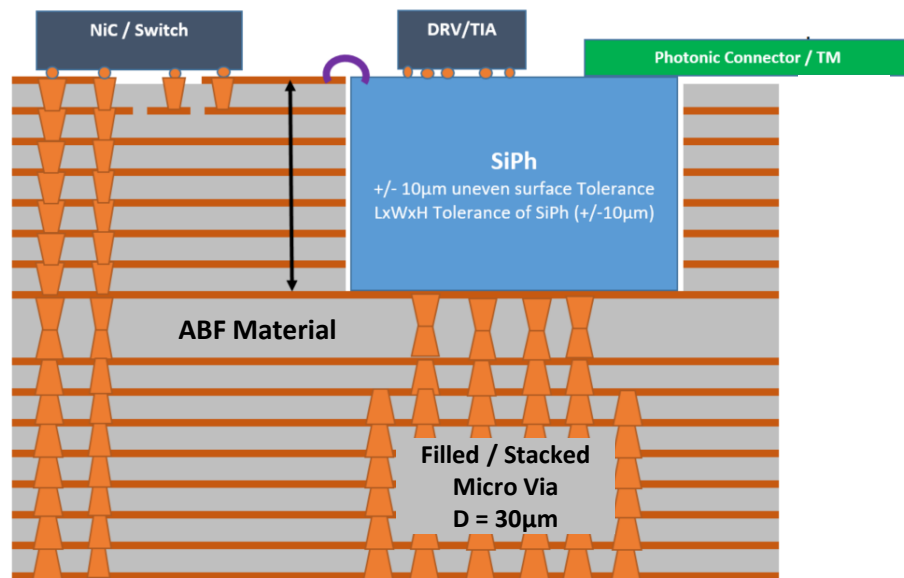
Simulation Results



Co Packaged Optics Demonstrator

Heterogeneous Integration of SiPh 800G / 1,6T DR-8 transceivers

High Level Scetch



Cooperation model

AT&S

Providing & development of IC Substrate & embedding SiPh
Apply reliability tests on functional demonstrator



Define design & specifications for CPO NiC / Switch
Functional testing of fully assembled Demonstrator

imec
embracing a better life

Providing SiPh components & development



Providing & development of flip chip bonding process

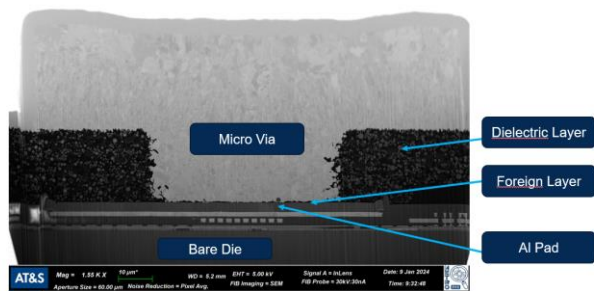


Providing Fiber connector & development

Validation of non destructive Test method

Reference Metrology – destructive Test method

2D Analysis via FIB



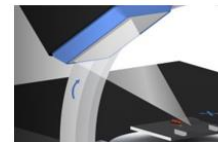
FIB prepared by AT&S Lab

3D X-ray metrology – non destructive Test method

Development of a novel 3D inspection tool for planar samples within HiCONNECTS project

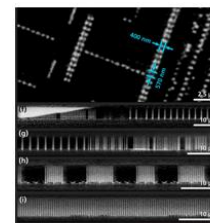
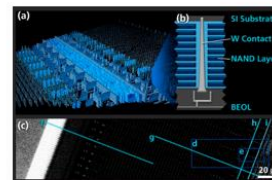
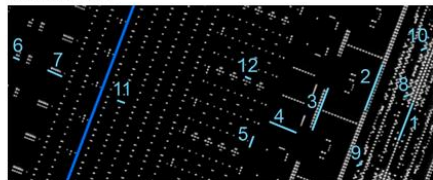
Key features:

- 3D inspection of large size planar samples
- non-destructive
- Sub-300nm resolution



Example:

Micro SD card - from 2D → to 3D, individual contacts with an expected size of 100-200nm can be clearly identified



D. Müller, at al" Crystals, vol. 11, no. 6, p. 677, 2021, doi: 10.3390/cryst11060677.

excillum

X HUBER
Diffraction and Positioning Equipment

Conclusion

- Better signal integrity need Miniaturization & Modularization
- Miniaturization drives High End PCB's and IC Substrate Technologies
- Modularization drives Heterogeneous Integration Concepts
- Higher data rates drives Optics elements

Acknowledgement

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