



Jumping the Barriers of Future Lithography

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From chips everywhere to artificial intelligence everywhere

Gen AI opens endless opportunities, expected to generate >6T\$ value by 2030 across several industries



Connected world



Climate change and
resource scarcity



Social and
economic shifts



Hyperconnectivity



Cloud
infrastructure



Energy
transition



Electrification,
smart mobility



Working,
learning remotely



Healthcare,
medical tech



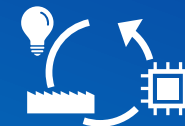
Edge
computing



Agricultural
innovation



Smarter use of
limited resources



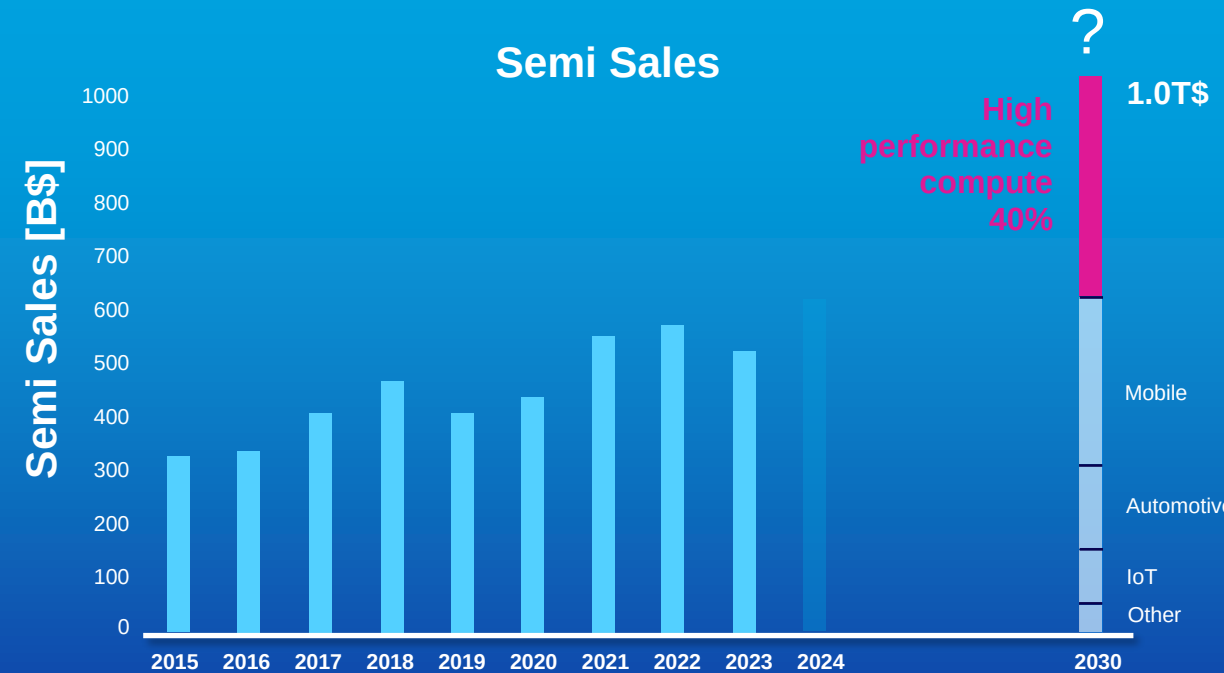
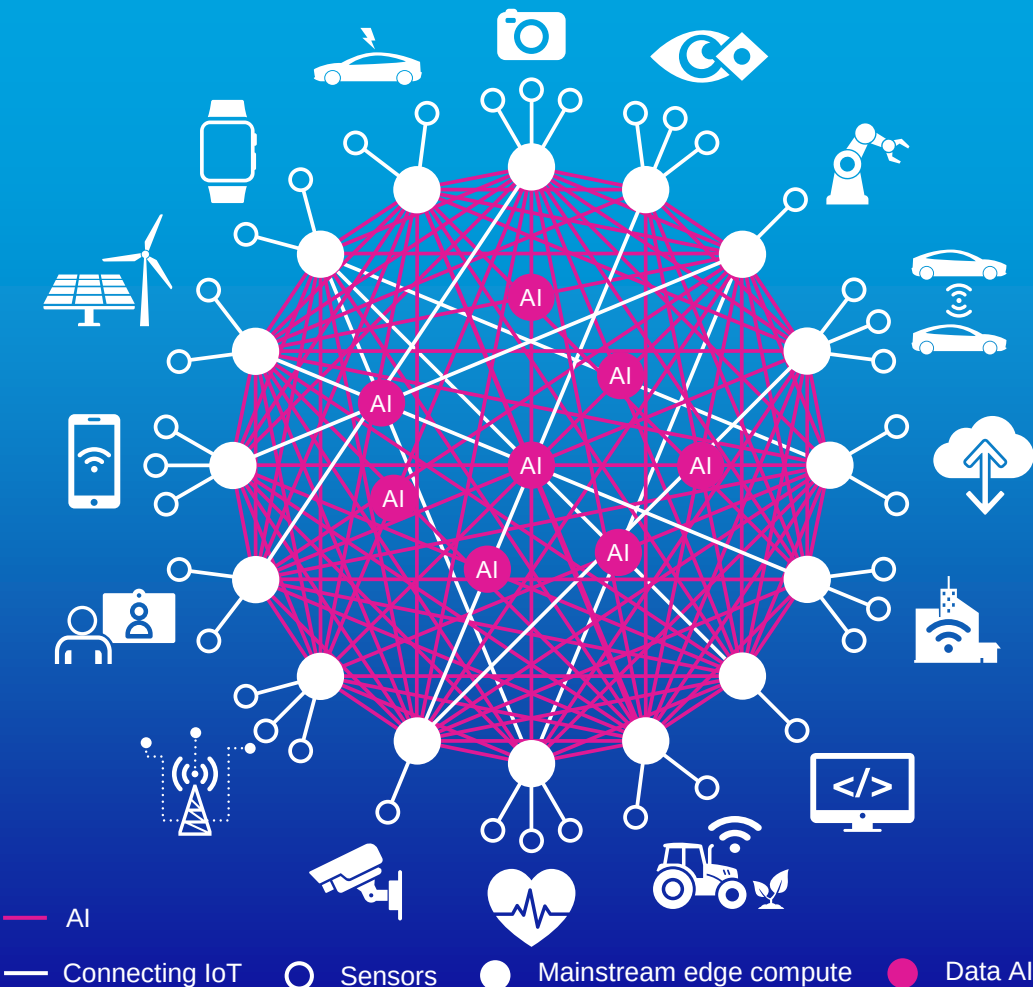
Technological
sovereignty



Automation

From chips everywhere to artificial intelligence everywhere

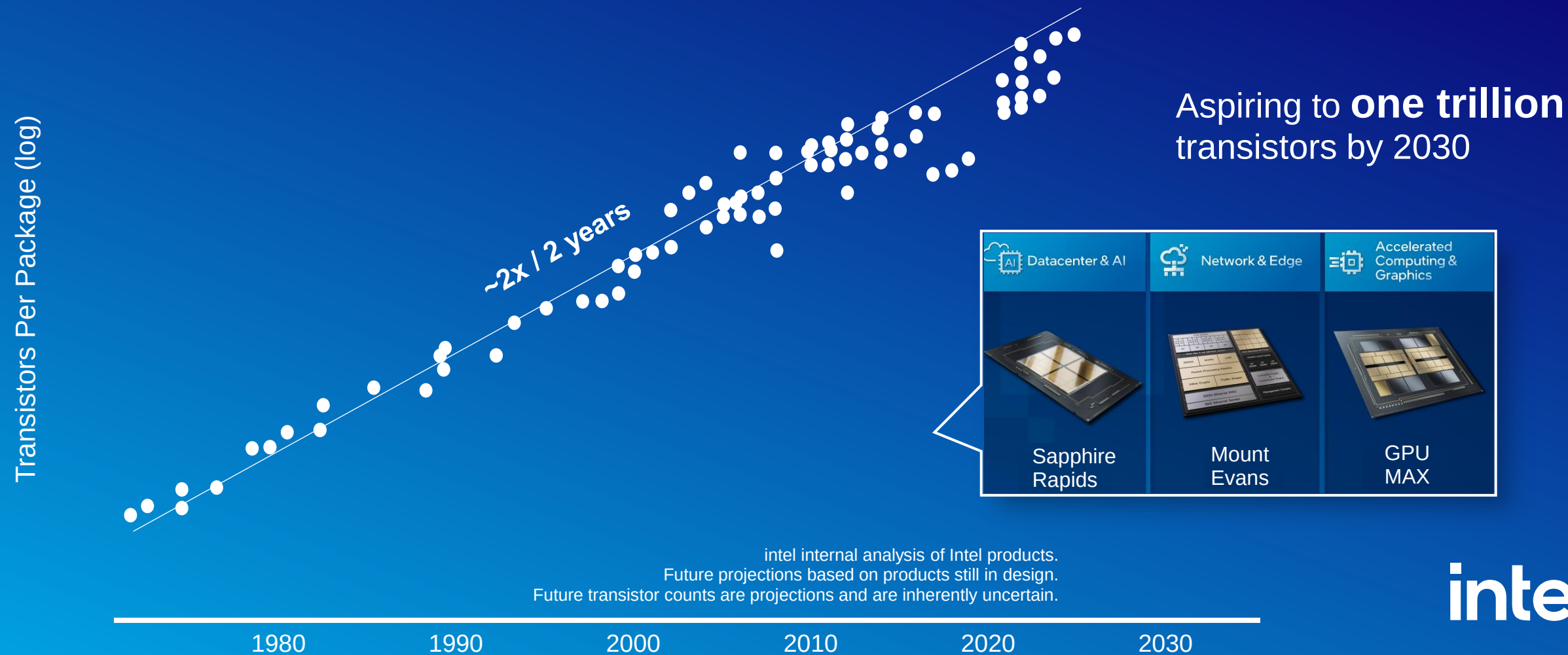
Gen AI opens endless opportunities, expected to generate >6T\$ value by 2030 across several industries



Global data center and edge AI demands are expected to grow significantly year on year to represent >40% of SEMI demand in 2030 and generate some upside for our industry

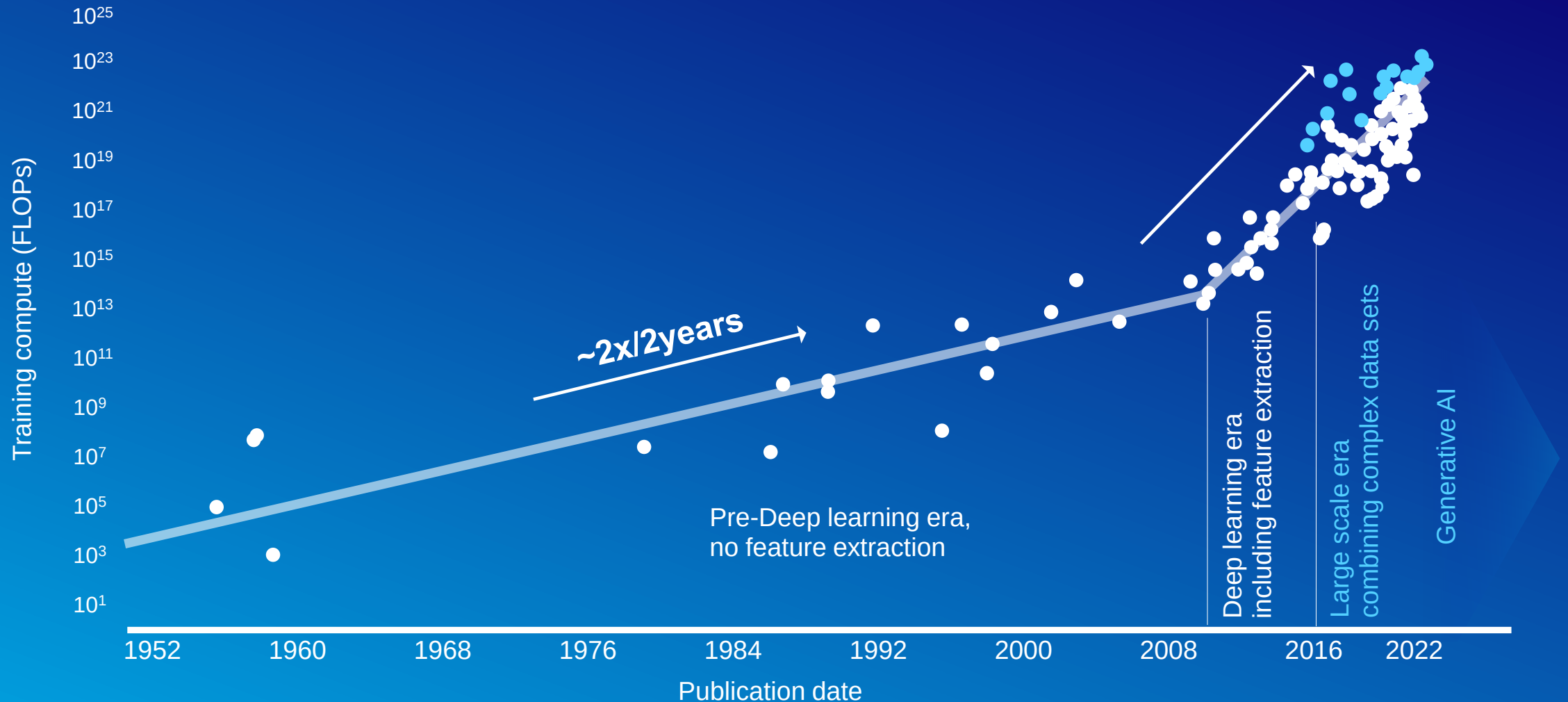
Moore's law for computing power

Transistors per package continue to double every two years enabling one trillion by 2030



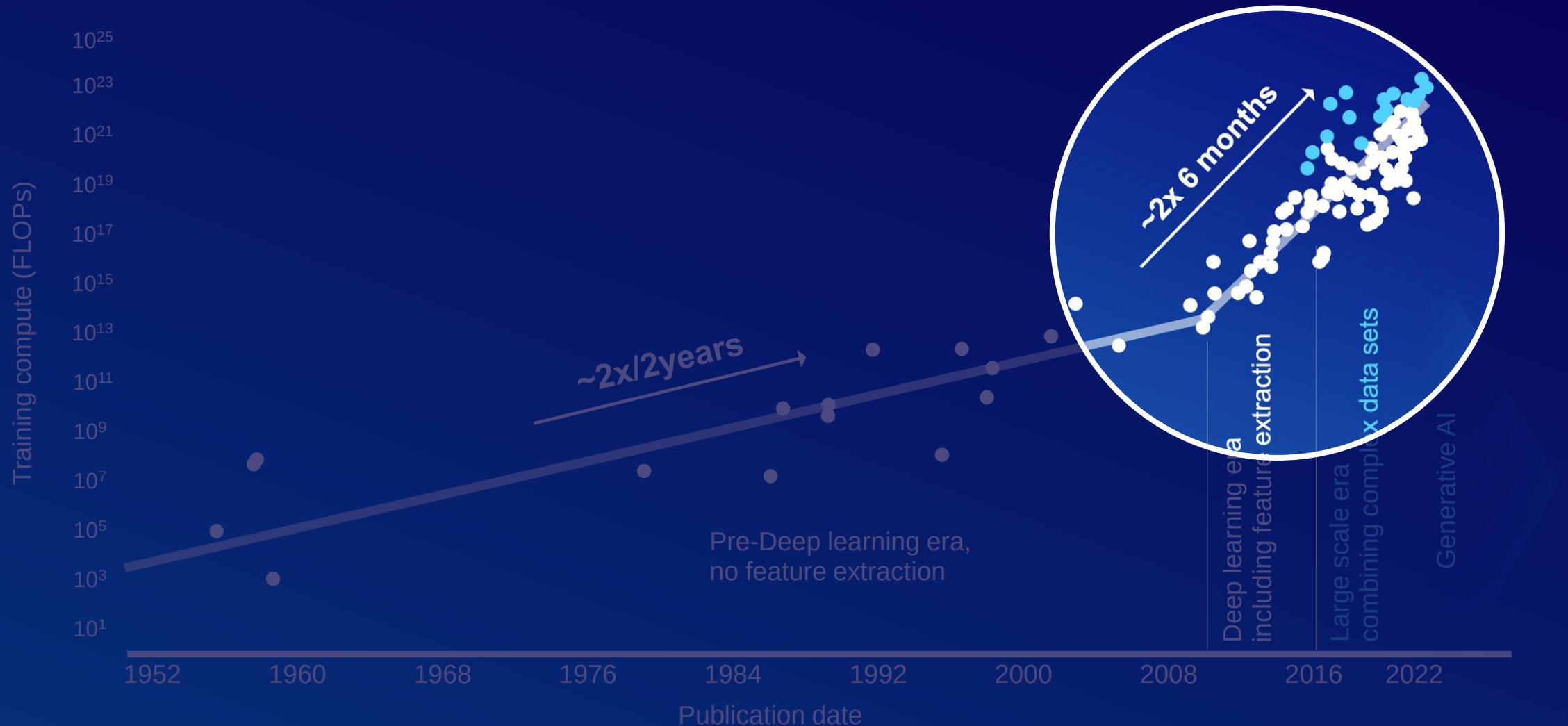
Generative AI, high-performance computing power outpaces Moore's law

In 2030, >50% of data center demand could be driven by AI, representing >90% of Gen AI FLOPs



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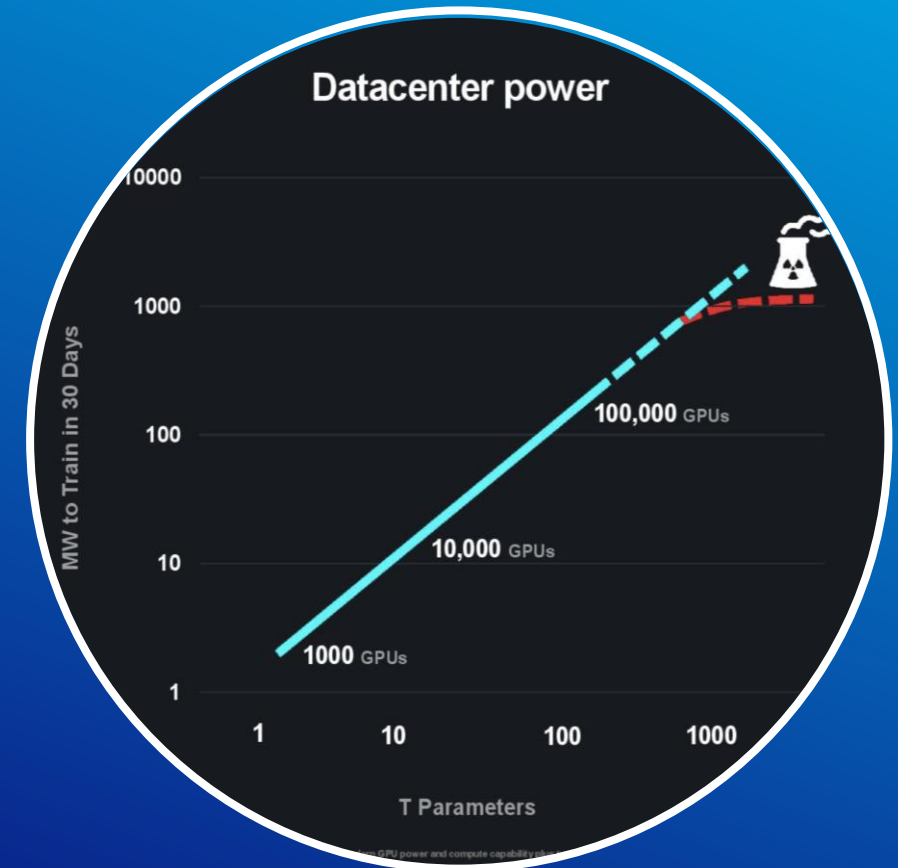
HPC can be achieved but at the expense of energy consumption

Energy consumption



Aurora supercomputer (HPC and AI applications)
delivers **2,000,000,000,000,000,000 FLOPs**

using **60MW** and **34000 gallons of water per minute** for cooling



Scalability of HPC is endless, but cost and energy challenges must be solved

AI computing architecture¹



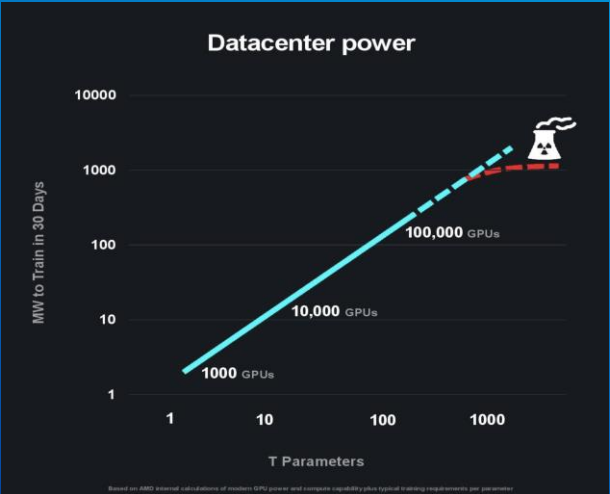
Source: Luc van den Hove, IMEC, ITF May 21, 2024



AI architecture cost²



AI energy consumption³



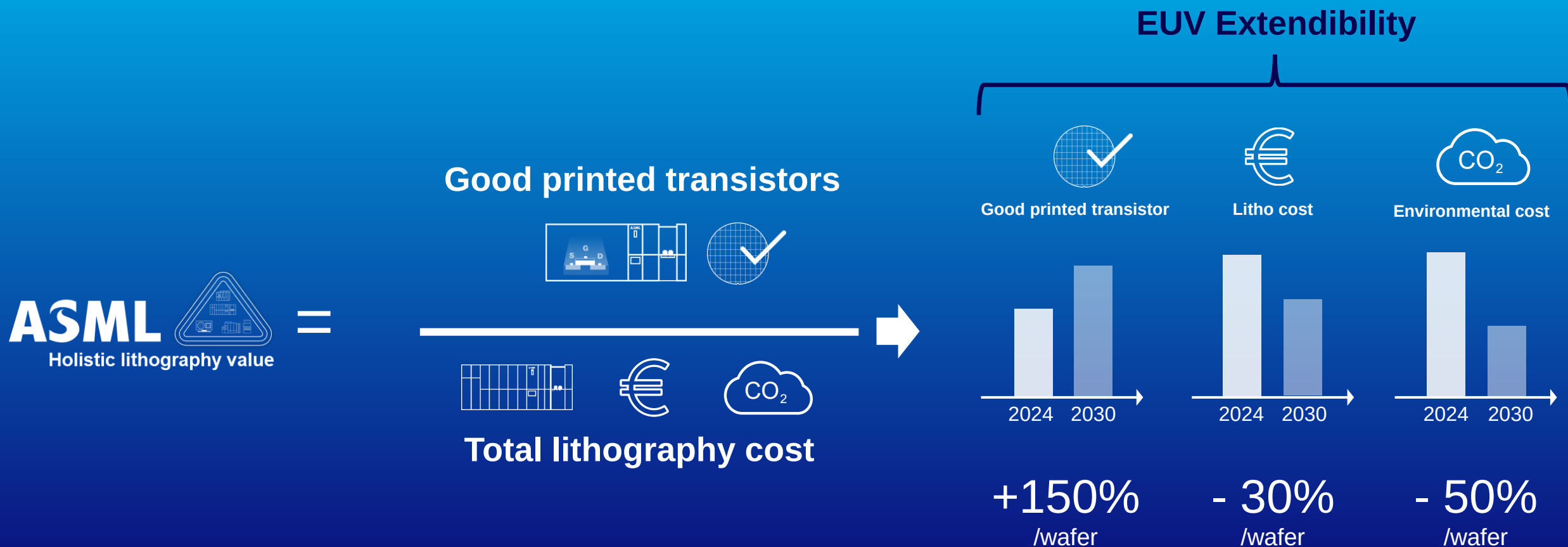
Source: Lisa Su, AMD, ITF May 21, 2024



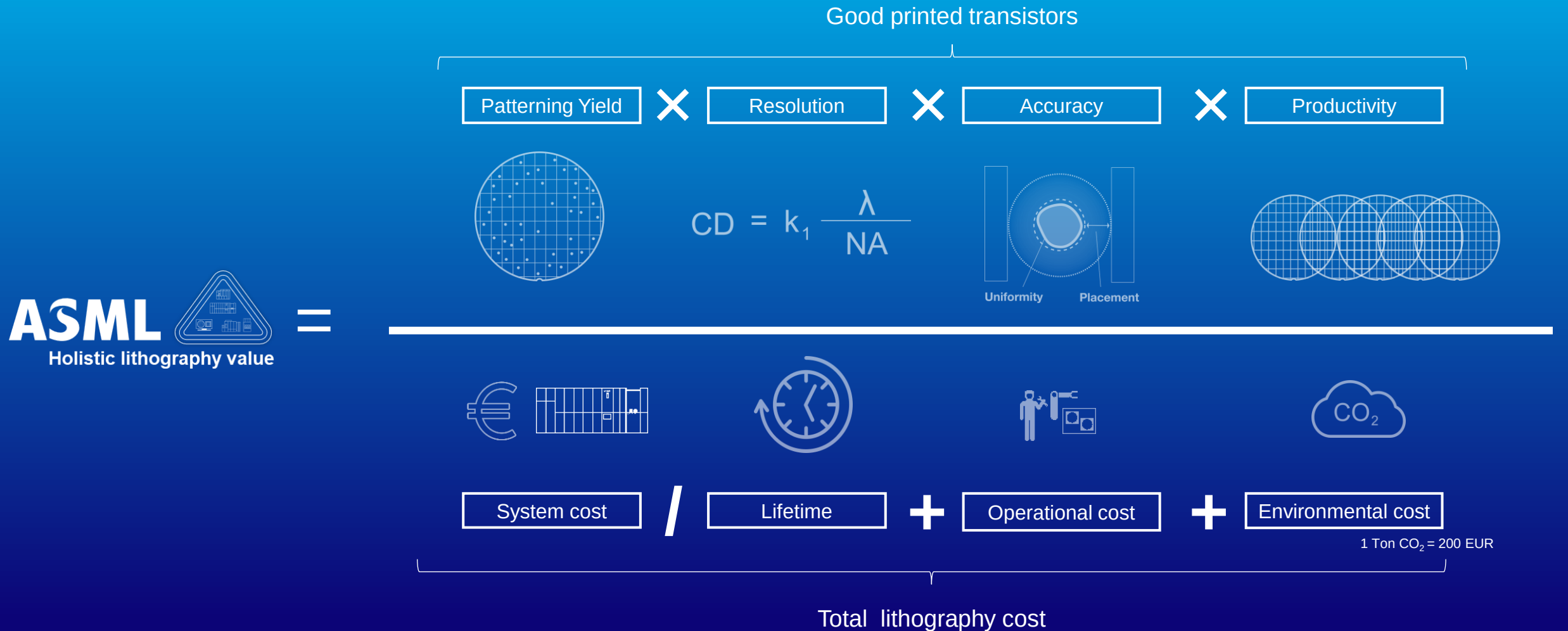
The semiconductor industry needs to deliver the highest computing power / transistor density at the lowest cost, including the lowest possible CO₂ emission

ASML roadmap drives higher transistor density at lower cost and environmental impact

EUV extendibility provides a path towards >3.5x transistor print cost reduction by 2030

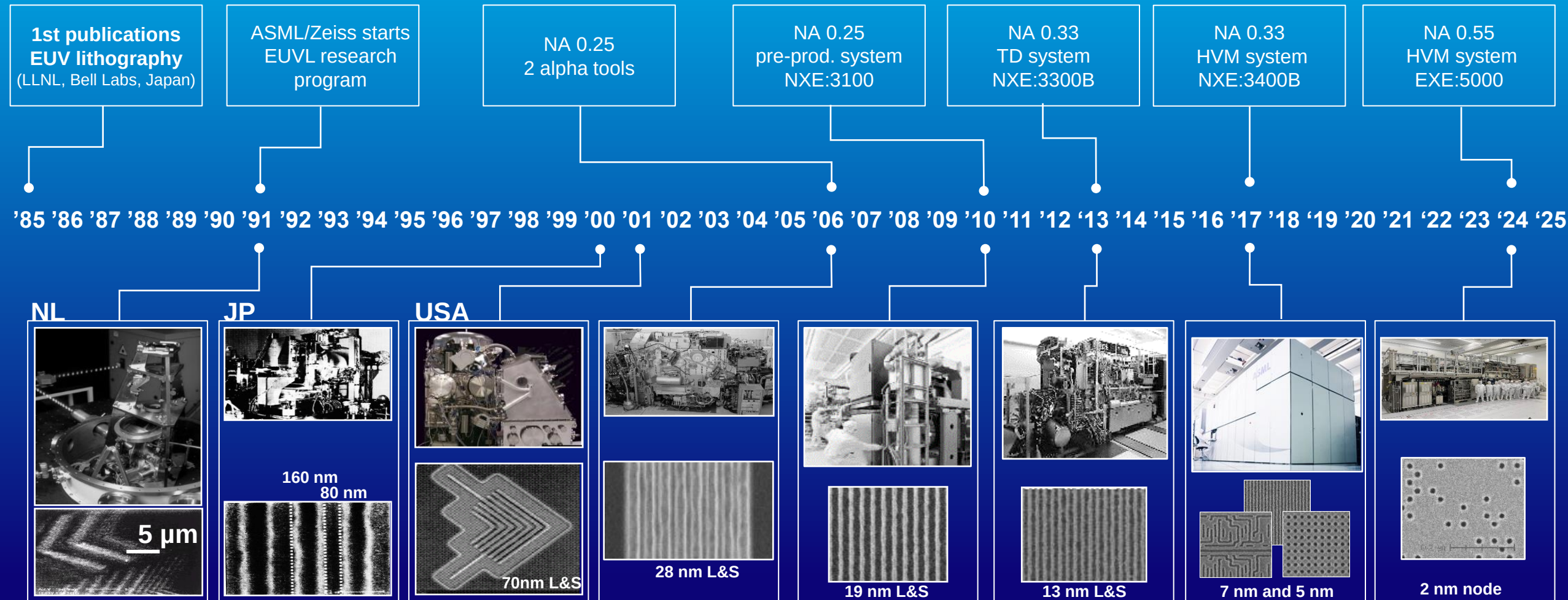


All critical contributors will be improved to achieve higher transistor density at lower cost and environmental impact

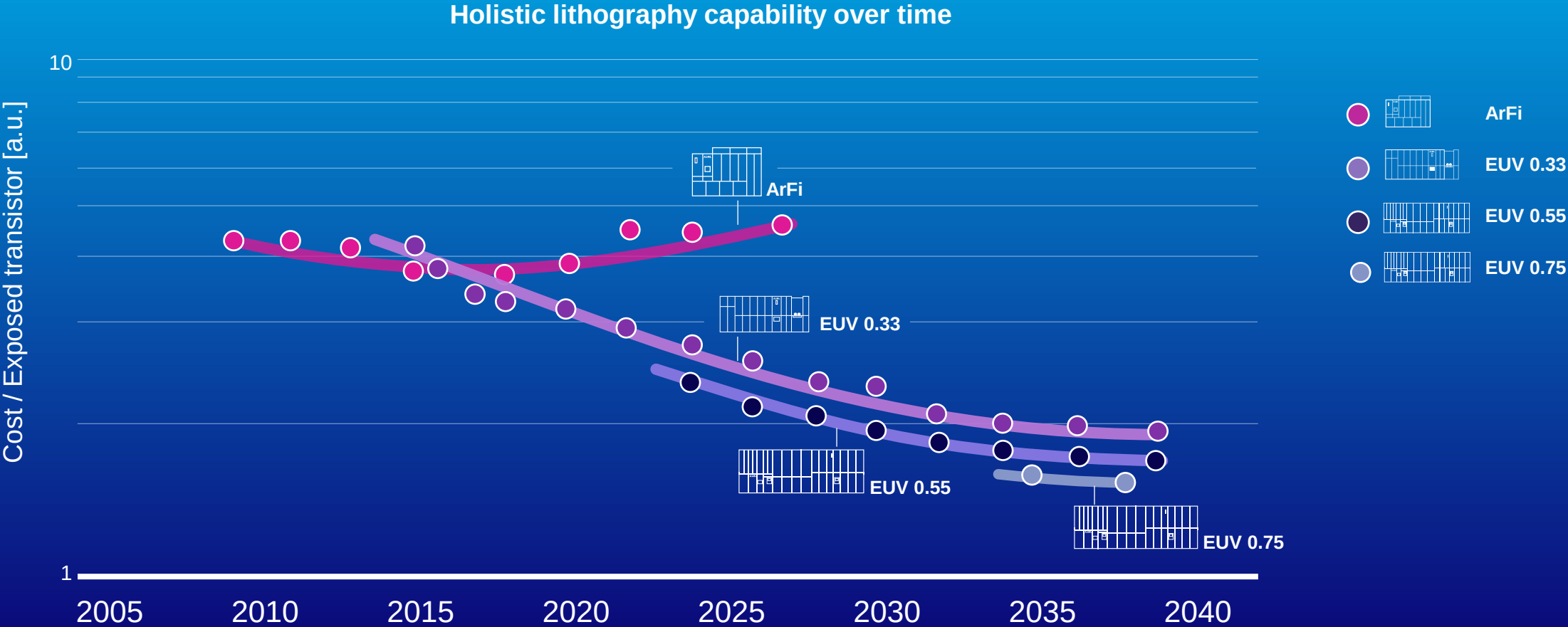


EUV development has progressed over approximately 30 years

Our learning now enables us to extend EUV technology well into the next decade



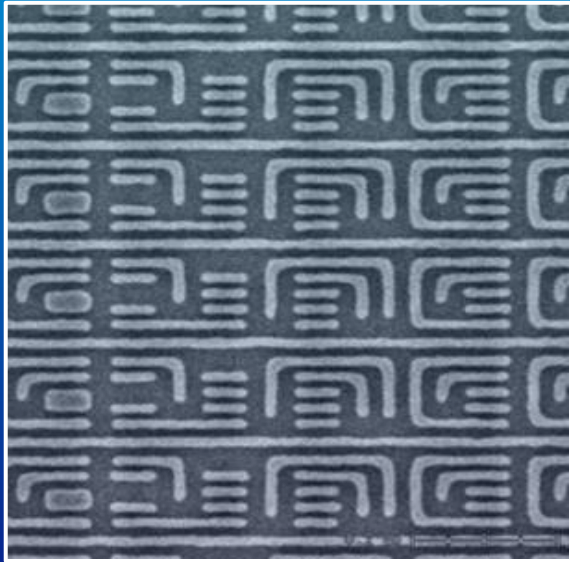
ASML roadmap continues to deliver higher transistor density at lower cost



LOGIC: High NA enables more design freedom for 2D designs

Applicable to 2D metal interconnects, as well as multi-pitch/multi-CD lines and contacts

Low NA Multi Patterning



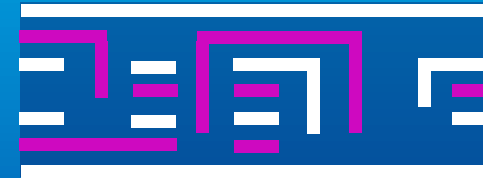
P22 in horizontal direction combined with P28 in vertical direction.

High NA Single Patterning

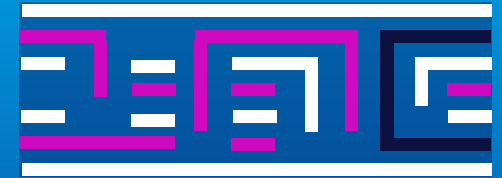
Exposure NXE ①



Exposure NXE ②

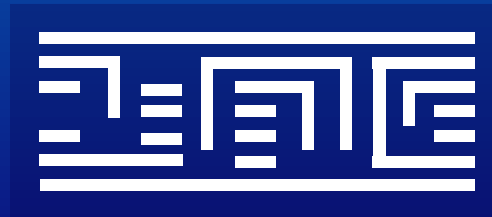


Exposure NXE ③



This multi-exposure method is not performed in high-volume manufacturing due to its complexity.

① Exposure High NA

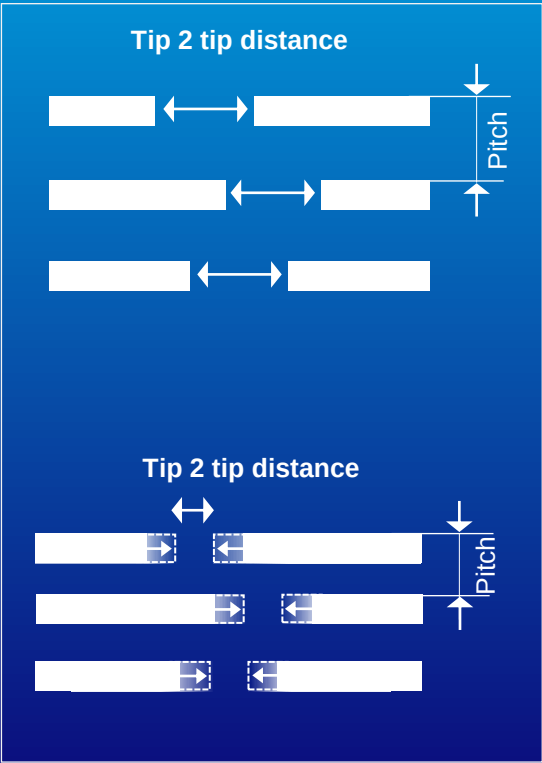


High NA Logic metal: ~35% cost benefit and process simplification

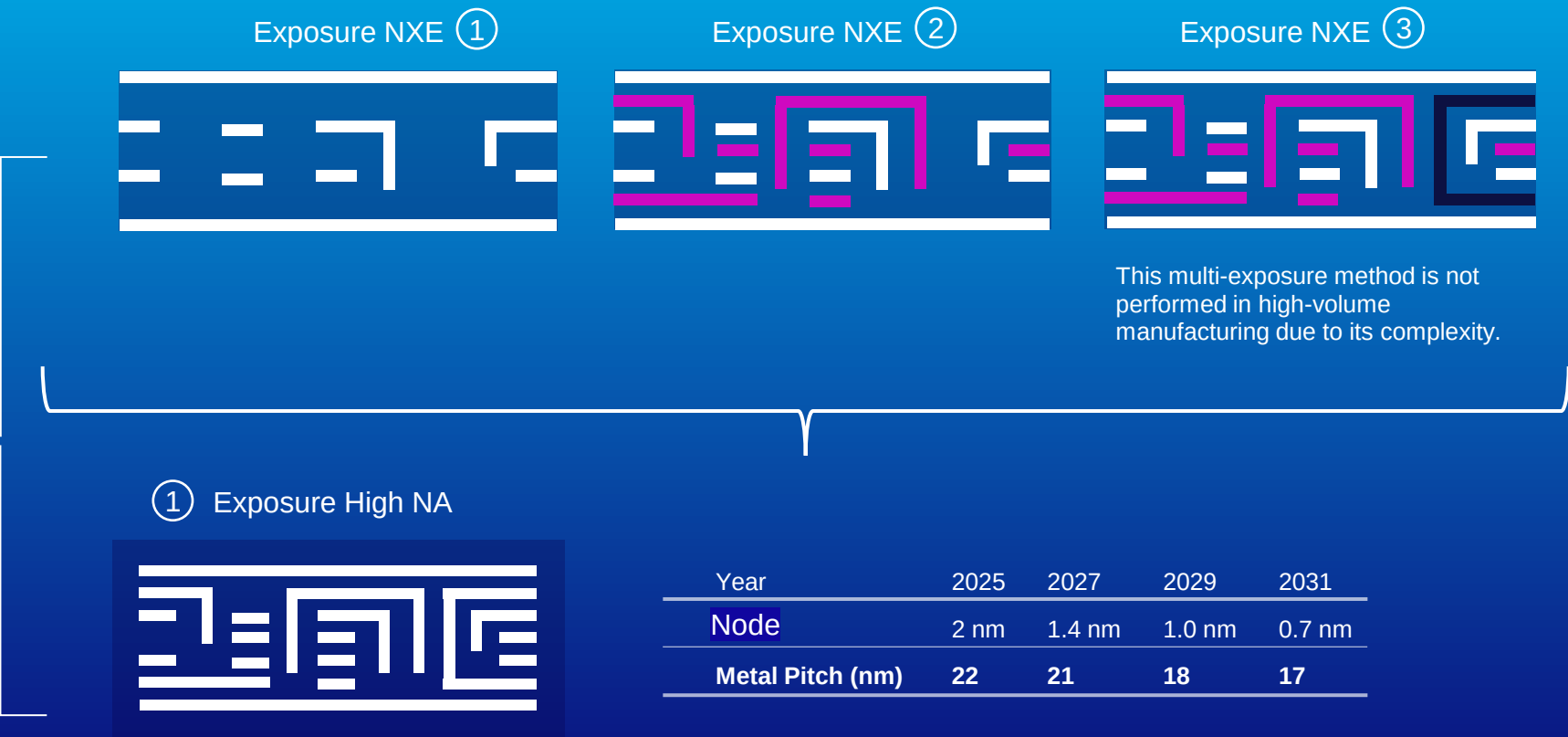
LOGIC: High NA enables more design freedom with 1.5D and 2D designs

Support tip to tip distance requirement all the way to 17nm pitch @ A7 node

Low NA Multi Patterning



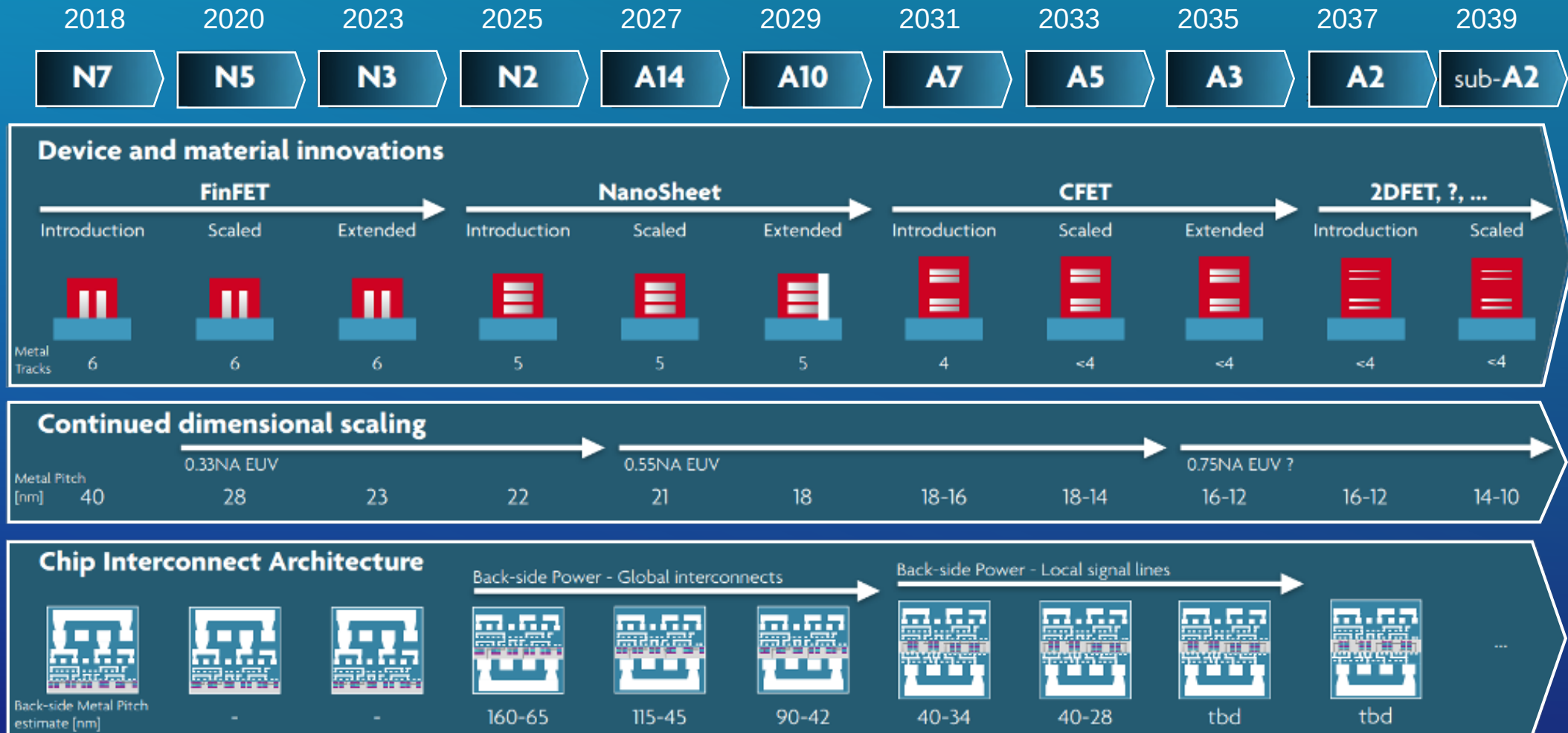
High NA Single Patterning



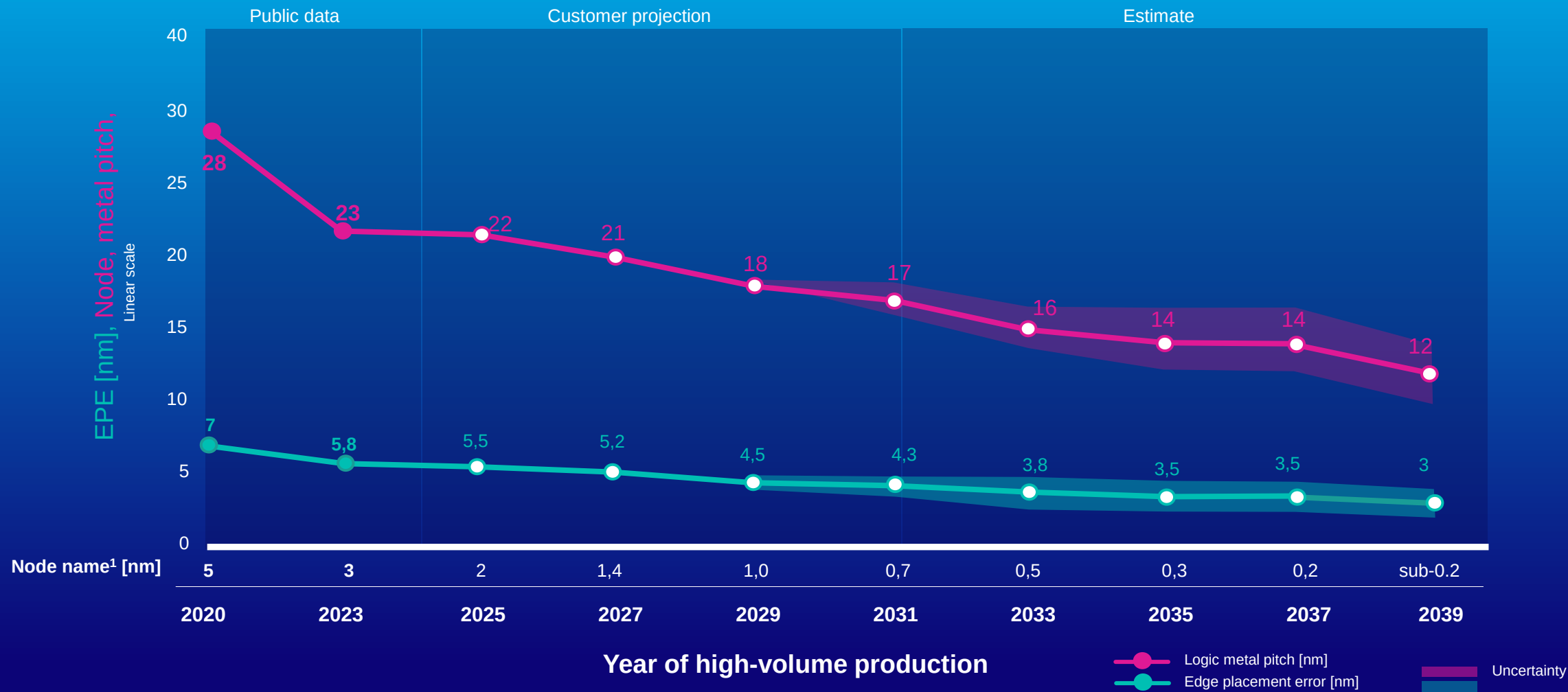
High NA Logic metal: 2x improvement in tip to tip control

The logic device roadmap will drive density using 2D shrink and 3D integration

Future innovations are paving the way for the next 15 years

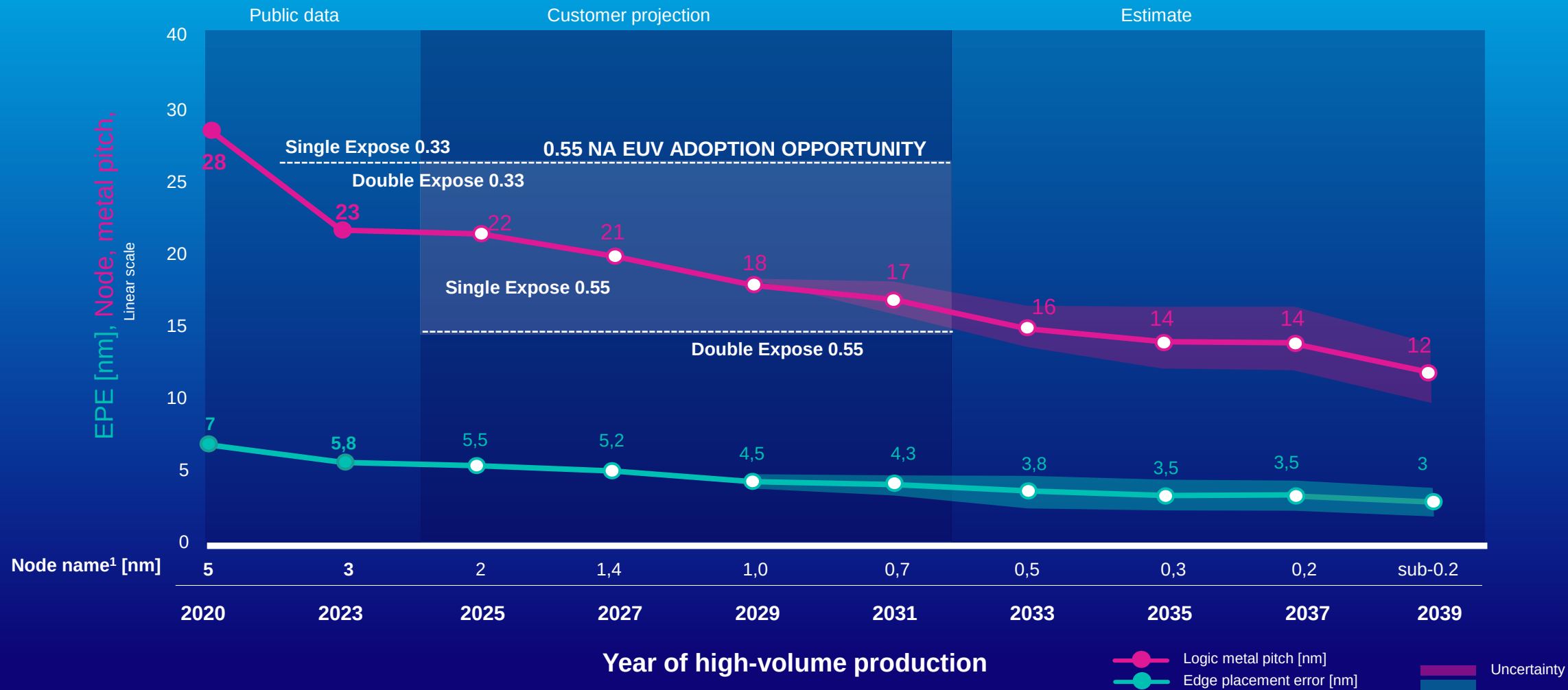


Semiconductor manufacturers continue to drive transistor shrink through better lithography resolution and accuracy

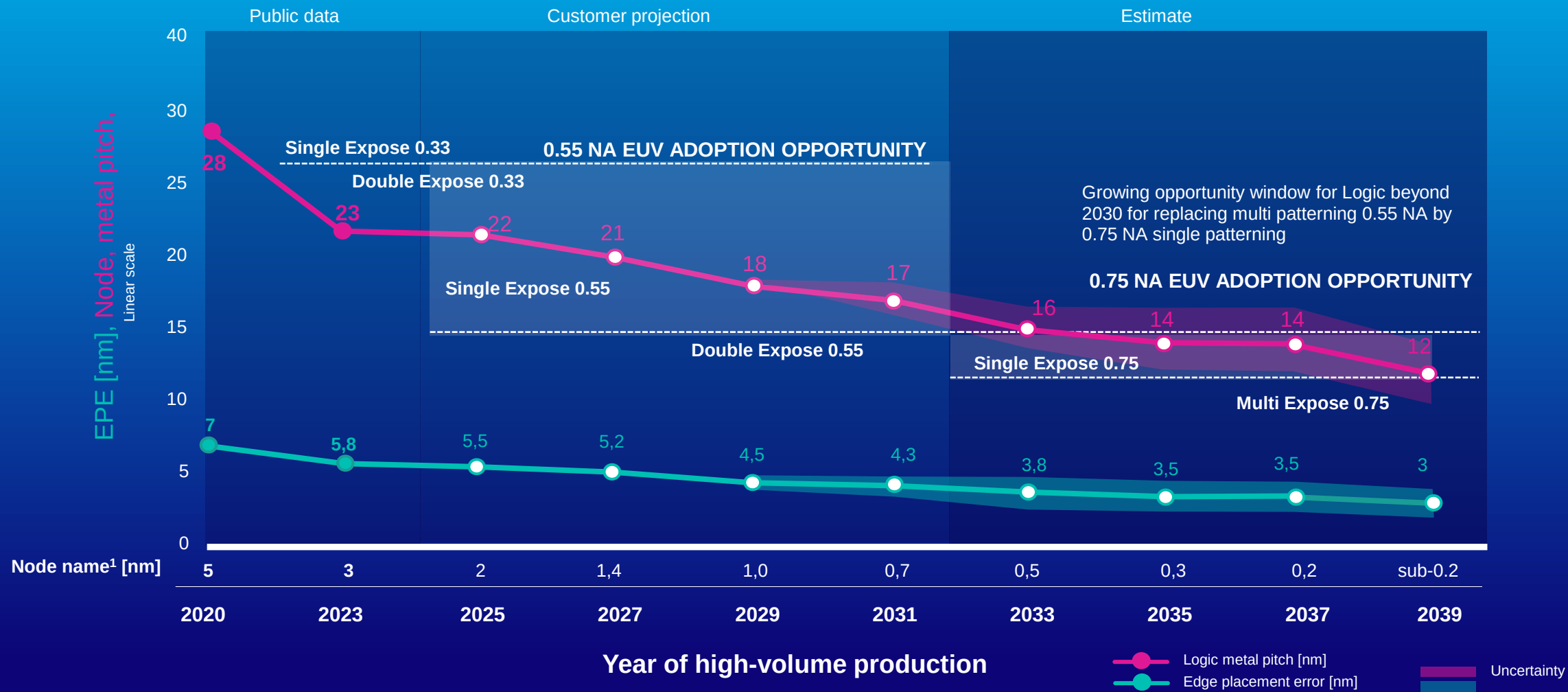


High NA EUV opportunity starting now

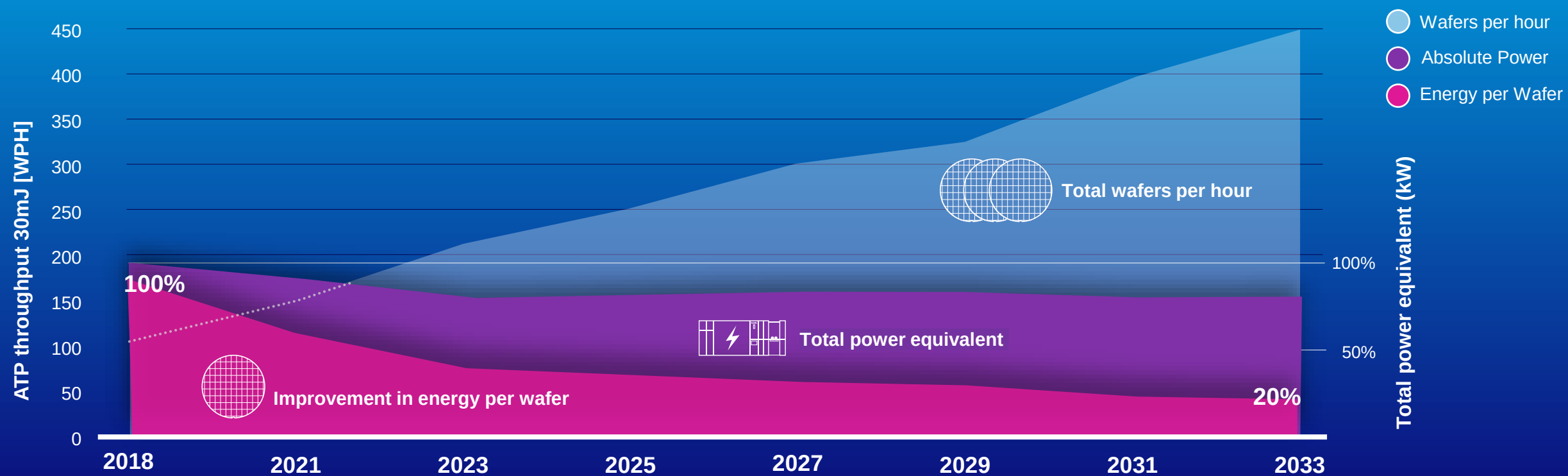
0.33 NA EUV transitions to multi-patterning on <26nm pitch critical layers



Hyper NA opportunity to start next decade when shrink requires <16nm pitch



High transmission optics combined with higher source efficiency will continue to reduce the energy per wafer



EUV source power continues to scale with opportunity to achieve >1000W

740W EUV power demonstrated - improvements identified to reach 1000W

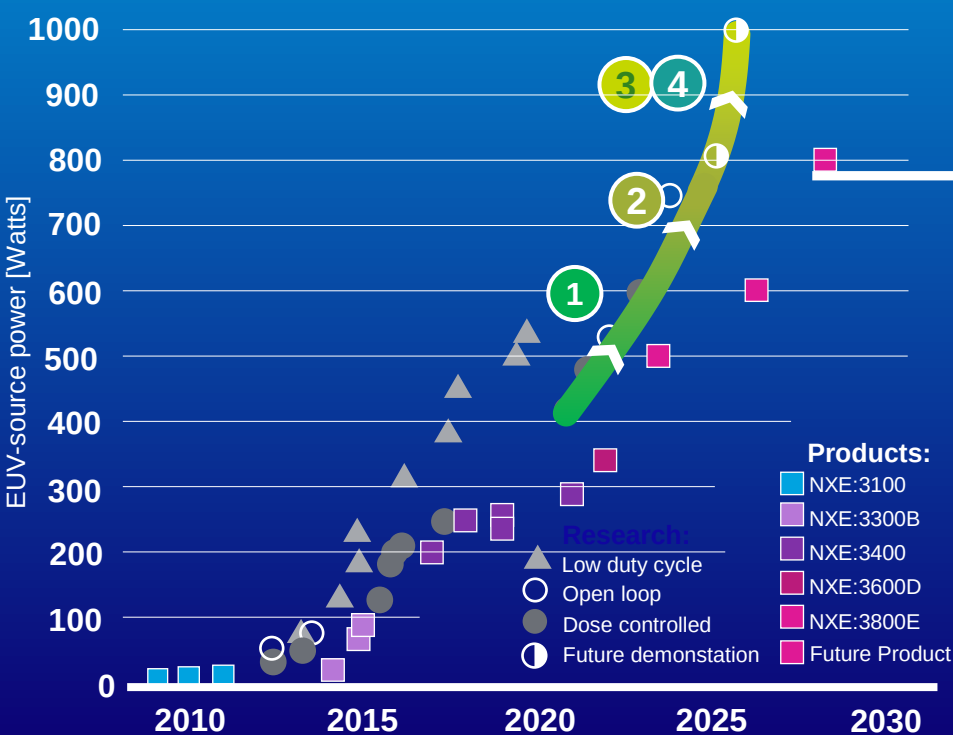
1 1 μ m architecture

2 Droplet Repetition Rate

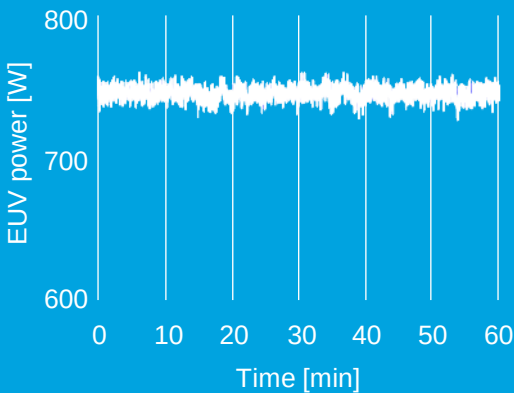
3 CO₂ Drive Laser Power Scaling

4 High-pressure droplet generation

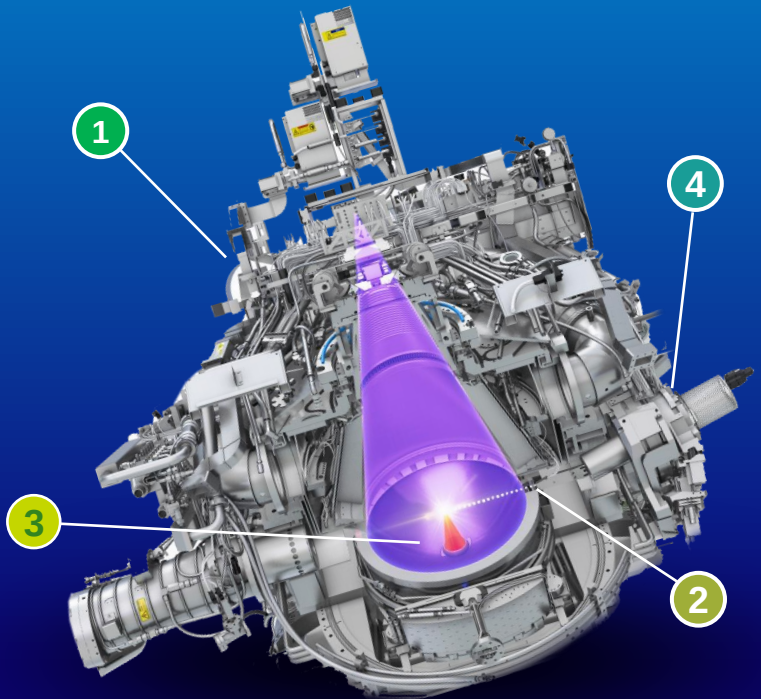
EUV source power scaling

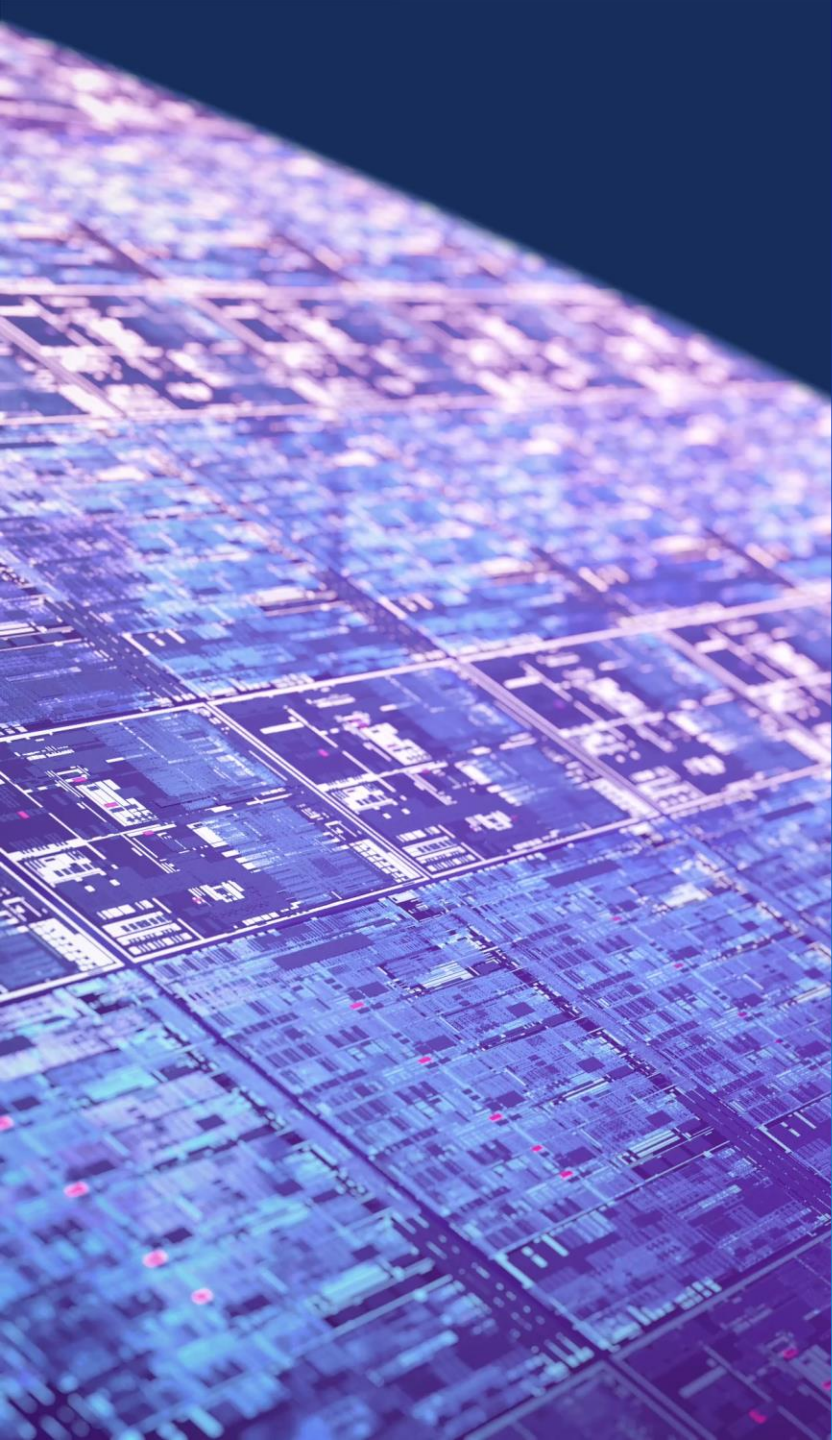


First 100kHz results:
740 W EUV
(open energy control loop)



- 1 μ m architecture
- 700 bar Droplet Generator





Summary

- Endless market pull for semiconductor innovation continues to be strong through applications, data and algorithms
- EUV Lithography has taken its place as the primary enabler of the IC roadmap
- The extension of IC device scaling beyond this decade is enabled by the introduction of high-NA EUV
- To continue to support future extensions of the device shrink roadmaps, feasibility studies have been started on even higher NA beyond 0.55
- The ASML roadmap reduces cost/energy per transistor, but more importantly, reduces cost/energy of device operation, to support the ever-growing needs of hyperconnectivity and AI

An aerial, high-angle photograph of a city's street grid at night. The image is heavily stylized with a color gradient, transitioning from a deep blue in the upper right to a vibrant purple in the lower left. The city lights are visible as a dense pattern of small, bright points, with some larger, more distinct lights that could be buildings or intersections. The perspective is looking down at an angle, creating a sense of depth and scale.

**THANK
YOU**