



SOI & ADVANCED SUBSTRATES NEWS
ACCELERATING INDUSTRY GROWTH | Bi-Weekly Newsletter

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16-CHANNEL PHOTONIC SOLVER
FOR OPTIMIZATION PROBLEMS ON A
SILICON CHIP

A programmable photonic solver for quadratic unconstrained binary optimization problems is demonstrated with a hybrid optoelectronic scheme, which consists of a photonic chip and an electronic driving board. The photonic chip is fabricated on the silicon on insulator (SOI) substrate and integrates 16 high-speed electro-optic modulators, 88 thermo-optic phase shifters, and 16 balanced photodetectors.

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SILICON-ON-INSULATOR
WAVELENGTH-SELECTIVE FILTER
WITH INTEGRATED DETECTORS AT
THE 2 MM WAVE BAND

Integrating active and passive photonic components is essential to achieve compact optical solutions. This paper reports for the first time a wavelength-selective detection system based on the heterogeneous integration of two grating-coupled InGaAs photodetectors operating at the 2µm wave band, with a wavelength selectivity provided by a dual-channel Mach–Zehnder interferometer fabricated using a silicon-on-insulator (SOI) wafer.

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OBSERVATION OF ROOM
TEMPERATURE GATE TUNABLE
QUANTUM CONFINEMENT EFFECT IN
PHOTODOPED JUNCTIONLESS
MOSFET

In pursuing room temperature quantum hardware, this study introduces the effect of tunable photodoping in gate-bias assisted quantum wire within a tri-gated architecture of n-type junctionless MOSFET. To fabricate tri-gated silicon nanowire-based junctionless MOSFET, researchers used silicon-on-insulator (SOI) wafers with a few high-quality nanometers of top silicon.

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NEXPERIA'S NEW 120 V/4 A HALF-
BRIDGE GATE DRIVER RAISES
ROBUSTNESS AND EFFICIENCY IN
AUTOMOTIVE APPLICATIONS

Nexperia introduced a new series of high-performance gate driver ICs designed for driving both high-side and low-side N-channel MOSFETs in a synchronous buck or half-bridge configuration. These ICs are fabricated using a silicon-on-insulator (SOI) process to achieve superior robustness in power conversion and motor driving applications.

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SOI ECOSYSTEM NEWS

ESMC'S 300-MM WAFER FAB: A BID
TO EU'S SEMICONDUCTOR
SOVEREIGNTY

ESMC, a joint venture among TSMC, Robert Bosch, Infineon Technologies and NXP Semiconductors, recently broke ground on its first semiconductor fab in Dresden, Germany. The 300-mm fab, which will provide semiconductor manufacturing services and act as a foundry, will meet the needs of the high-growth automotive and industrial sectors.

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X-FAB AND SMART PHOTONICS
COLLABORATE TO ENABLE MULTI-
TERABIT TRANSCEIVERS WITH
SILICON PHOTONICS AND INP
INTEGRATION

This collaboration builds upon the PhotonixFAB EU funding project, which aims to provide a path to scalable high-volume manufacturing for SOI and SiN silicon photonics, MTP-ready InP chiplets and micro-transfer printing of chiplets.

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HOLE-SELECTIVE SINX AND ALOX
TUNNEL NANOLAYERS FOR
IMPROVED POLYSILICON
PASSIVATING CONTACTS

The future development of solar modules depends on a device structure that can complement the electron-selective tunnel oxide passivating contact with an equivalent hole-selective contact. In this work, researchers investigate plasma enhanced chemical vapor deposited (PECVD) SiNx and atomic layer deposited AlOx as alternative nanolayers for the passivation layer in polysilicon tunnel contacts.

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TOWARD CRACK-FREE ALN
GROWTH ON SILICON (111) BY
INTRODUCING BORON
INCORPORATED BUFFER LAYER VIA
MOCVD

High-quality aluminum nitride (AlN) films on silicon substrates are crucial for various applications. Nonetheless, producing high-quality and crack-free AlN on silicon presents significant challenges due to the stress caused by lattice and thermal expansion mismatches. In this study, researchers report on the ability of boron added to AlN to allow the growth of thicker AlN layers on silicon without cracking.

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COMPOUND SEMICONDUCTOR

US DOE ANNOUNCES \$481.5M LOAN
TO SK SILTRON CCS

As part of the Biden-Harris Administration's Investing in America agenda, the Department of Energy (DOE) has announced a \$544 million loan to SK Siltron CCS, LLC to expand American manufacturing of high-quality SiC wafers for electric vehicle (EV) power electronics.

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SCALED VERTICAL-NANOWIRE
HETEROJUNCTION TUNNELLING
TRANSISTORS WITH EXTREME
QUANTUM CONFINEMENT

Silicon transistors are held back by a physical limit that prevents transistors from operating below a certain voltage. To overcome this limit, MIT researchers have made a novel 3D transistor from ultra thin compound semiconductors. The team's scaled vertical-nanowire heterojunction tunnelling transistors are based on the broken-band GaSb/InAs system.

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ENHANCING AND MAPPING
THERMAL BOUNDARY
CONDUCTANCE ACROSS BONDED
SI-SIC INTERFACE

A 4-inch Si-on-4H–SiC bonded wafer was fabricated using the surface-activation bonding (SAB) technique. This work proposes a promising candidate for thermal management materials and provides an advanced methodology for investigating thermal-boundary conductance distribution.

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POLYCRYSTALLINE DIAMOND FILM
GROWTH ON GALLIUM NITRIDE WITH
LOW BOUNDARY THERMAL
RESISTANCE

As the demand for high-frequency and high-power electronic devices has increased, gallium nitride (GaN), particularly in the context of high-electron mobility transistors, has attracted considerable attention. This paper proposes a novel method for directly depositing diamond films onto N-polar GaN epitaxial layers.

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SEMI BLOG

HOW AI-DRIVEN 3D X-RAY
INSPECTION SUPPORTS A
SUSTAINABLE INSPECTION
STRATEGY FOR AI CHIPS

Ensuring both precision and efficiency in manufacturing has become an increasing challenge in today's rapidly evolving semiconductor industry, particularly as advanced technologies like MEMS and AI chips push the boundaries of design and production. The introduction of AI-driven 3D X-ray inspection technologies is transforming the landscape, offering manufacturers a sophisticated tool to ensure quality control, while driving sustainable production strategies.

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SEMI NEWS HIGHLIGHT

WORLDWIDE SILICON WAFER
SHIPMENTS INCREASE 6% IN Q3
2024, SEMI REPORTS

Worldwide silicon wafer shipments increased 5.9% quarter-over-quarter to 3,214 million square inches (MSI) in the third quarter of 2024 and registered 6.8% growth from the 3,010 million square inches recorded during the same quarter last year, the SEMI Silicon Manufacturers Group (SMG) reported in its quarterly analysis of the silicon wafer industry.

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