



**SOI & ADVANCED SUBSTRATES NEWS**  
ACCELERATING INDUSTRY GROWTH | Bi-Weekly Newsletter

Share 

**SEMI COMPOUND SEMICONDUCTORS UPDATE**

The SEMI Standards Compound Semiconductor Materials (CSM) Technical Committee has initiated new standards development activities across its 13 Task Forces. These activities aim to address key industry challenges and establish comprehensive standards for the compound semiconductor sector. Among the Task Forces, these are currently working on new standards listed below:

- GaN Task Force
- Silicon Carbide Substrate Task Force
- SiC Epi Defects Task Force
- Silicon Carbide Engineered Substrate Task Force

Download a [comprehensive list](#) of the current Compound Semiconductor Materials standards activities.

Join the [SEMI International Standards Program](#) or contact your [local SEMI Standards staff](#).

**FEATURED IN THIS EDITION**

**PASSIVE MATRIX SCHOTTKY BARRIER 2D PHOTODIODE ARRAY ON GRAPHENE/SOI PLATFORM**

Research found that high resolution image sensing or multiple pixel optical detection applications can be realized by increasing the density of the G/n-Si pixels with homogeneous active junction area on a graphene/ silicon-on-insulator (SOI) platform.

[Read More](#)

**AN EFFICIENT AND COMPACT MID-INFRARED POLARIZATION SPLITTER AND ROTATOR BASED ON A BIFURCATED TAPERED-BENT WAVEGUIDE**

This work presents predictive simulations for a novel mid-infrared (MIR) polarization splitter and rotator (PSR) design, which operates in the 3.1–3.6µm range. This is the first report of a MIR PSR in this range on a silicon-on-insulator (SOI) platform.

[Read More](#)

**APERIODIC OPTICAL PHASED ARRAY WITH WIDE FIELD OF VIEW AND HIGH SIDELobe SUPPRESSION RATIO BASED ON SIN-ON-SOI PLATFORM**

Optical phased array (OPA) has the advantages of fast scanning speed, high reliability, and the ability to achieve all-solid-state scanning and scanning at any position, making it a promising solution for all-solid-state LiDAR. In this paper, a 128-channel aperiodic OPA based on standard SiN-on-SOI integrated process platform is presented.

[Read More](#)

**ULTRA-LOW-LOSS POLARIZATION-SPLITTING GRATING COUPLER BASED ON INVERSE-DESIGN**

A high-performance polarization-splitting grating coupler (PSGC) designed by an inverse design method is proposed. Experimental results indicate a peak insertion loss (IL) of -1.05 dB and a polarization-dependent loss (PDL) of 0.04 dB at 1534.7 nm, which are believed to be the lowest on current 220nm-silicon on insulator (SOI) platforms.

[Read More](#)

**SOI ECOSYSTEM NEWS**

**INFINEON REACHES NEXT MILESTONE ON 200 MM SILICON CARBIDE (SiC) ROADMAP**

The products provide first-class SiC power technology for high-voltage applications, including renewable energies, trains, and electric vehicles. Additionally, the transition of Infineon's manufacturing site in Kulim, Malaysia, from 150-millimeter wafers to the larger and more efficient 200-millimeter diameter wafers is fully on track.

[Read More](#)

**FAMES DETAILS FD-SOI PILOT LINE COMMERCIAL PARTNERS**

The pilot line is developing 10nm and 7nm FD-SOI process technology for applications with a range of embedded non-volatile memories, radio frequency, 3D integration and power management integrated circuits. There is commercial support from 44 companies.

[Read More](#)

**INDIUM PHOSPHIDE SEMICONDUCTOR TECHNOLOGY FOR NEXT-GENERATION COMMUNICATION SYSTEMS: SUSTAINABILITY AND MATERIAL CONSIDERATIONS**

Indium phosphide (InP) semiconductor technology is being explored for RF applications, targeting frequencies exceeding 100 GHz, to support the next generation of 6G communication systems. In this study, researchers evaluate the environmental impacts of manufacturing InP wafers based on industrial data and those of InP-based heterojunction bipolar transistors based on early-stage research data.

[Read More](#)

**A WAFER-LEVEL FABRICATED HEATING-VACUUM MICRO-PLATFORM WITH RESONANT MEMS MONOLITHICALLY INTEGRATED**

A novel wafer-level fabricated heating-vacuum micro-platform with a monolithically integrated resonant MEMS is introduced. Building upon the traditional three-layer wafer-bonding vacuum packaging process, the wafer-level integration of a thermistor, a heater, an isolation structure, and a MEMS resonator is achieved by adding only a mask and an additional silicon wafer, combined with deep silicon-etched embedded structures and a clever grinding release process.

[Read More](#)

**COMPOUND SEMICONDUCTOR**

**NAVITAS' GAN AND SiC TECHNOLOGIES DRIVE POWER FOR DELL'S AI NOTEBOOK LINEUP**

By combining GaN and SiC innovations, Navitas empowers Dell to offer rapid charging with superior efficiency, minimal heat generation, the smallest form factor, and the lowest component count.

[Read More](#)

**EPC RELEASES 4TH EDITION OF 'GAN POWER DEVICES FOR HIGH-EFFICIENCY POWER CONVERSION' BOOK**

Co-authored by EPC CEO Dr. Alex Lidow and a team of GaN experts, the book remains an essential reference for engineers, students, and industry professionals seeking to stay ahead in power electronics innovation.

[Read More](#)

**INGAN LASER DIODES ON C-PLANE LATERAL OVERGROWTH MATERIAL**

Researchers from the University of California Santa Barbara (UCSB) have successfully demonstrated InGaN/GaN edge-emitting laser diodes (EELDs) on a fully coalesced epitaxial lateral overgrown film from a c-plane GaN substrate. The team used native c-plane (0001) GaN substrates with a threading dislocation density better than 5x10<sup>6</sup>/cm<sup>2</sup>, supplied by Sumitomo Chemical.

[Read More](#)

**DIELECTRIC FUNCTION AND THERMO-OPTIC COEFFICIENTS OF SILICON-DOPED GAN SUBSTRATES AT ELEVATED TEMPERATURE FROM 298 K TO 873 K IN THE UV-VIS-NIR SPECTRUM**

This study reports for the first time the dielectric function of Silicon doped GaN substrates from room temperature to 873 K over the wavelength from 250 nm to 1600 nm. It is found that the temperature dependence of both the exciton transition and the refractive index of the substrate is lower than that reported in thin films.

[Read More](#)

**SEMI BLOG**

**DEVELOPING SYSTEMS FOR HETEROGENEOUS INTEGRATION: INSIGHTS FROM HICONNECTS**

The European semiconductor ecosystem continues to evolve, driven by the ambitions outlined in the EU Chips Act. With goals to strengthen Europe's technological leadership and double its semiconductor manufacturing market share to 20% by 2030, collaboration across the value chain is imperative. Heterogeneous Integration for Connectivity and Sustainability (HICONNECTS), a Horizon Europe-funded project, exemplifies this collaborative spirit.

[Read More](#)

**SEMI NEWS HIGHLIGHT**

**STRATEGIC MATERIALS CONFERENCE 2025 TO HIGHLIGHT THE NEW ERA OF MATERIALS INNOVATION**

With advanced materials as a critical enabler of semiconductor growth applications, the Strategic Materials Conference (SMC) 2025 will gather top executives and technology leaders from the semiconductor manufacturing industry for exclusive insights into the latest advancements in materials innovation. The event will take place on June 23-25, 2025 at Hayes Mansion in San Jose, California. Registration is open.

[Read More](#)

**EVENTS**



Thank you for reading this newsletter. For feedback, please email [hhoffman@semi.org](mailto:hhoffman@semi.org).

Subscribe