



SOI & ADVANCED SUBSTRATES NEWS
ACCELERATING INDUSTRY GROWTH | Bi-Weekly Newsletter

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SPECIAL ANNOUNCEMENT

The RF Workshop 2025, sponsored by Incize, is set for April 4 in Brussels. Leading experts from across the RF value chain—substrate manufacturers, foundries, fabless companies, IDMs, research centers, and academia—will come together for a full day of cutting-edge insights, in-depth discussions, and high-level networking.

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FEATURED IN THIS EDITION

GLOBALFOUNDRIES, MIT TEAM ON PHOTONIC AI CHIPS

The initial research focus is on AI and other applications with the first projects using GF's differentiated silicon photonics technology, which monolithically integrates **RF SOI**, CMOS, and optical features on a single chip with its 22FDX platform for ultra-low power consumption for intelligent devices at the edge.

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PHOTO-DRIVEN ELECTRONIC SKIN ENABLE ACTIVATION OF CALCIUM CHANNEL FOR REFRACTORY WOUND HEALING

A team of researchers developed an environment friendly photo-driven electronic skin for refractory wound repair promotion, which composed of the micro-pillar p-type Si thin-film and an NIR irradiation unit. The fabrication of micro-pillar p-type Si thin-film starts with silicon-on-insulator (SOI) wafers.

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A METHOD FOR FABRICATING CAVITY-SOI AND ITS VERIFICATION USING RESONANT PRESSURE SENSORS

Experimental findings show that during the formation of Cavity-SOI, dry etching can accurately fabricate cavities of predefined dimensions, wafer-level Au-Si eutectic bonding can achieve efficient sealing, and chemical mechanical polishing can precisely regulate the depth of cavities, thus validating the feasibility of the Cavity-SOI formation process.

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EXPERIMENTAL PARAMETER STUDY OF THERMALLY TUNABLE MACH-ZEHNDER SWITCHES

Tunable Mach-Zehnder switches (MZIs) play a key role in upcoming fields like neuromorphic photonic computing for AI applications. This work presents a comprehensive experimental parameter study of thermally tunable MZIs on SOI, compared the results to Lumerical simulations and found very good agreement.

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SOI ECOSYSTEM NEWS

STMICROELECTRONICS TO ENABLE HIGHER-PERFORMANCE CLOUD OPTICAL INTERCONNECT IN DATACENTERS AND AI CLUSTERS

ST's new, proprietary silicon photonics (SiPho) technology will bring customers the ability to integrate multiple complex components into one single chip, while ST's next-gen, proprietary BiCMOS technology brings ultra high-speed and low power optical connectivity, which are key to sustain the AI growth.

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CEA AND QUOBLY REPORT SIMULTANEOUS, MICROSECOND QUBIT-READOUT SOLUTION WITH 10X POWER-USE REDUCTION

CEA-Leti, in its collaboration with Quobly, CEA-List and CEA-Irig, reported it has developed a unique solution using FD-SOI CMOS technology that provides simultaneous microsecond readouts of tens of quantum devices, while reducing the readout power consumption by 10x and footprint by 2x.

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HIGH-Q MINIATURIZED BOUND STATE IN THE CONTINUUM MICROCAVITIES ON THIN-FILM LITHIUM NIOBATE TOWARDS EFFICIENT SPATIAL LIGHT MODULATION

By leveraging the high-order topological charge of $q = -2$ carried by bound states in the continuum (BICs), the proposed microcavity reaches an ultra-high Q up to 1.2×10^5 , showing as a milestone record for the BIC cavities on the thin-film lithium niobate (TFLN) platform.

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EFFECTS OF ELECTRON BEAM LITHOGRAPHY PROCESS PARAMETERS ON THE STRUCTURE OF NANOSCALE DEVICES ACROSS THREE SUBSTRATE MATERIALS

Electron beam lithography (EBL) is a pivotal technology in the fabrication of nanoscale devices, renowned for its high precision and resolution capabilities. This paper explores the effect of EBL process parameters on various substrate materials, including silicon dioxide, silicon-on-insulator (SOI), and silicon nitride.

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COMPOUND SEMICONDUCTOR

ROHM TEAMS FOR GAN TOLL PACKAGING

In response to the increasing adoption of GaN devices in the automotive sector, which is expected to accelerate in 2026, Rohm plans to ensure the rapid introduction of automotive-grade GaN devices by strengthening these partnerships in addition to advancing its own development efforts.

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KOREAN TEAM DEVELOPS METHOD TO EVALUATE SIC CHIPS FOR SPACE

A research team at Korea has developed technology to evaluate radiation resistance and reliability of SiC power semiconductor devices in Space. The team plans to expand the technology's scope by pursuing reliability evaluations of SiC power semiconductors under ultra-high energy radiation conditions and developing advanced radiation-resistant power semiconductors.

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CRACK-FREE LOW THREADING DISLOCATION DENSITY ALGAN FOR SUB-365NM UV

Researchers from China reports the lowest $6.65 \times 10^8/\text{cm}^2$ threading dislocation density for crack-free aluminium gallium nitride grown on unpatterned sapphire. The team performed two-step growth by metal-organic chemical vapor deposition on sapphire substrates with 25nm sputtered AlN films as nucleation.

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ALSCN-BARRIER GAN HEMT WITH RECORD HIGH ON-CURRENT

Researchers in the USA claim record high on-current up to 4A/mm for gallium nitride (GaN) high-electron-mobility transistors (HEMTs) with an epitaxial aluminum scandium nitride (AlScN) barrier layer. The material for the HEMTs was grown using plasma-assisted molecular beam epitaxy on silicon carbide (SiC) substrate.

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SEMI BLOG

SUSTAINABLE AI SYSTEMS FOR ENERGY-EFFICIENT COMPUTING

AI runs on the semiconductor engine, and in turn, creates a rising demand for semiconductor chips. The semiconductor industry is predicted to reach \$1 trillion in revenue by 2030, in large part due to the market demand for AI and data. However, there are formidable challenges to overcome for this virtuous cycle to continue. Addressing these challenges requires innovation from algorithms and architecture to foundational silicon technologies.

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SEMI NEWS HIGHLIGHT

SEMI CYBERSECURITY CONSORTIUM'S NIST SEMICONDUCTOR MANUFACTURING COMMUNITY PROFILE OPENS FOR PUBLIC FEEDBACK

The commentary period runs from February 27 through April 14, 2025, with a public workshop to review comments and plan the next steps to follow on March 13, 2025. NIST and SMCC request feedback from stakeholders interested in securing the semiconductor supply chain including cybersecurity professionals, equipment manufacturers, engineers, architects, operations professionals, representatives from fabs, fabless companies, and other semiconductor or electronic system providers.

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