

Rethinking Connectivity: HiCONNECTS, FOCAL and the Chips that Power Tomorrow

**Ilan Englard on behalf of NXP-DE and SEMI
20 November 2025**

Agenda



14:35

Heterogeneous Integration Standards Update, Ilan Englard, EU Projects Manager and Consultant HiCONNECTS

14:45

**Towards Quantum-Ready End-to-End Security and Resilience for Critical Infrastructures
Angelos Marnerides, Professor (Asst.), University of Cyprus**

14:55

**Heterogeneous Integration of Co-Packaged Optics to navigate AI complexities
Dimitrios Velenis, Group Leader, imec**

15:05

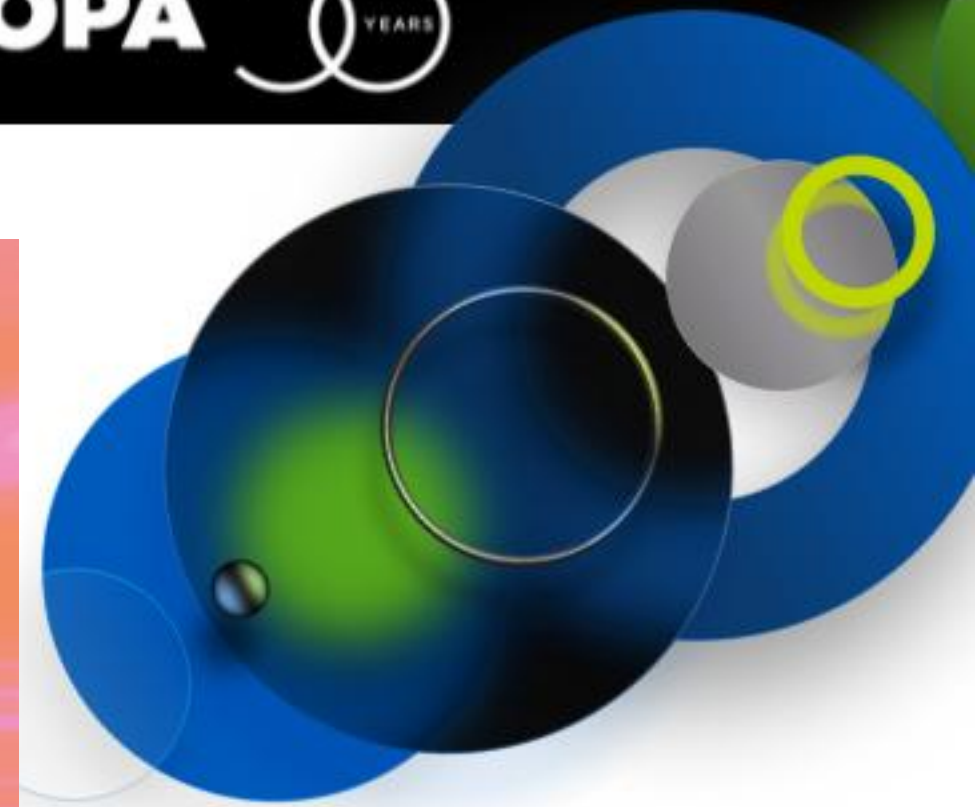
**Development and manufacturing of Co-Packaged optics demonstrator on IC Substrate technology for the beyond state-of-the-art smart NICs and Switches
Gyuhyeon Park, Advanced Technologies and Solutions**

15:15

**Integration and Assembly of Co-Packaged Optics (CPO) for smart Networks and Switches
Anneirudh Sundararajan, Project Leader - Photonics Packaging, PHIX Photonics Assembly**

15:25

Q&A and Closing Remarks by Session Chair, Ilan Englard, EU Projects Manager and Consultant HiCONNECTS



Heterogeneous Integration (HI) presents unique opportunities and challenges regarding security and sustainability in the semiconductor industry. It offers advantages like enhanced performance and functionality but also introduces new vulnerabilities and environmental considerations across the design, manufacturing, and supply chain processes



HiCONNECTS is driving Europe's next wave of innovation in **semiconductor integration** – enabling faster, greener and smarter electronic systems for the cloud, edge, and automotive industries.

Ask us about:

- Advanced heterogeneous integration
- Sustainable semiconductor manufacturing
- AI and automotive
- European innovation in packaging

FOCAL is advancing **post-quantum cryptography (PQC)** and cybersecurity by developing an optimal, interoperable, end-to-end PQC system framework to ensure quantum-safe security across critical European networks.

Ask us about:

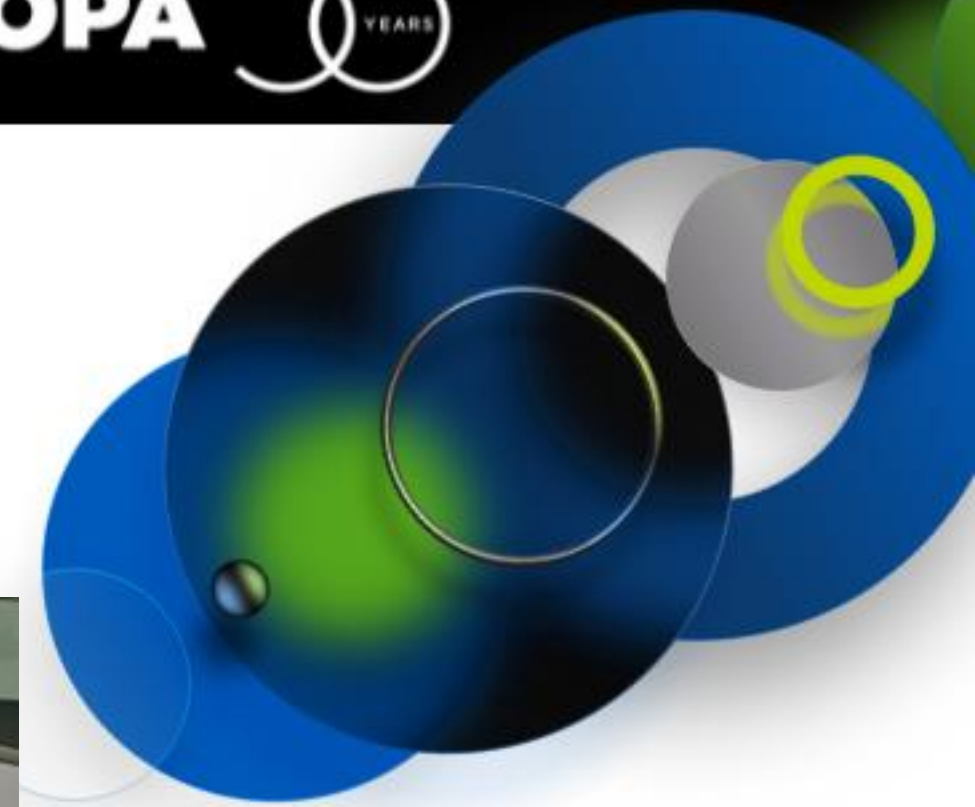
- Post-quantum cryptography
- Cyber Security
- PQC Transition
- Crypto-Agility

GENESIS is an EU program supported by CHIPS JU and its associated members states. In addition, GENESIS Swiss partners are supported by the Swiss state secretariat (SERI). Its mission is to reduce the environmental footprint of semiconductor manufacturing while enabling innovation across materials.

Ask us about:

- Sustainable semiconductor manufacturing
- Solution for harmful chemicals
- Collaboration across Europe's semiconductor ecosystem
- Innovation driving a more sustainable digital future

 **Funded by the European Union**

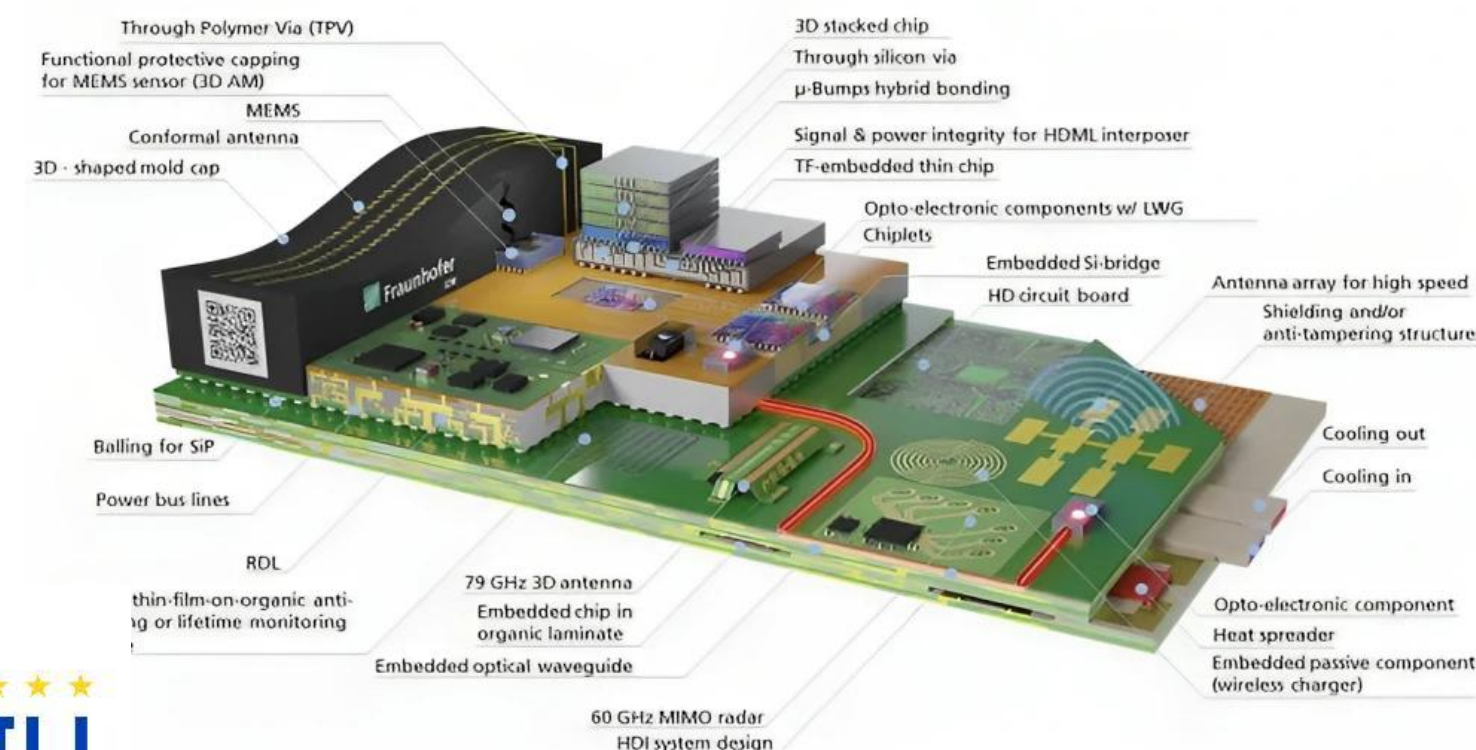


HiCONNECTS Consortium

HETEROGENEOUS INTEGRATION FOR CONNECTIVITY AND SUSTAINABILITY (2023 – 2026)

The HiCONNECTS project develops the next generation of electronic components and systems heterogeneous integration core technology solutions for energy-efficient, high-performance wireless/wired cloud and edge computing and automotive radar in support of the next radio frequency and IT technology evolution. It covers the full semiconductors value chain from design to manufacturing front and back end.

The consortium consists of a well-balanced set of large enterprises (55%), SMEs (23%), RTO (14%) and academic institutions (8%). Partners from 15 countries.

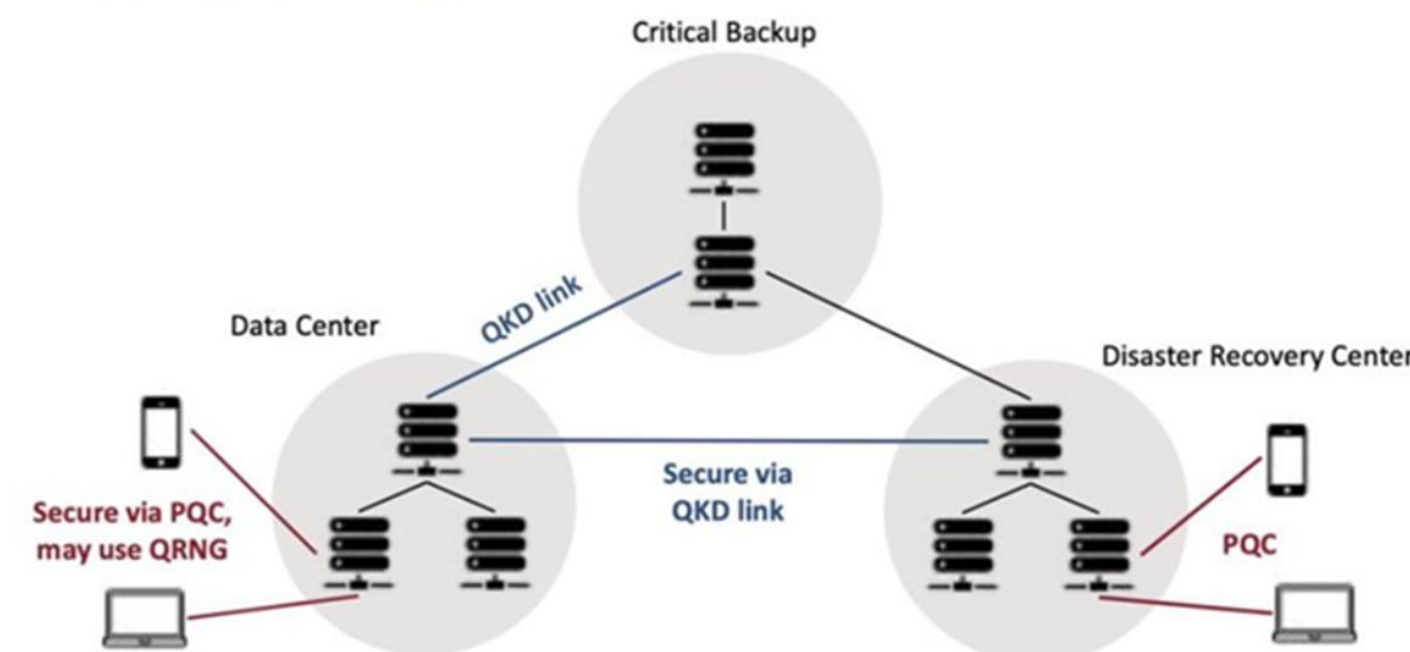


FOCAL Consortium

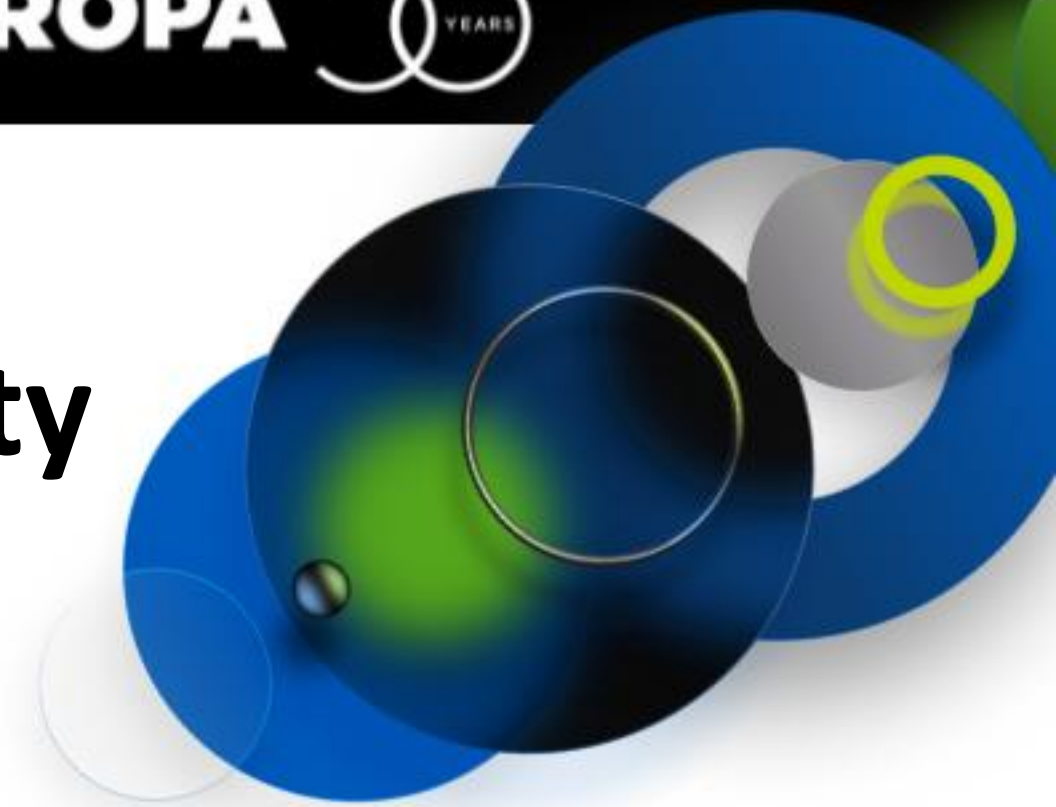
FUNCTIONAL COMPOSITION OF POST QUANTUM CRYPTOSYSTEMS AT LARGE (2025 – 2028)

The FOCAL project focuses on advancing post-quantum cryptography (PQC) and enhancing cybersecurity across critical European sectors.

Coordinated by the University of Cyprus and supported by 14 consortium partners, FOCAL aims to develop theoretical foundations and engineering mechanisms for the first optimal and interoperable end-to-end (E2E) functional composition of PQC-enabled systems across both provisioned and resource-constrained large-scale networked environments. The project contributes significantly to the EU's strategic objectives and guidelines as outlined in the European Commission Recommendation on Post-Quantum Cryptography.



Heterogeneous Integration (HI) for Connectivity and Sustainability



Technology Challenges

- **IoT:** High latency and power consumption, low bandwidth limiting real-time IoT applications.
- **Connectivity:** Lack of resolution, classification, segmentation, localization, and mapping in radars not enough to achieve L4-5 Autonomous Driving.
- **More than Moore's Law:** need of alternative chips design, process and metrology which are cost-competitive, low power, and have high performance.
- **Digital Sovereignty:** Current EU semiconductors market share is only 10%.

Scope

To develop compelling and cost competitive heterogeneous integration (HI) core technology solutions for energy-efficient and high-performance Silicon based RF and photonics solutions enabling:

- 1- Fast transmission of IoT data over the network.
- 2- Sensing for L4-5 Autonomous Driving.

HiCONNECTS will also aim at using the novel RF solutions (5G/6G and radar) and IT cloud infrastructure for connected vehicles, industry 4.0 and smart health, smart cities.

Societal and Environmental Impacts

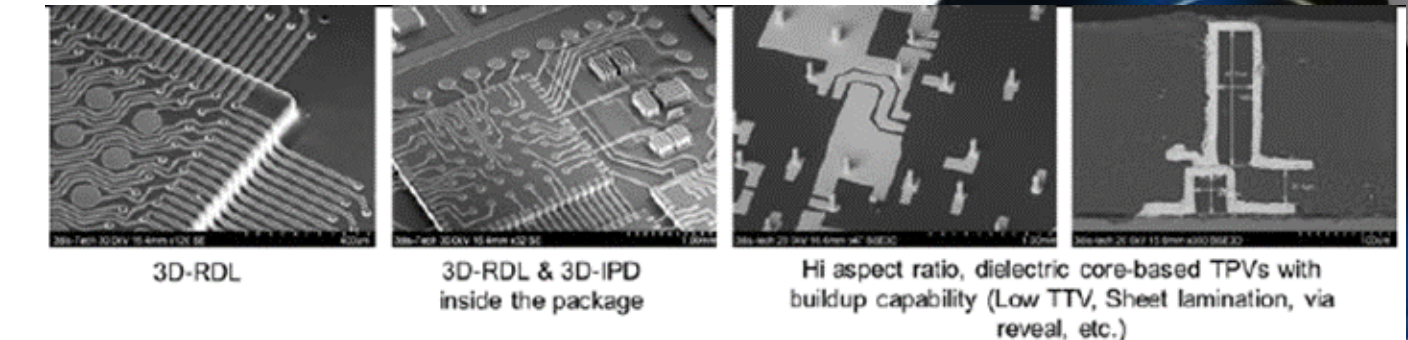
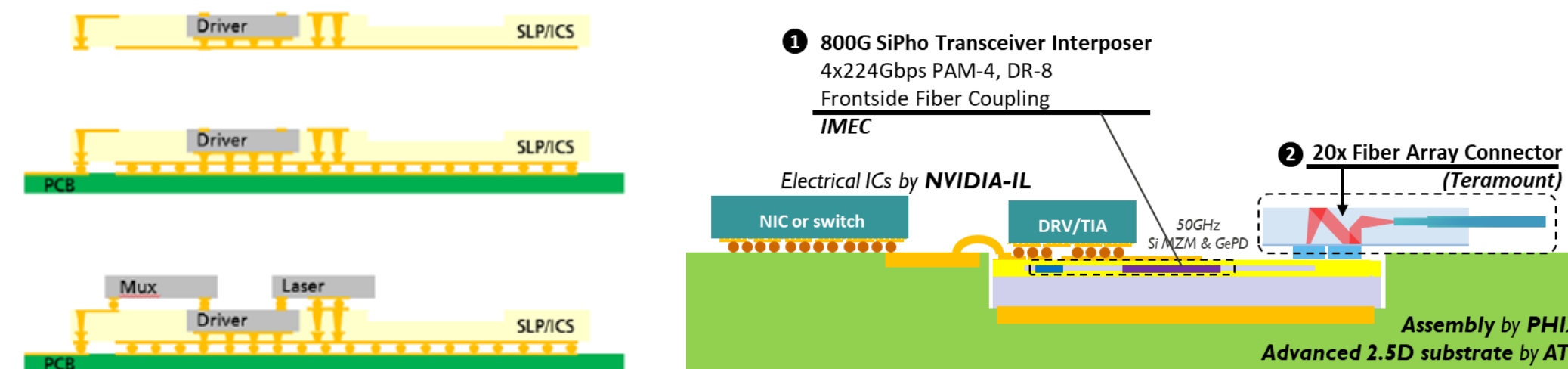
EU Sovereignty and Industrial Competitiveness

Digital Autonomy	Novel low power, cost- and performance- efficient, scalable HI products boosting EU market share in cloud, smart cities and automotive applications.
Digital Health Care	Smart drugs & vaccines development (Cryo-EM workflow) and delivery enabled by high-speed data transfer in data centers.
Cities of the Future	Deployment of a reliable connectivity infrastructure (IoT, cloud), incl. A.I. solutions. Highly effective vehicular communications for traffic management.

EU Green Deal

Resource efficient and carbon neutral EU	Energy efficient communications, radar and cloud, which will pave the way to real-time response and resilience against hazards & related CO2 emissions (e.g. wildfires).
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Pilot Lines



Pilot Line 1

RF Electronics HI

Lead: Ferdinand-Braun- Institut

- HI for high-speed broadband & RF electronics based based on InP on BiCMOS, incl. thermal management.
- Photonic and electronic heterogeneous integration.

Pilot Line 2

Photonic Components for HI

Lead: IMEC

- Next gen. photonics components and Si photonics based on HI platform development.
- High-Speed Lasers and Photodetector.

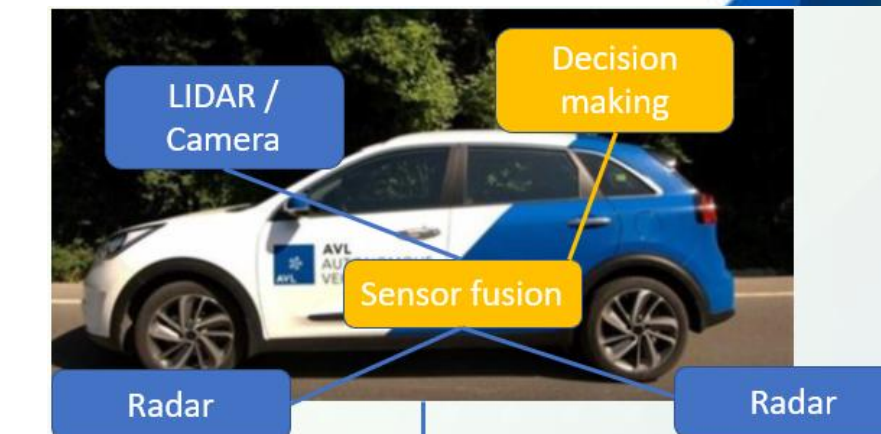
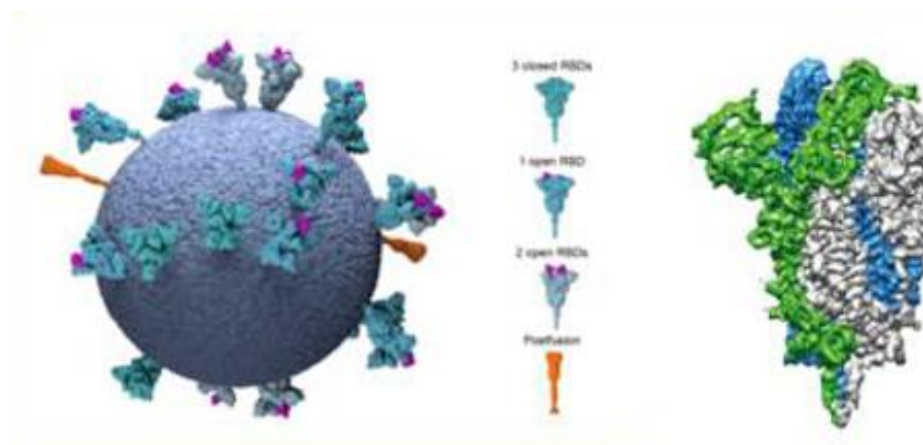
Pilot Line 3

Advanced Packaging

Lead: 3DiS

- 3D-Fan-Out Wafer Level Packaging, pivotal for antenna in packages, and 5G/6G packages (beyond 100 GHz).
- Next gen. interconnects based on glass interposer.

Demonstrators



Public Health Lead: Thermo Fisher

- Cryo-electron microscopy Data Management Platform (DMP) for fast access and processing.
- AI-enabled data-analytics.

Public protection and disaster relief Lead: Centria

- Drone equipped with 77 GHz radar, sensor and camera tech.
- Situation Awareness: edge processing and AI acceleration.
- Comms: 5G/6G.

Smart Construction Lead: ULAK

- Holographic communication
- Mobile Edge.
- Fully connected and autonomous UGV and excavator with sensors (LIDAR, radar & stereo camera).

Connected & Autonomous mobility Lead: AVL

- Trustworthy and explainable AI for L4 car.
- High performance radar, C-V2X modem.
- High accuracy intention recognition.



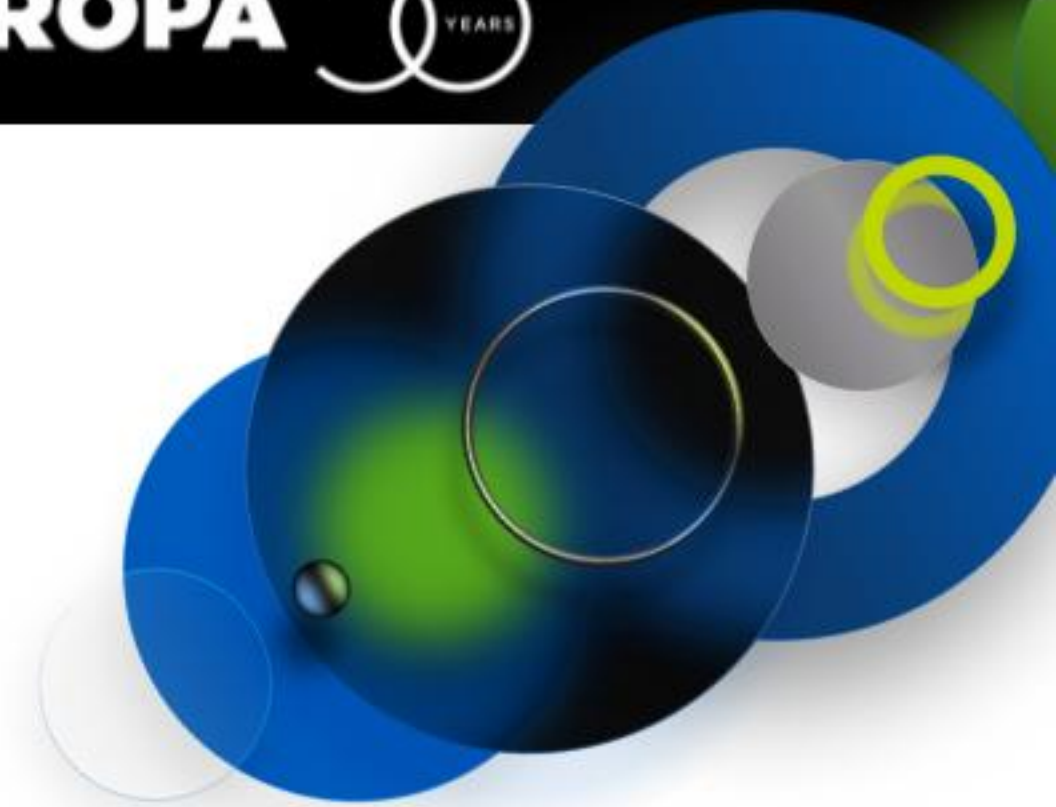
Status after 2.5 Years

Heterogeneous Integration processing modules:

- Progress toward 400GBAUD (800Gb/s) connectivity proceeding as planned, e.g. Monolithic Microwave Integrated Circuit (MMIC) scaled down transistors (400 -> 300nm node) had been realized.
- High-speed transceivers architecture and integration scheme finalized and components taped out.
- RF packaging activity with novel multi redistribution layers (RDL) finalized.

Heterogeneous Integration based systems productization:

- ST-I enhancement of in-line metrology and predictive manufacturing on-going.
- AT&S finalized the panel level integration design with both NXP (RF components and antenna for 70GHz and D band 140 GHz) and NVIDIA (networking card and switches).



Status after 2.5 Years

Public Health and Safety Demonstrator:

- TEM data management platform (DMP)-based protein's structure determination (including COVID19) workflow established.
- Public protection and disaster relief preparations and specifications established.

Automotive and Smart City Demonstrator:

- Smart automotive logistics: area and scenario & possible implementations defined.
- Digital Twin to optimize stamping manufacturing incl. wireless 5G communication, data collection at Edge and AI based anomaly detection with image processing. discussions, site visit and planning were completed;
- Smart construction area set up incl. connectivity modules development (C-V2X) and 5G modems and UGV.
- L4 autonomous vehicle high-level architecture (incl. NXP radar) and use case scenario being planned for highway environment.

Standardization activities, incl. surveys and participation to committees (e.g. IPC- CFX, ETSI).



SEMI Technology Coalition & Standards Activities

HiCONNECTS Session

TechARENA | SEMICON Europa 2025

CONNECT - COLLABORATE - INNOVATE - GROW - PROSPER



SEMI is Uniquely Qualified to Address the Industry’s Top Challenges that Require Global Collaboration

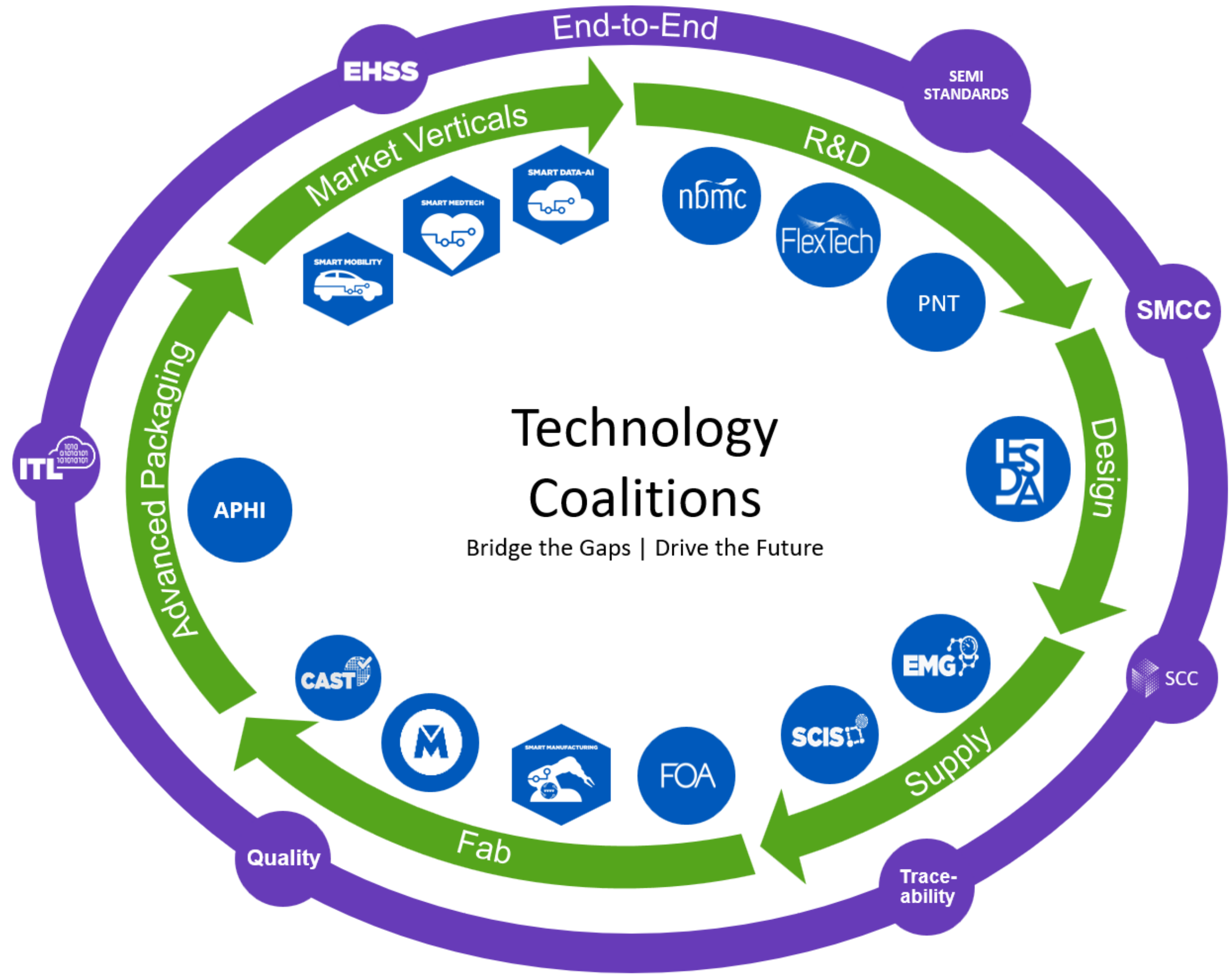
 SEMI™	Foundational	Expanded Programs and Scope				2025 Top Priorities
3,000+ members worldwide Spanning the Semiconductor and Electronics Design and Manufacturing Supply Chain Driving Global Programs	Thought Leadership	Worldwide Offices	Market Intelligence Reports	Tech partners: imec, Fraunhofer, CEA-Leti, IEEE, ITRI, AIST	Supply Chain Resilience	Global Advocacy & SIPS Platform
	Standards	2,300+ Program Hours				Workforce Development
	SEMICON® Expositions/Conferences	170+ Tech Programs				Sustainability
	EHS	20+ Tech Communities				PFAS
			Smart Initiatives	Strategic Tech Communities: ESDA, IESA, FOA, FlexTech, MSIG, SOIIC		Cybersecurity & AI
			Think Tanks			

SEMI Technology Communities



PROVIDING TECHNOLOGY STEWARDSHIP & COLLABORATION ACROSS THE ECOSYSTEM

PARTICIPATE | CONNECT | CONTRIBUTE | LEARN | LEAD | ENGAGE | COLLABORATE | TEACH | NETWORK | DISCUSS | CHALLENGE



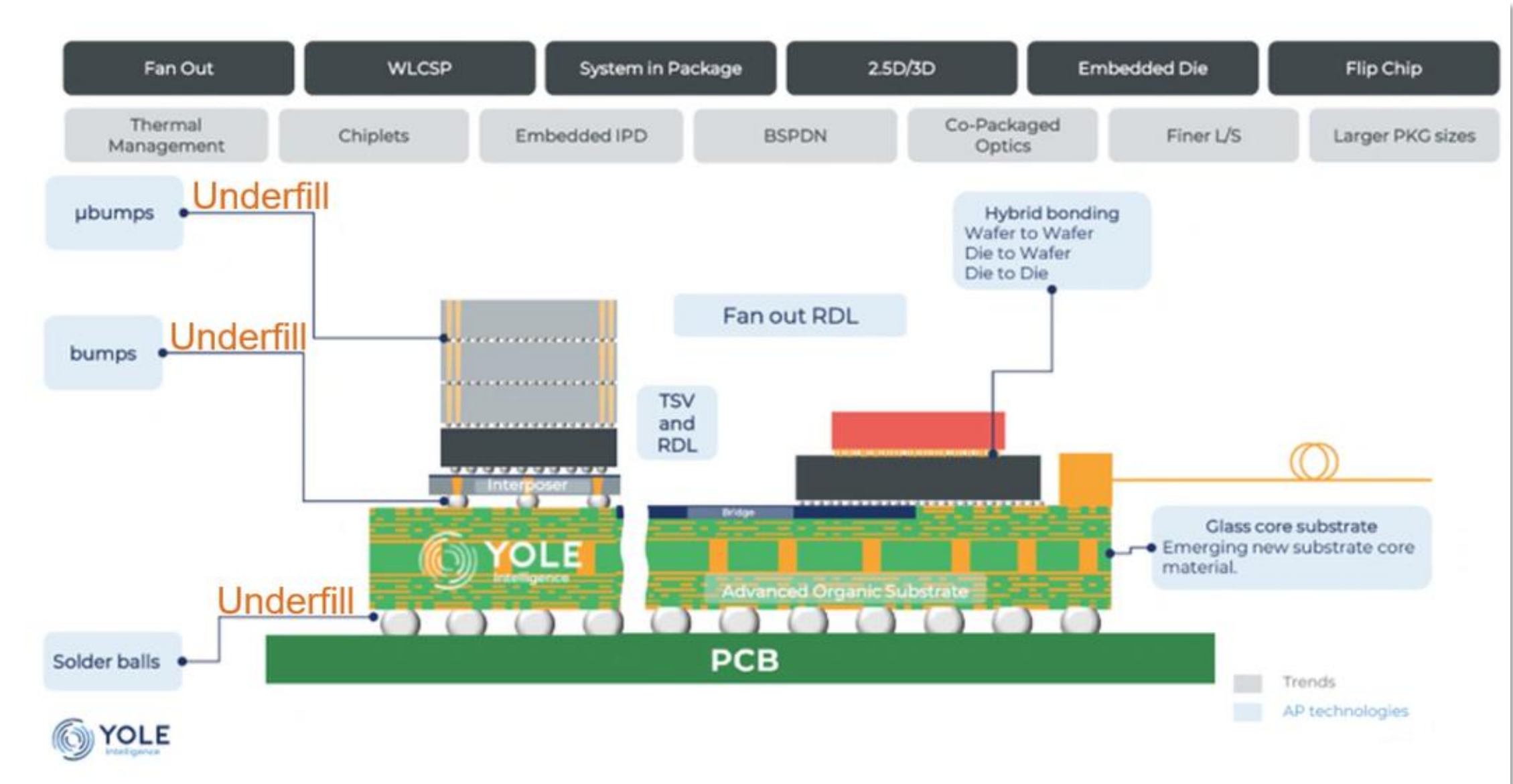


SEMI Advanced Packaging & Heterogeneous Integration (APHI) Initiative



Criticality of Advanced Packaging Enabling the Next Era of Electronics

- Improves circuit / system performance (memory to CPU bottleneck, lower latency)
- Lowers cost (IP reuse and chip technology optimization)
- Increases design flexibility and enables IP block performance optimization (heterogeneous integration/chiplets)
- Drives the attributes of Moore's law beyond linear shrinks



Source: Yole

- Transistor density through interconnect abundance (3D stacking)
- Maximize compute performance through function and system partitioning changes
- Better power efficiency (power delivery design, lower parasitics/loss, HI optimization)

SEMI APhi Initiative

Vision, Mission and Key Deliverables

Focus on Advanced Packaging & Heterogeneous Integration

- Awareness through education (SEMI U¹) and events (Conferences & Forums)
- Active in all SEMI regions to address shared/common challenges

Support Global APhi Technology (pre-competitive) Development

- Global APhi TC to facilitate holistic & congruent roadmaps² including regional HI startups technology roadmaps
- Identify technology gaps & new standards to support APhi (non-duplicative)
- Build tools for members to assess existing capability & use cases to validate ROI for onshoring project

Innovation for APhi Manufacturing Readiness

- Facilitate member-driven technology & proof-of-concept projects
- Support innovation through CHIPS NSTC/NAPMP Programs

VISION: To foster an Advanced Packaging and Heterogeneous Integration (APhi) community focused on supporting global, pre-competitive tech development and innovation for mfg readiness

MISSION: To educate, raise awareness, remove barriers, drive consensus and adoption, interoperability and development of design-enabling Advanced Packaging and Heterogeneous Integration (APhi) technology and standards, empowering electronics industry and its enabling ecosystems to speed up time to market for reliable advanced electronic and photonic system

¹ Collaborate with IEEE EPS for course development

² HIR founding members meeting – keep roadmap healthy with a dedicated headcount (1/3 share with IEEE-EPS, SEMI, ASME)

Global Activity

SEMI Americas

- ★ Regional Chapter
- ★ Regional Exec. Committee
- APHI @ SEMICON West
- ▲ HIR Roadmap
- ▲ R&D Public-Private Consortia Projects

SEMI Global

- ★ APHI IAC
- ASMC, SMC, HI Symposium

SEMI Europe

- ★ SiPAT Committee
- ★ Regional Exec. Committee
- 3D & Systems Summit
- APHI @ SEMICON Europe
- ▲ CSA Pan EU AP project

SEMI China

- ★ Regional Chapter
- APHI Seminar, Semi Mfg & AP Forum

SEMI Korea

- ★ Regional Chapter
- ★ Regional Exec. Committee
- Interconnect Package @ STS

SEMI Japan

- ★ Regional Chapter
- ★ Regional Exec. Committee
- APCS @ SEMICON Japan

SEMI Taiwan

- ★ Regional Chapter
- APHI Forum @ SEMICON Taiwan
- SiP Global Summit, HI Global Summit

SEMI SouthEast Asia

- ★ Regional Chapter
- ★ Regional Exec. Committee
- APHI Session @ SEMICON SEA

- ★ Leadership
- ◆ Standards
- Event
- ▲ Product

APHI Initiatives

Advanced Packaging & Heterogeneous Integration Standards White Paper



- Motivation
 - Identified need for new standards development to support advanced packaging technologies and processes
- Objective
 - Outline a path forward to developing relevant stds?.
 - Outline a roadmap for stds development and the technology investigations need to support this?
 - Call for Action ? alignment on approach? Do we suggest who does what? !!!
- CTA - Advanced Packaging & Heterogeneous Integration Standards White Paper
- Target Date – December 2025
- Next Steps
 - Recruit Contributors/Reviewers

SEMI 3DIC Advanced Manufacturing Alliance (3DICAMA)

- *Powering the Future of 3DIC Technology*
 - 50+ core members: fabs, OSATs, suppliers, academia
 - Led by Jun He (TSMC) & Mike Hung (ASE)
 - Tackling key challenges and scaling future of advanced packaging
- *Three Active Special Interest Groups (SIGs):*
 - Standards: Tool capacity & material quality
 - Packaging Process Tech: Next-gen tools & materials
 - Metrology & Inspection: Defect detection & yield improvement

SIGs to define priorities and technical direction in closed-door sessions
- *Public Kickoff – Sept 10, 2025*
 - Keynotes • Panels • Networking • Roadmap Reveal



SEMI Manufacturing Cybersecurity Initiatives



Semiconductor Manufacturing Cybersecurity Consortium (SMCC) – A SEMI Technology Community



Vision: **Strengthen cyber resilience and protection** of the global semiconductor supply chain against evolving threats.



Mission: Develop and promote a **standards-based, industry-wide** approach to improve cybersecurity and accelerate implementation of actionable solutions.



Optimal Member Profile

- Mix of **DMs & OEMs** representing **large and small** companies
- Active participation in **pre-competitive** environment with focus on **problem-solving**

Key focus areas

SMCC workgroups are focused on implementing Cybersecurity controls into our industry factories & supply chain

1

Develop a **robust framework** for cybersecurity that incorporates **lessons learned** from the recent transition and embraces open collaboration.

2

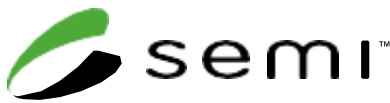
Create a **semiconductor industry-specific framework** to assess the strength of cybersecurity across the supply chain and **implement measures** to better protect ecosystem networks.

3

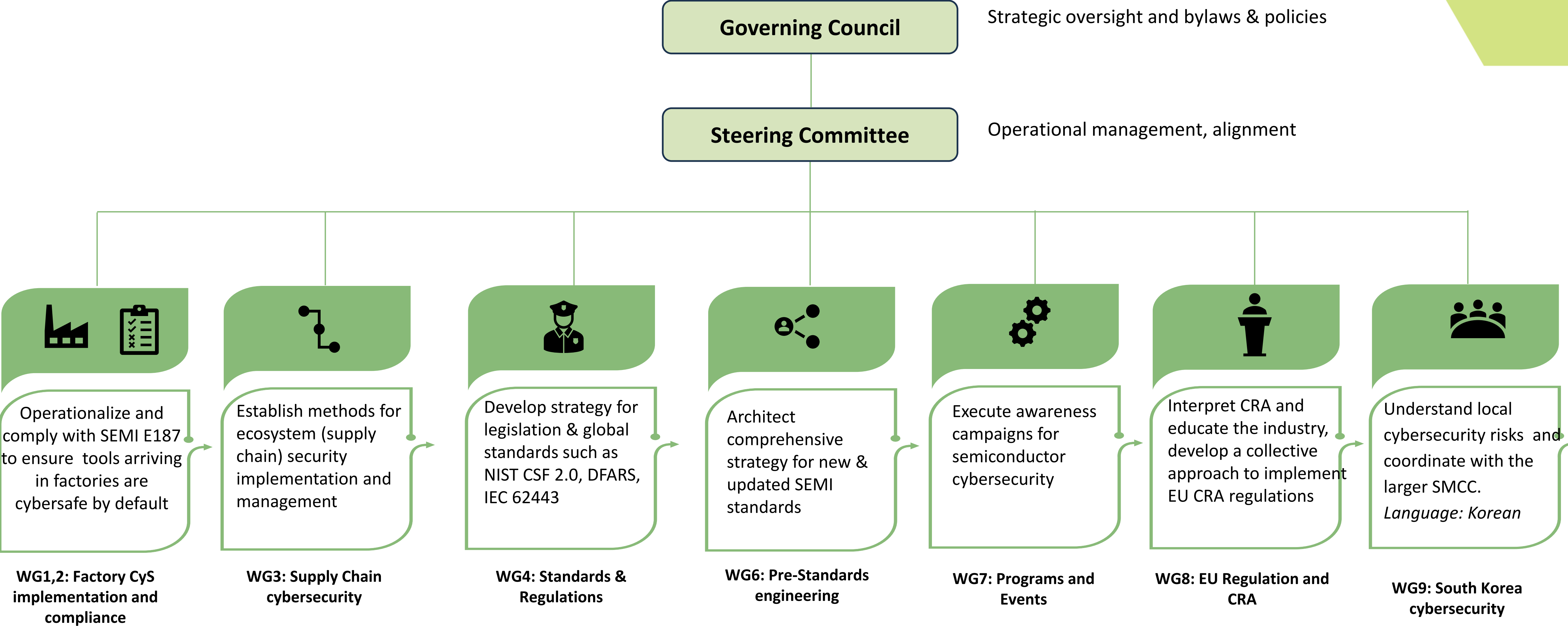
Incorporate **best practices from other industries** such as **automotive and medical** with the aim to modernize security protocols and facilitate greater collaborative information sharing through SEMI.



For more information or to join, contact
cybersecurity@semi.org



Organizational Structure



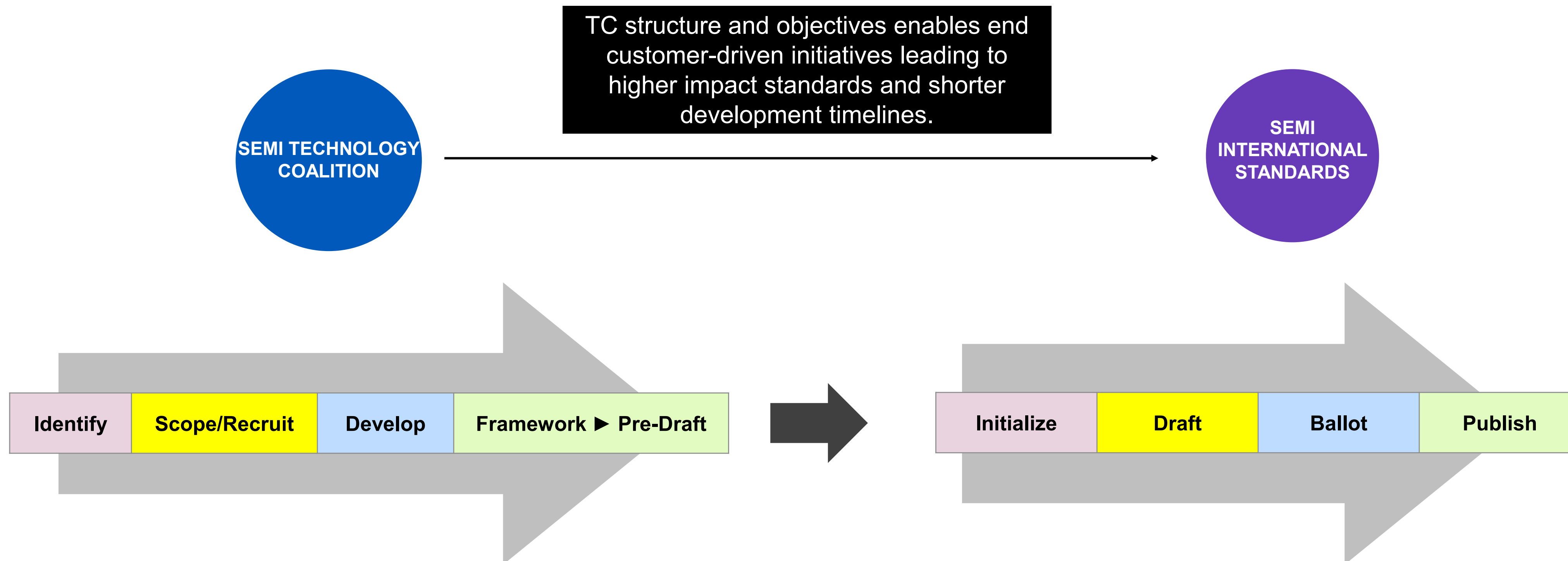


Leveraging SEMI Technology Coalitions for Standards Development

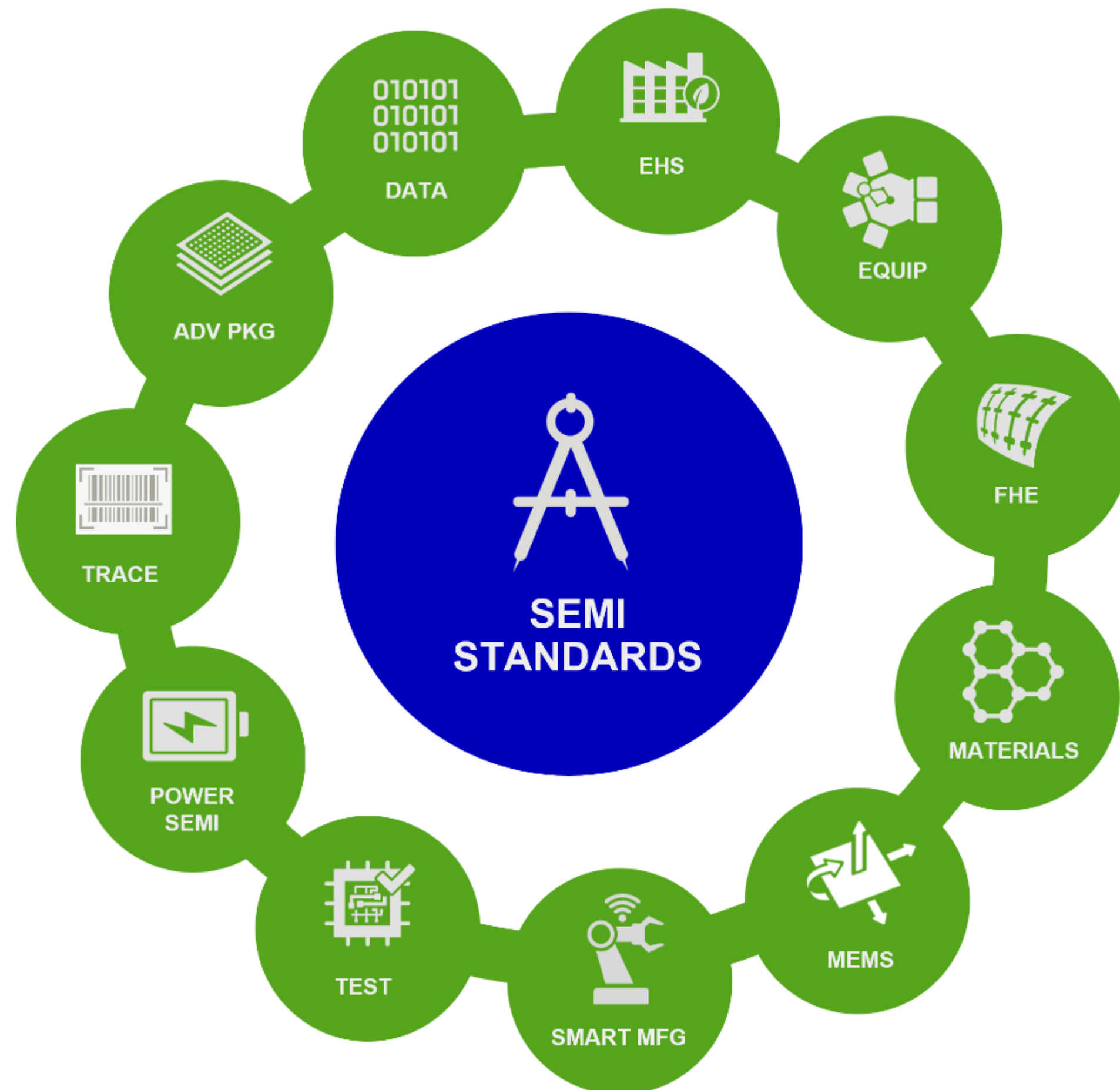
SEMI Standards Program Overview



SEMI Technology Coalitions (TC) to Standards – Process Flow



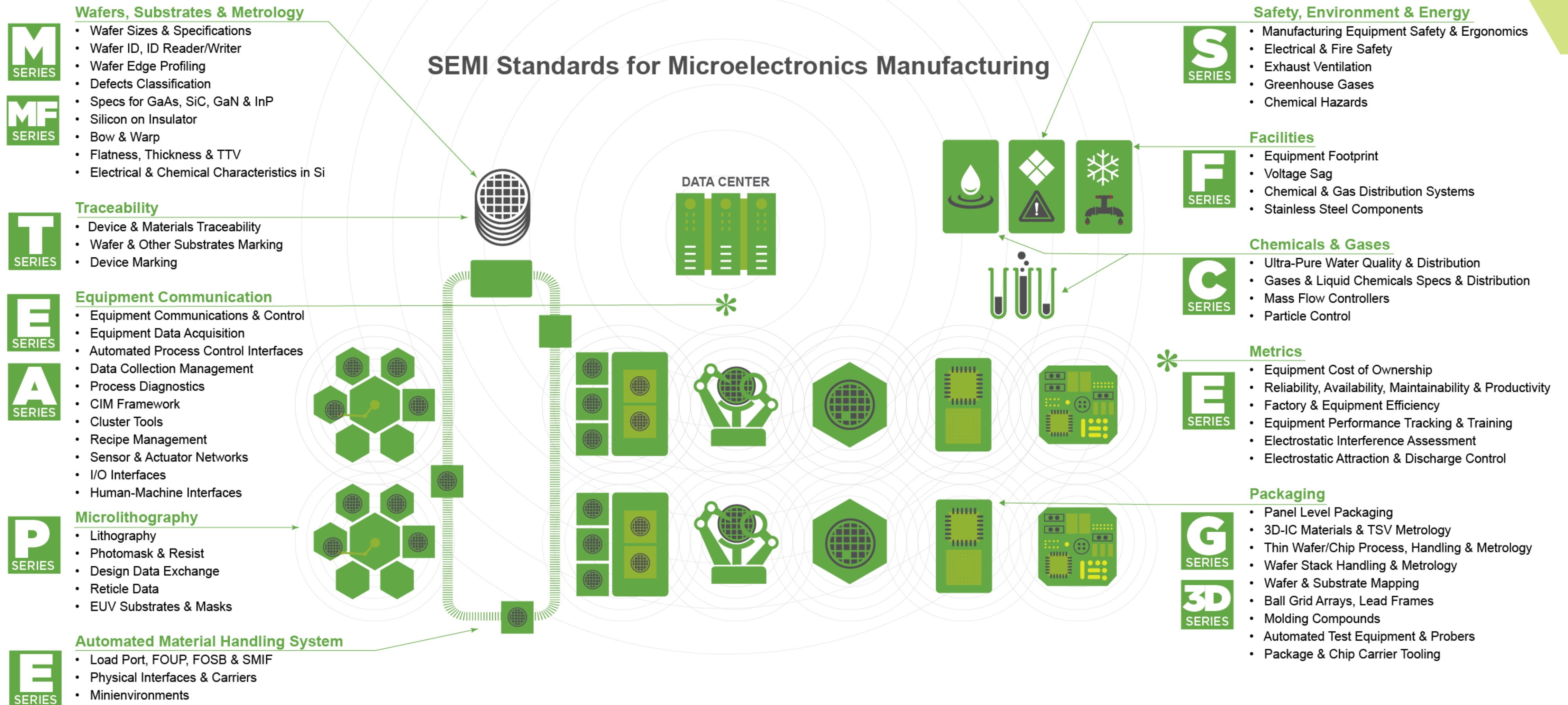
SEMI International Standards Overview



- **Established in 1973**
- **1,100+** published SEMI Standards & Safety Guidelines
- **5,000+** volunteer experts
 - 21 global Technical Committees
 - 200+ global Task Forces
- **2,000+** participating companies
- **Experts from semiconductor, PV, LED, MEMS, FHE & Display industries**
- **International presence**

Exchange ideas and develop globally-accepted technical standards

Enabling Microelectronics Manufacturing



SEMI Standards Supporting Advanced Packaging & Heterogeneous Integration

- Panel Level Packaging (PLP)
 - Panel Characteristics (Size) – [3D20](#)
 - Handling / Equipment
 - Panel FOUP – [E181](#)
 - Panel FOUP Loadport – [E182](#)
 - Glass
 - Glass Carrier Characteristics – [3D23](#)
 - ID Marking – [T24](#)
 - Encapsulation Materials for Wafer-Level Pkg (WLP) & PLP
 - CTE – [G98](#)
 - Flowability – [G99](#)
 - Gel Time – [G100](#)
 - Modulus – [G101](#)
 - Shear Strength – [G102](#)
 - Viscosity – [G103](#)
 - Wettability – [G104](#)

Related SEMI Standards for Supply Chain Traceability

- **SEMI T23** - Specification for **Single Device Traceability** for the Supply Chain
 - Defines, at a high level, the minimum requirements for device ID and traceability for new design and manufacturing implementation as well as for backwards compatibility with existing methods.
- **SEMI E142** - Specification for **Substrate Mappings**
 - Defines the data items that are required to report, store, and transmit map data for substrates such as wafers, frames, strips, and trays. Addresses assembly and packaging including the testing of semiconductor devices.
- **SEMI T25** - Specification for **Blockchain for Semiconductor Supply Chain** Traceability
 - Defines the technical information to manage the information needed to achieve supply chain traceability for semiconductor devices using blockchain.
- **SEMI T26** - Specification for **Electronic Supply Chain Traceability Using Distributed Ledger Technology**
 - Defines a secure, decentralized, traceability system based on Distributed Ledger Technology (DLT) that can be shared by all members of the electronics supply chain.

SEMI Manufacturing Cybersecurity Standards

SEMI E187 - Specification for Cybersecurity of Fab Equipment

Defines overarching and fundamental cybersecurity requirements as a baseline to secure semiconductor fab equipment by design and support security protection in operation and maintenance.

SEMI E188 - Specification for Malware Free Equipment Integration

Provides a framework for how to mitigate the propagation of malware to manufacturing facilities during capital equipment delivery and support activities.

NEW! SEMI E191 - Specification for Computing Device Cybersecurity Status Reporting

Specifies a framework for reporting cybersecurity status information about a computing device.

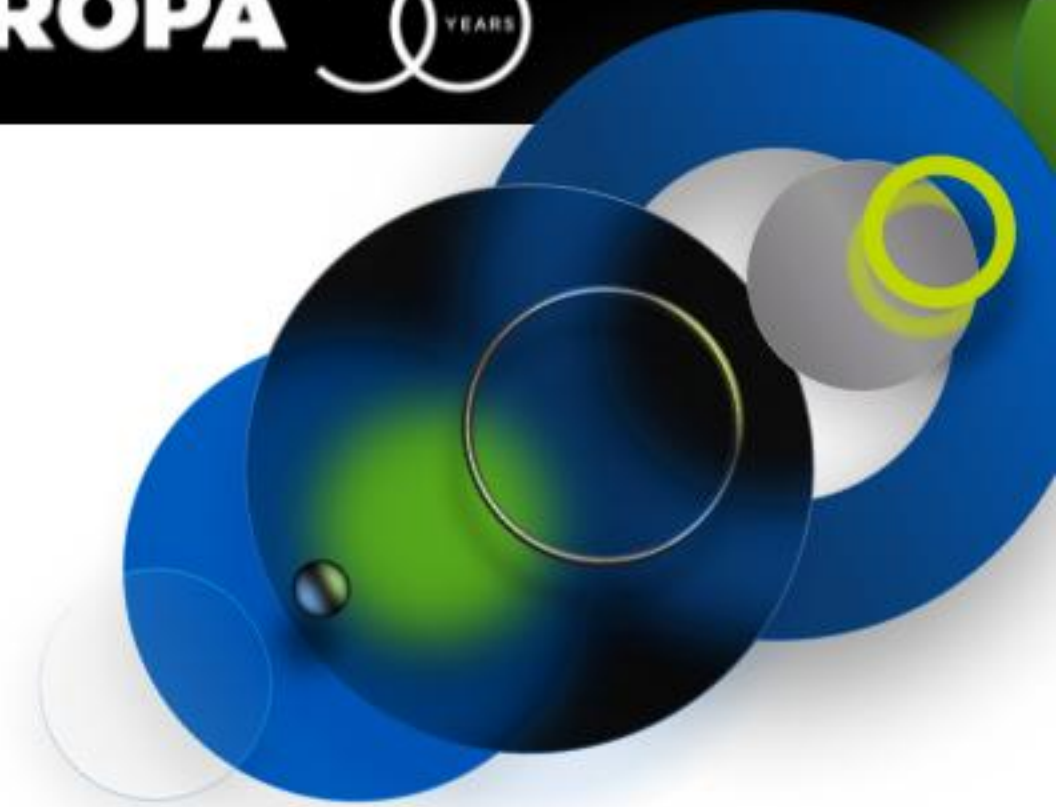
SEMI Standards Membership

- All participants must be registered SEMI Standards Program Members.
- **SEMI Standards Membership is free of charge.**
- SEMI Corporate Membership is NOT required to join the SEMI Standards Program.
 - Standards Membership is separate from SEMI Corporate Membership.
- Standards Members are required to abide by the SEMI Standards Regulations, particularly regarding:
 - IP handling
 - Anti-trust policy
 - Copyright agreement

www.semi.org/standardsmembership

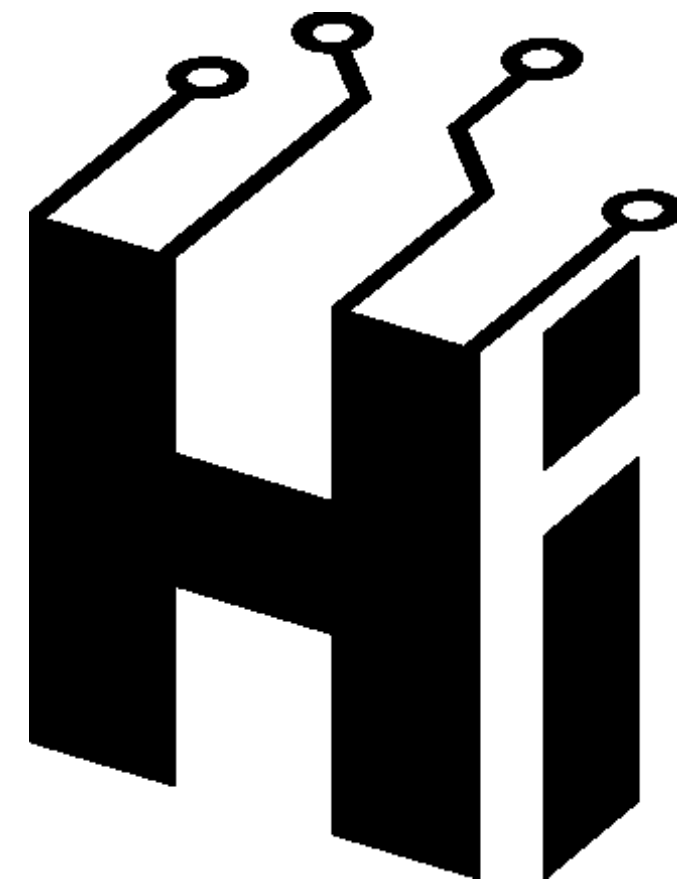
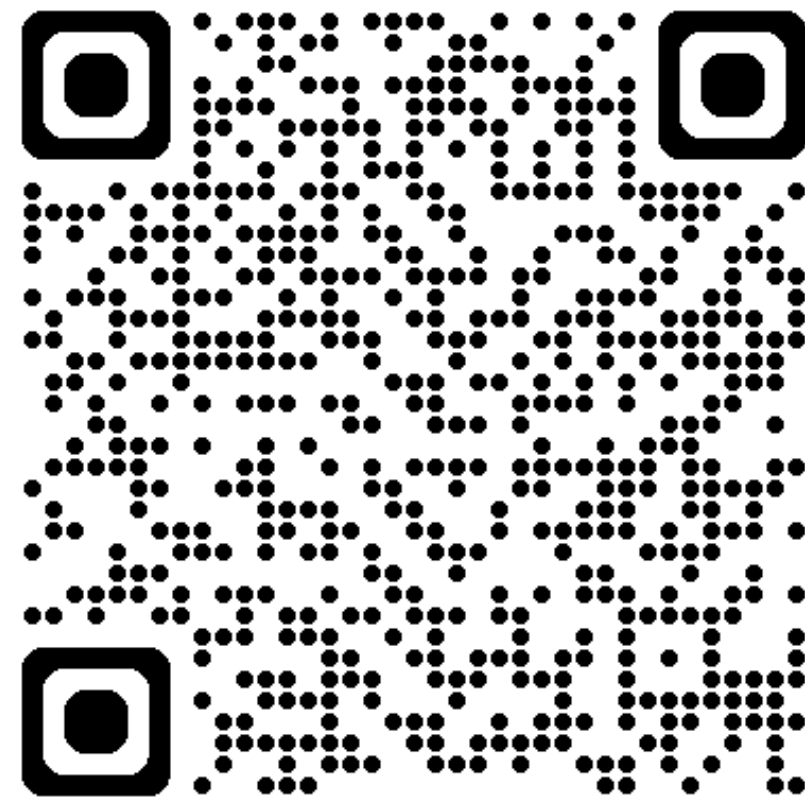
Contact SEMI Standards





Acknowledgement

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Thank you

