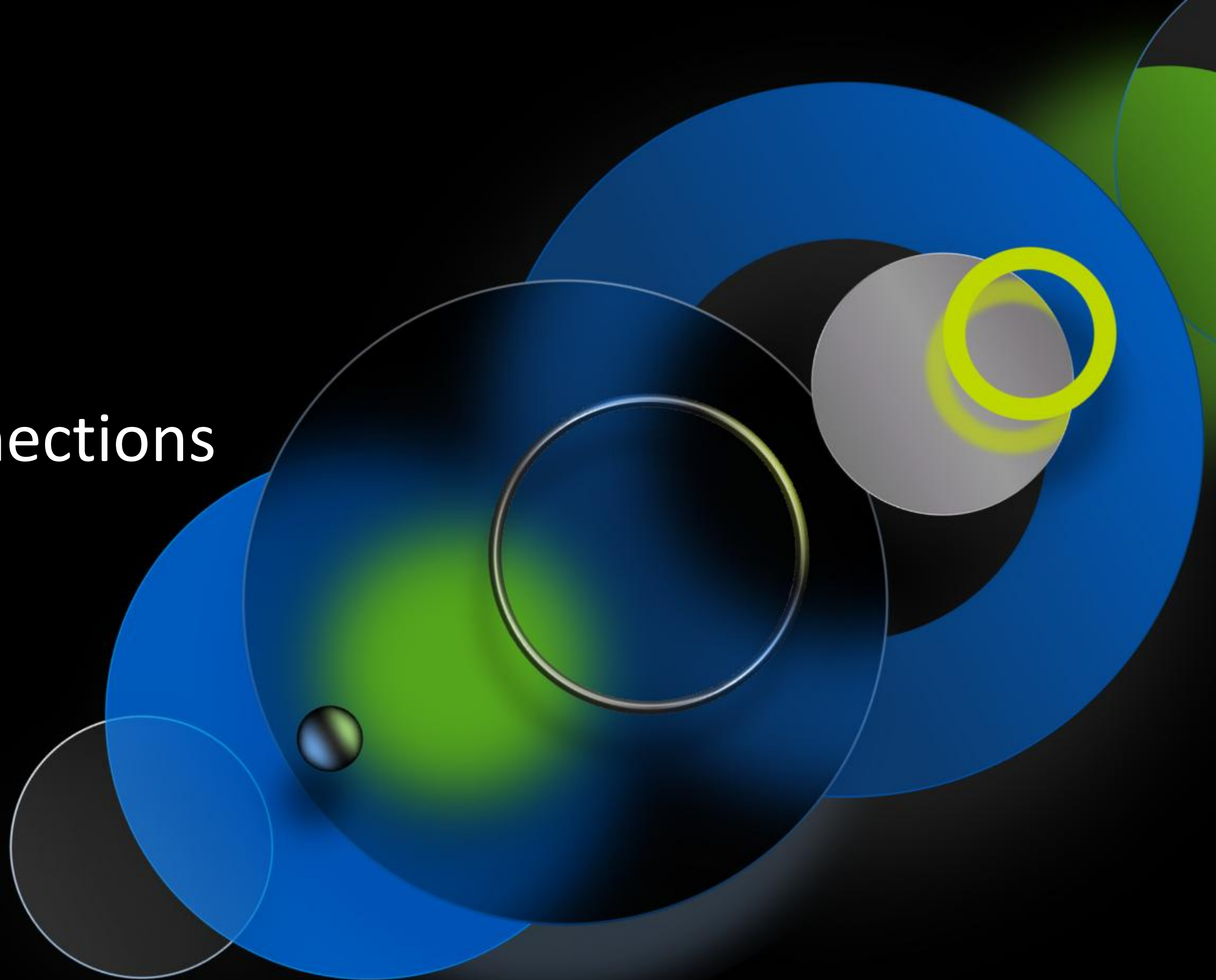


Technologies of Interconnections in Electronics (TIE)

Industry-wide Student Challenges

Octavian-Constantin Axinte,
Technical University of Cluj-Napoca, Romania

Nov. 21, 2025



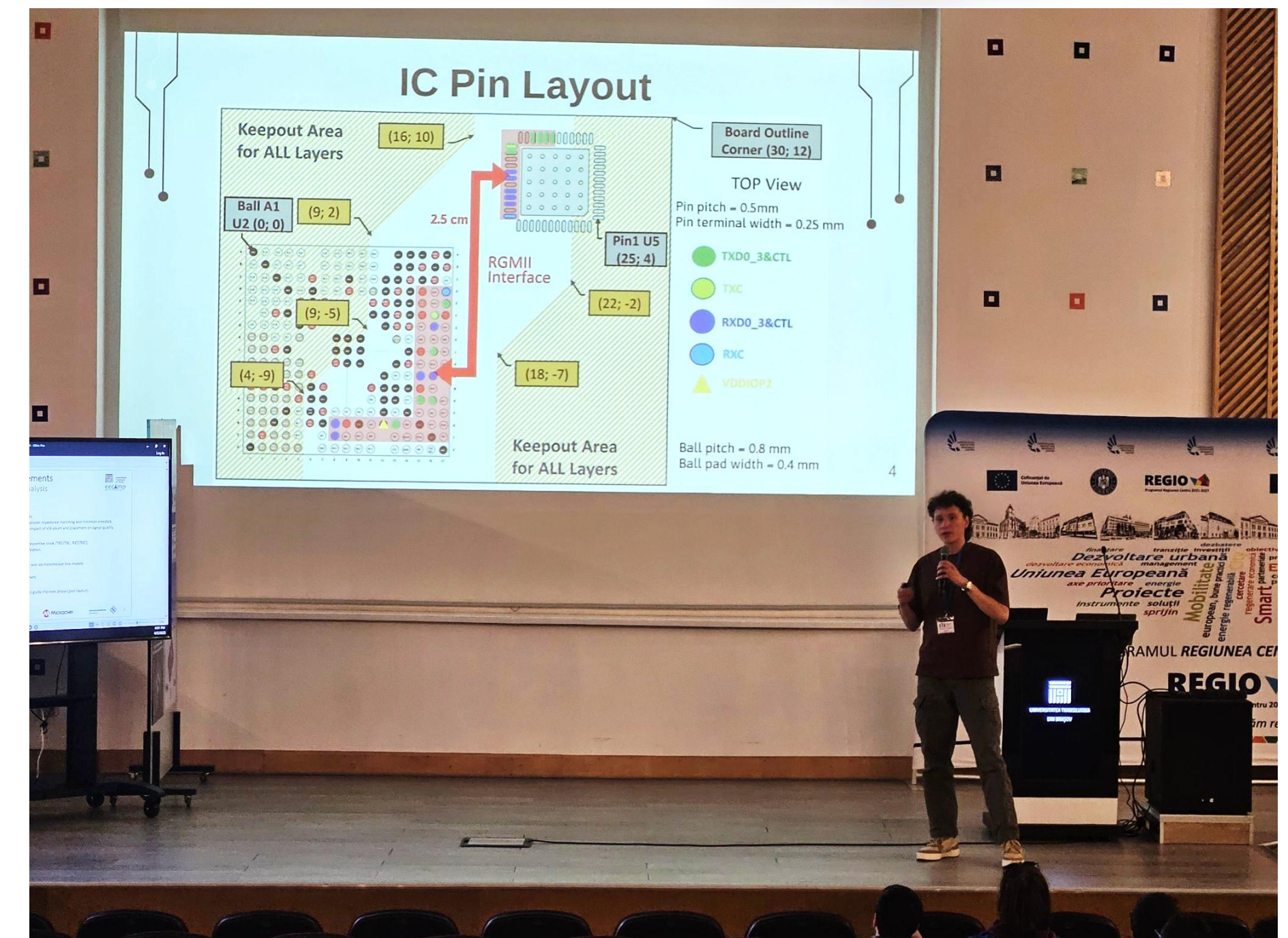
Octavian-Constantin Axinte

My work focuses on high-speed design, specializing in Signal and Power Integrity, PCB design, and fiber optic sensing.

Experience:

- TIE Participant 2024 and 2025, TIE_{E+} Winner 2025
- Research Intern VUB University Brussels (Jun 2023 – August 2023)
- Hardware Engineer at Analog Devices
- Graduate Student Assistant at TUCN

2nd year Master's student in Electronic Engineering at TUCN,
BSc in Applied Electronics at TUCN



What is TIE?

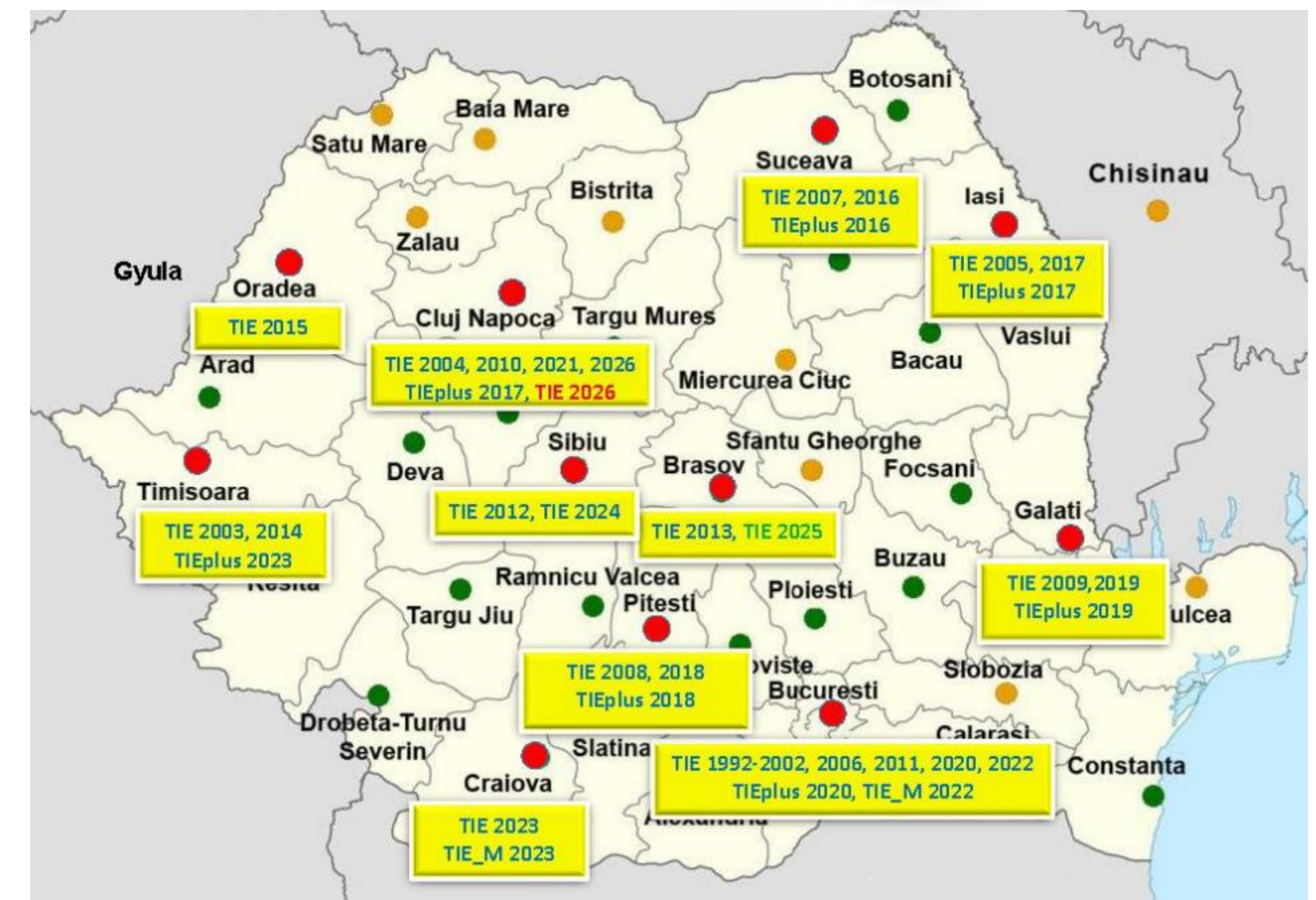
An Electronics Packaging specialized event focused on evaluation and validation of students' skills and knowledge.

Visit www.tie.ro for more details.

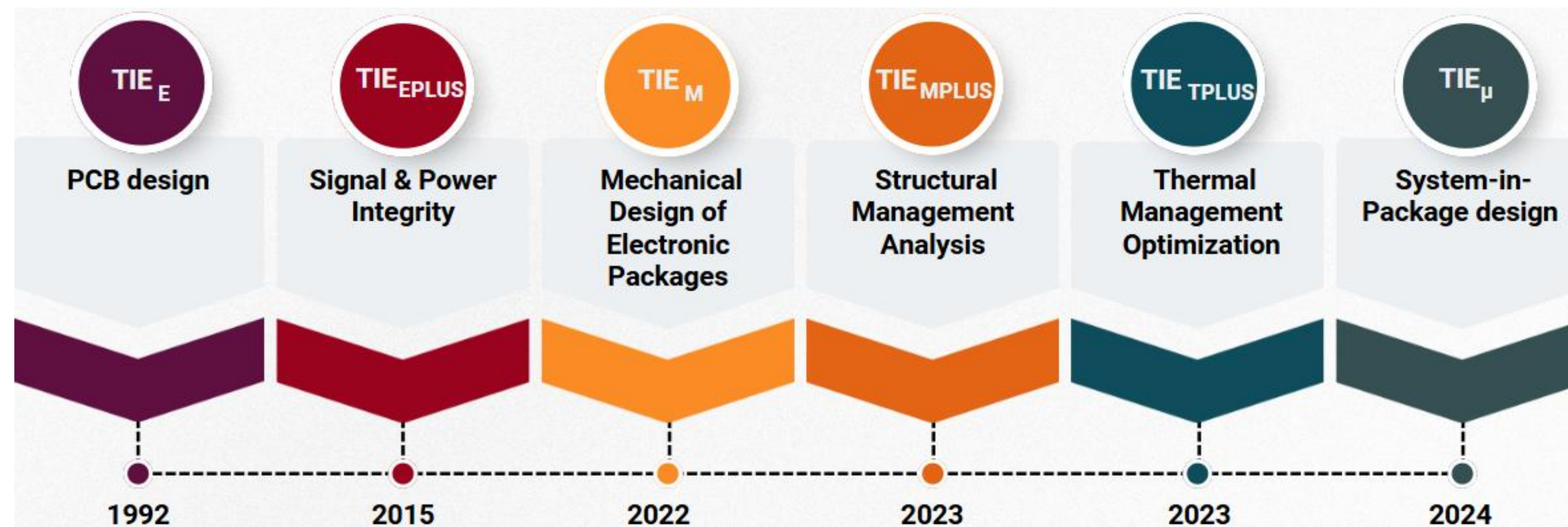


What is TIE?

- Electronic packaging industry-wide student challenge
- Strong relationship between industry and academia
- Started in 1992 → 34 editions
- Since 2011, the event language has been English
- 1500+ students (undergraduate/ master's) in the final stage from 11 universities across Romania

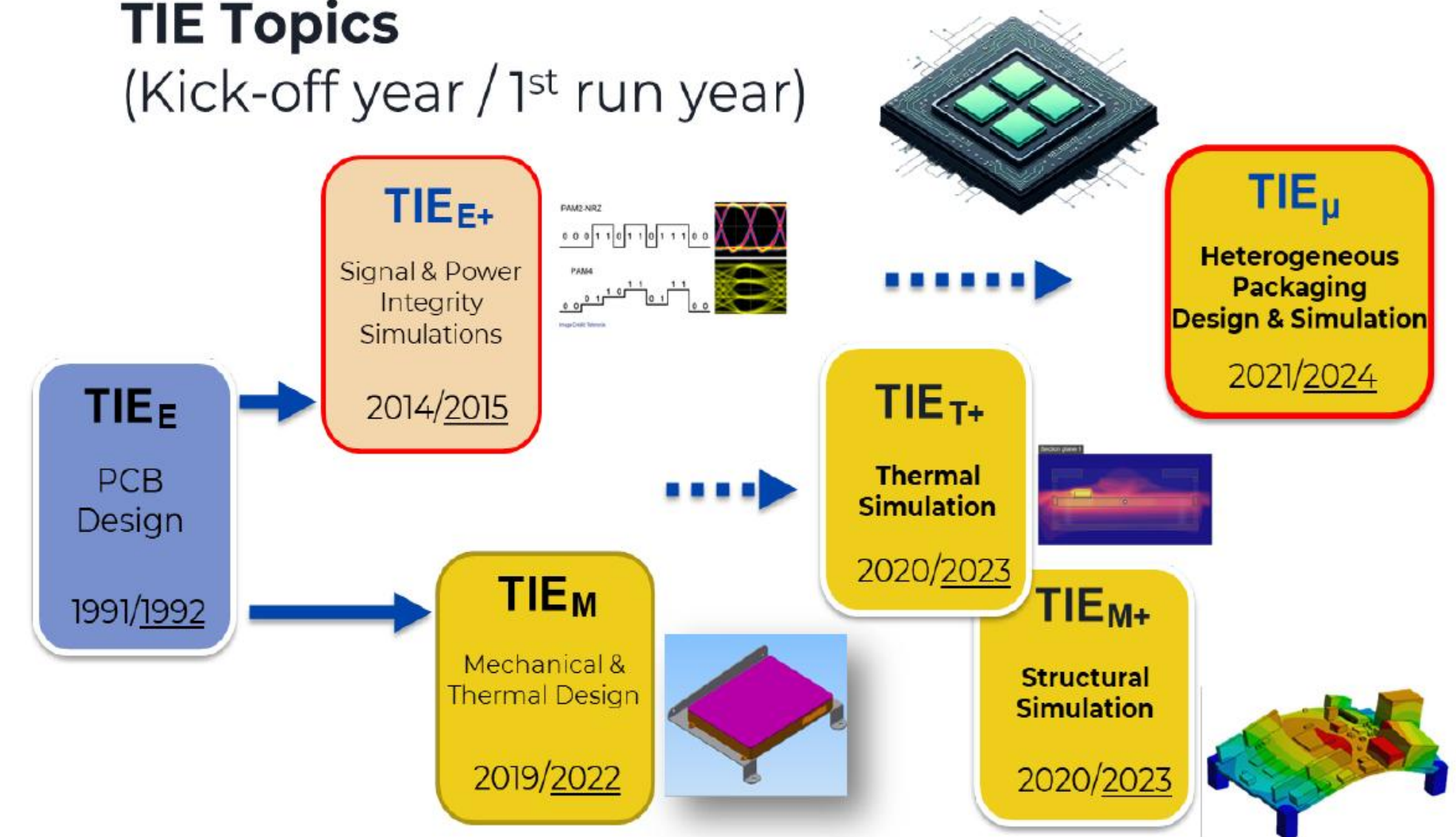


TIE Sections

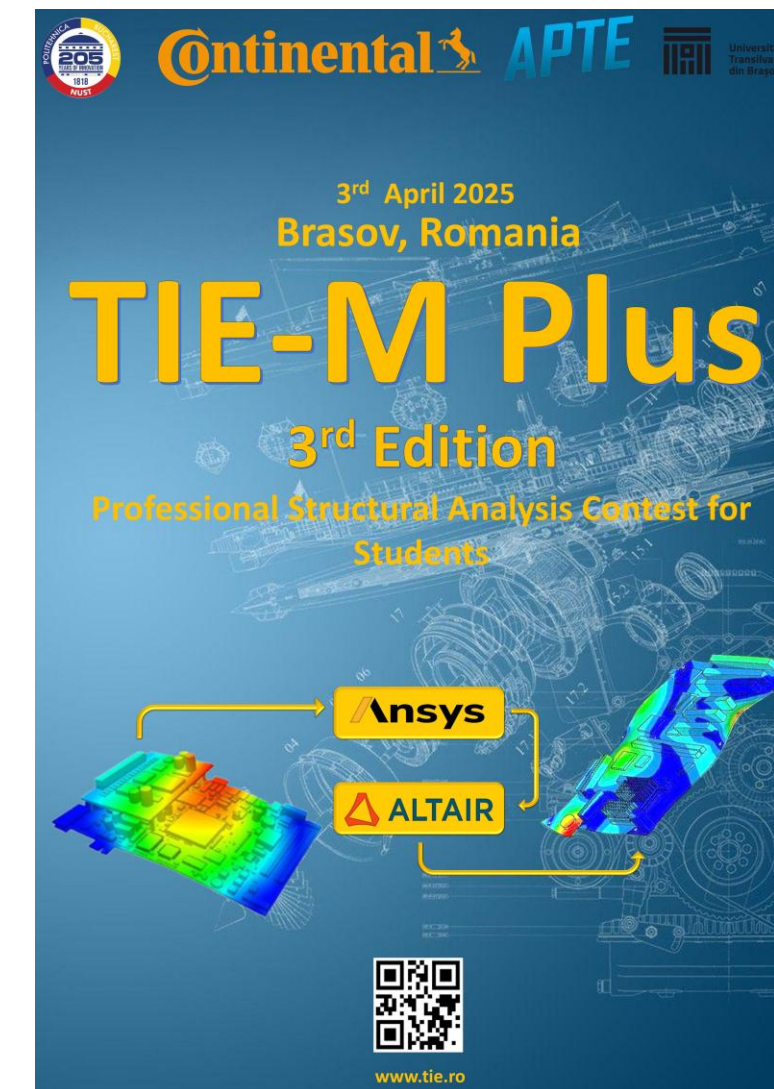


Dynamics of TIE over time

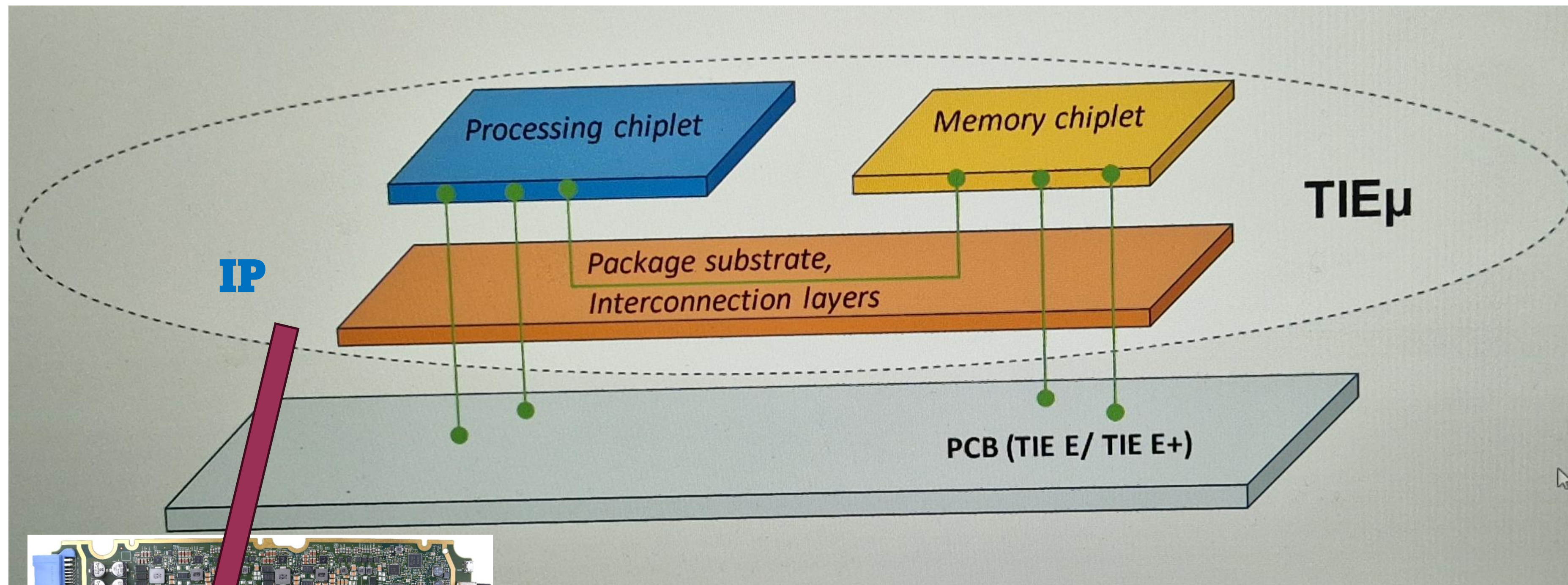
TIE Topics (Kick-off year / 1st run year)



TIE Sections



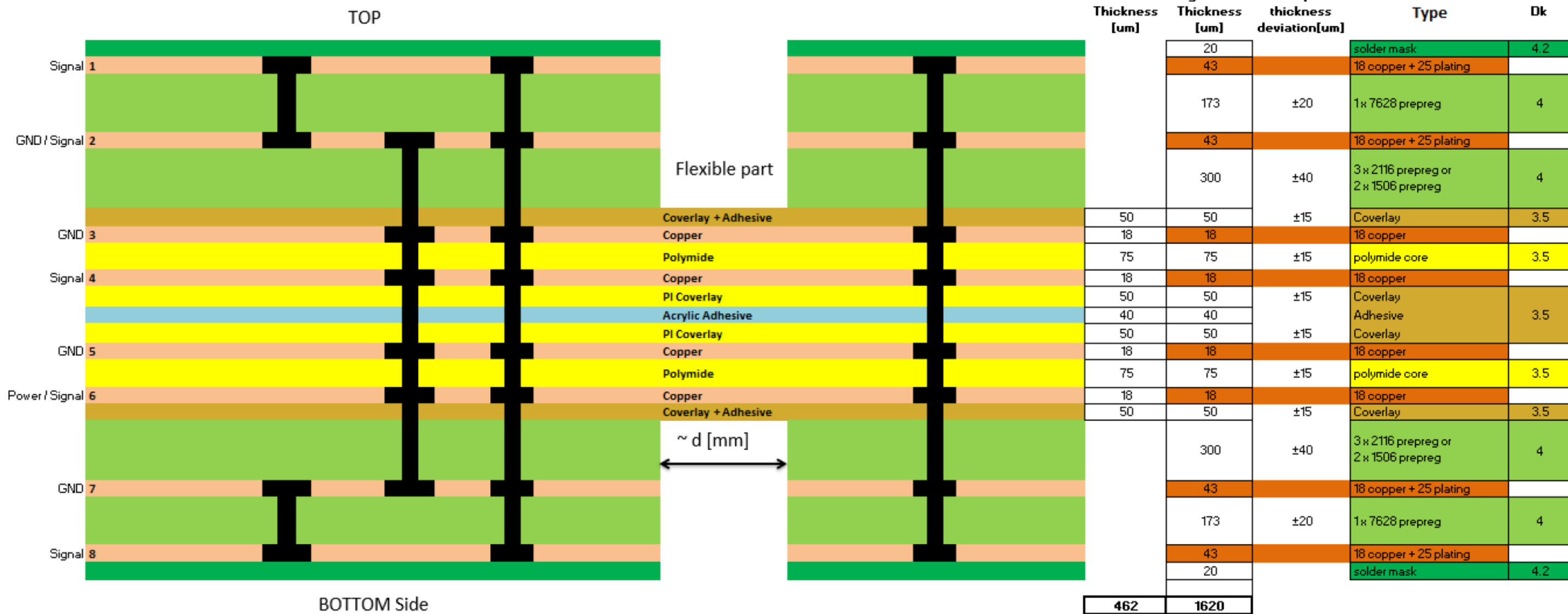
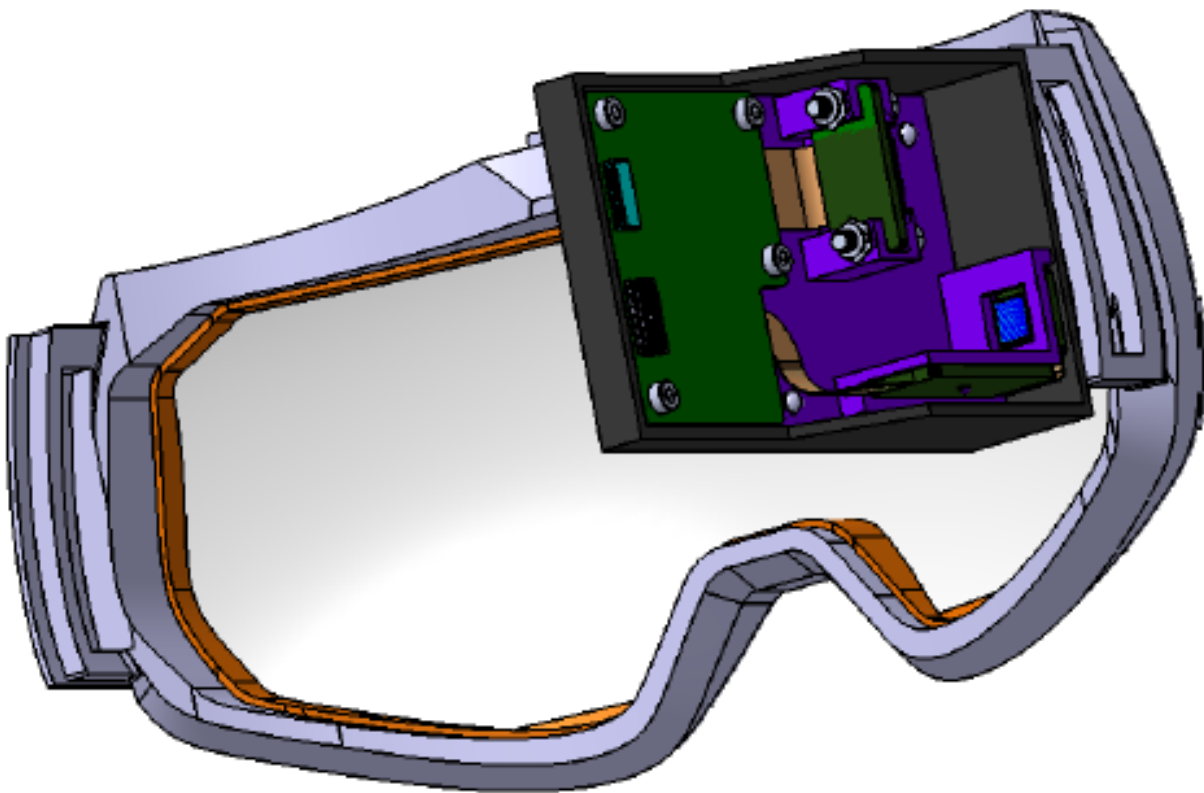
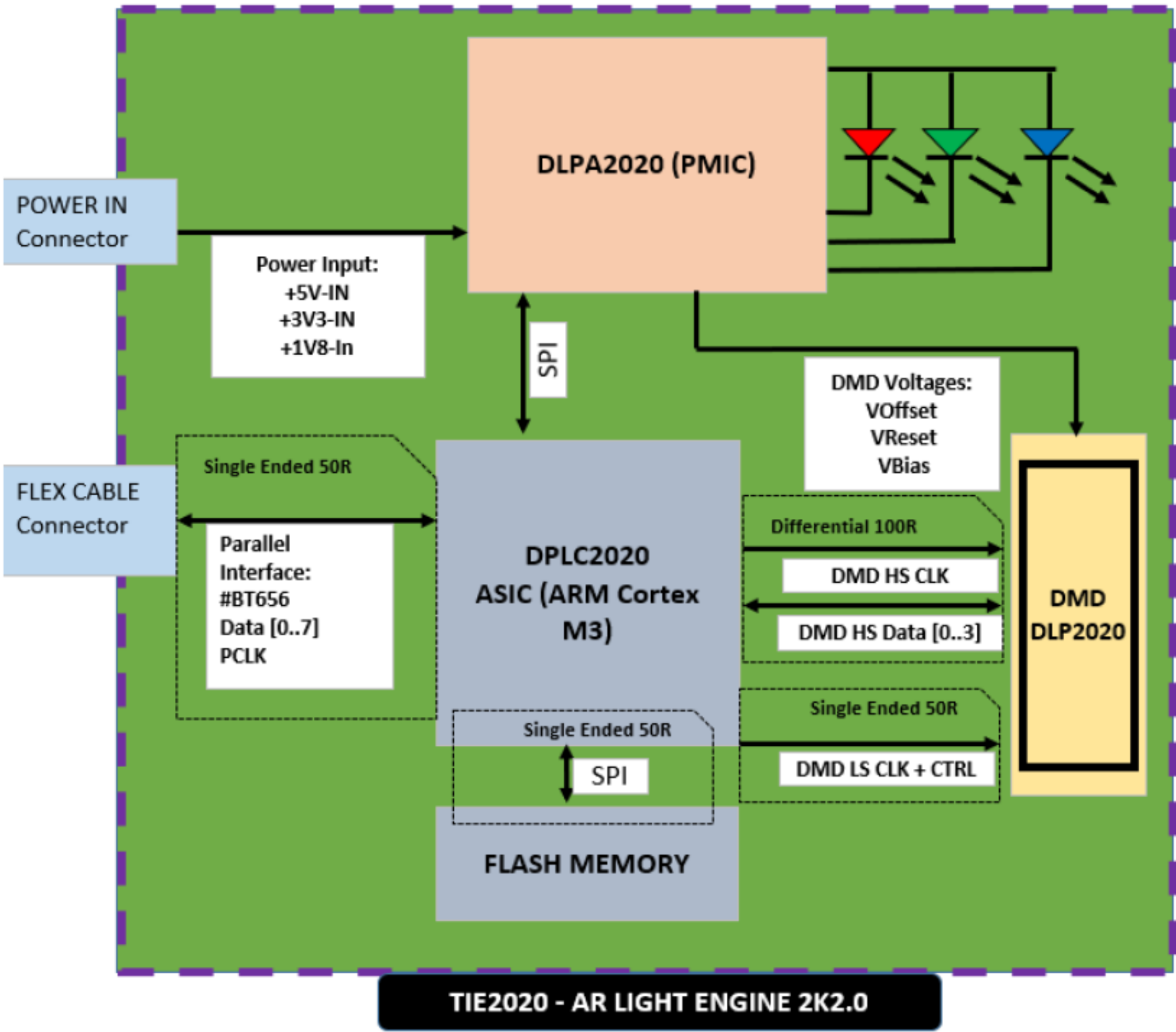
TIE Architecture



+TIE_M
+TIE_{M+}
+TIE_{T+}

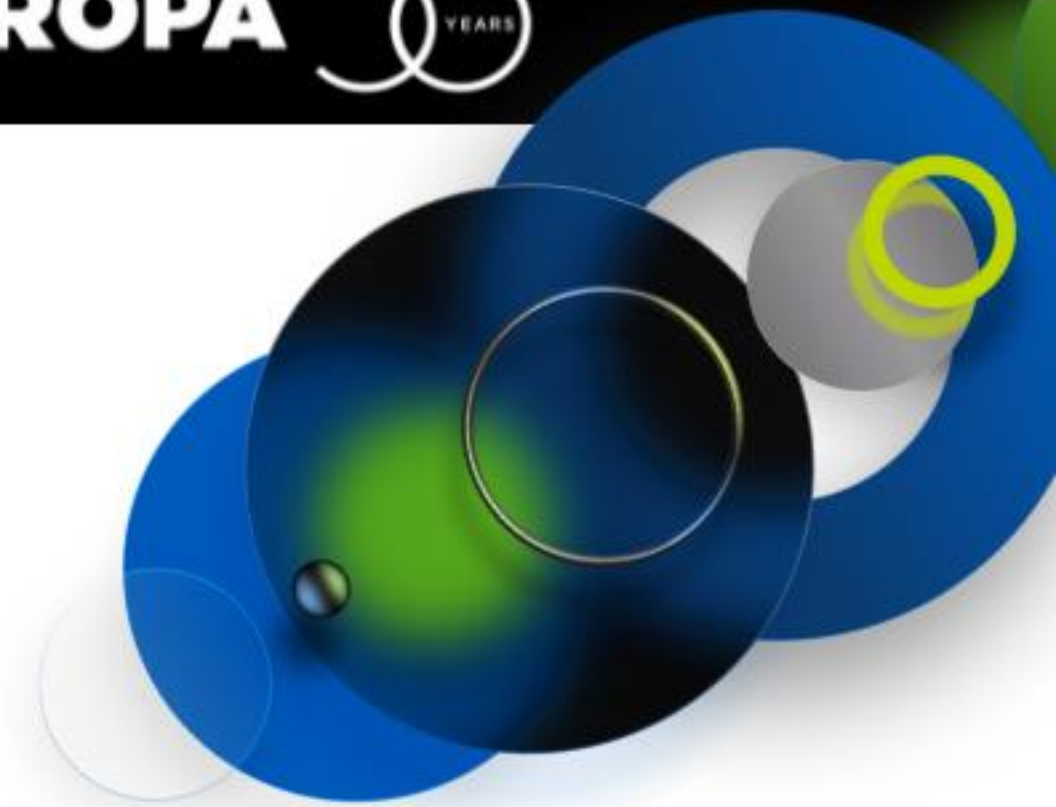
TIE Integrated Topics

TIE_E

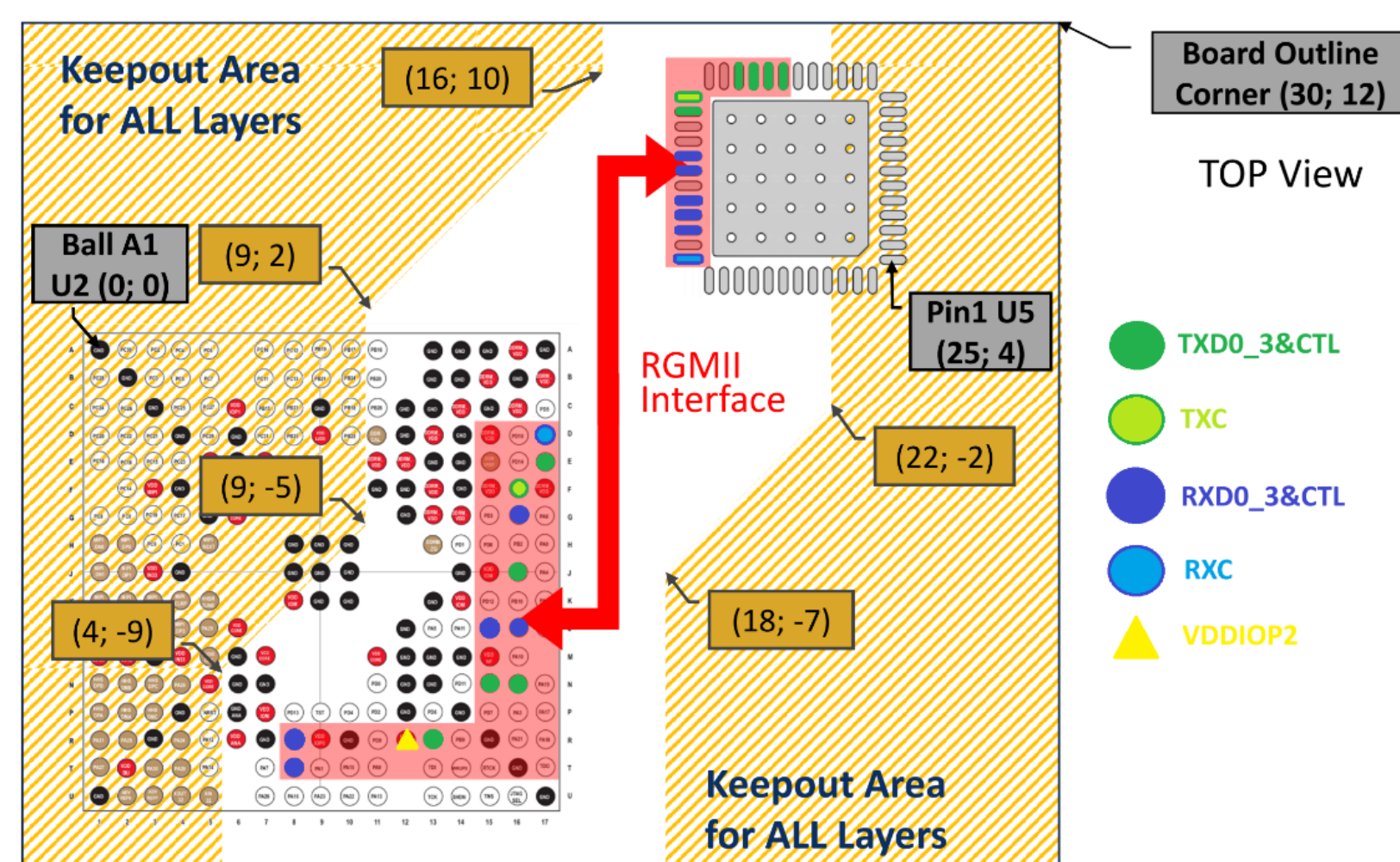


PCB Stack-up for Satellite

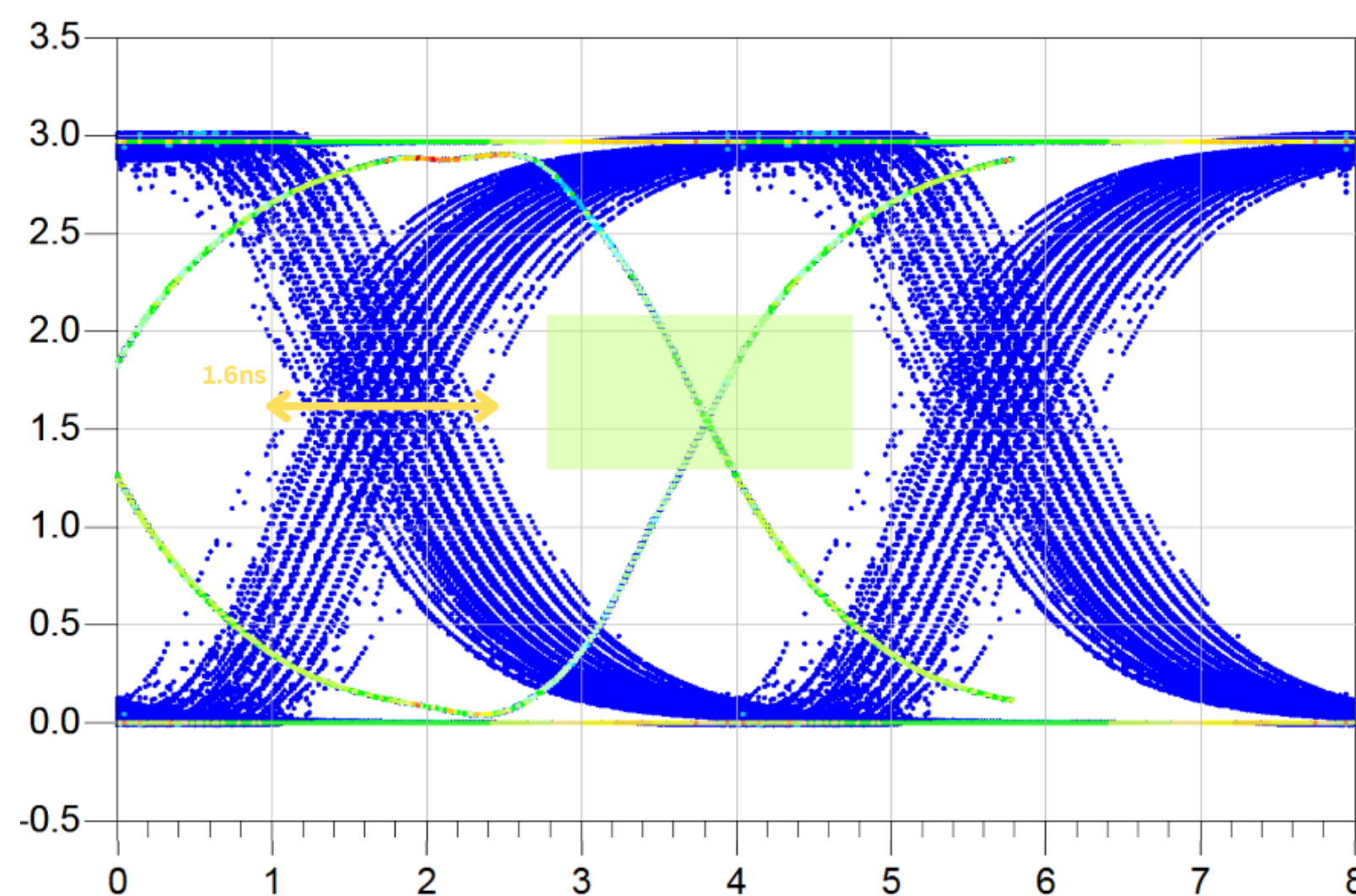
TIE_E Knowledge Evaluation & Competence Validation



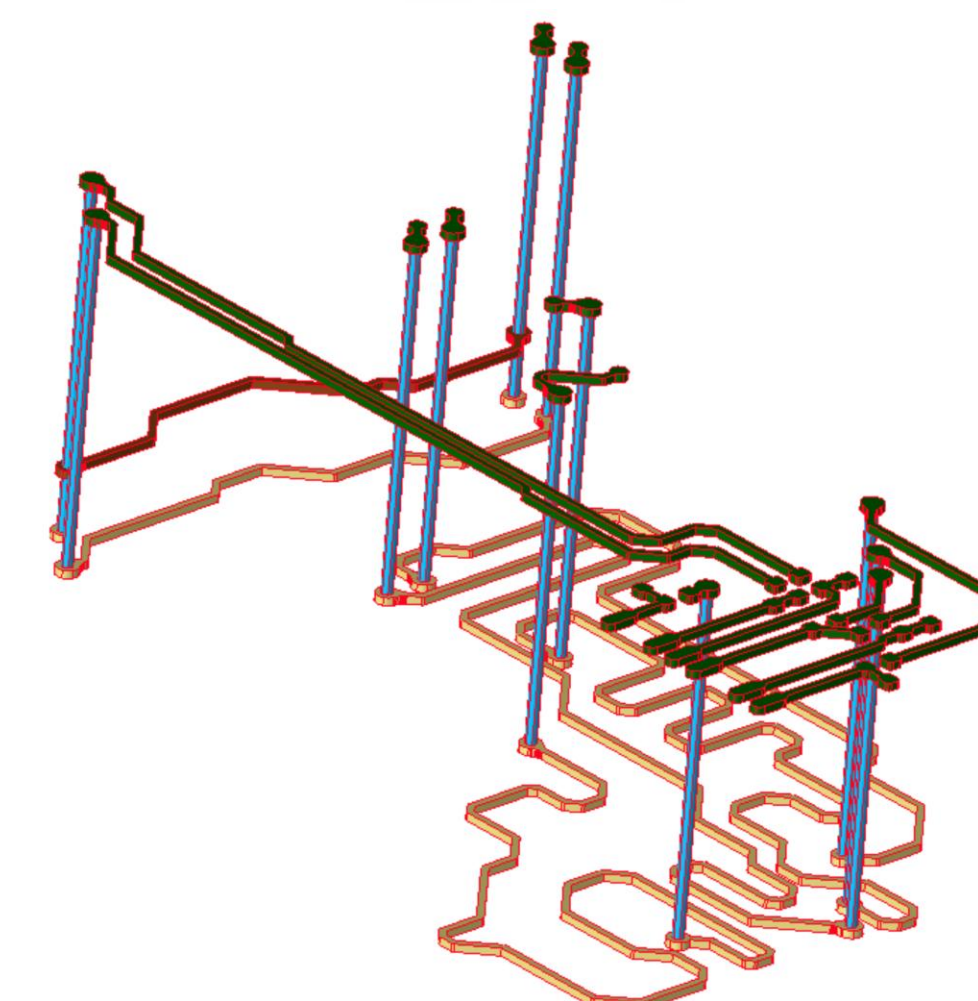
TIE_{E+}



Signal Integrity Analysis on RGMII Interface

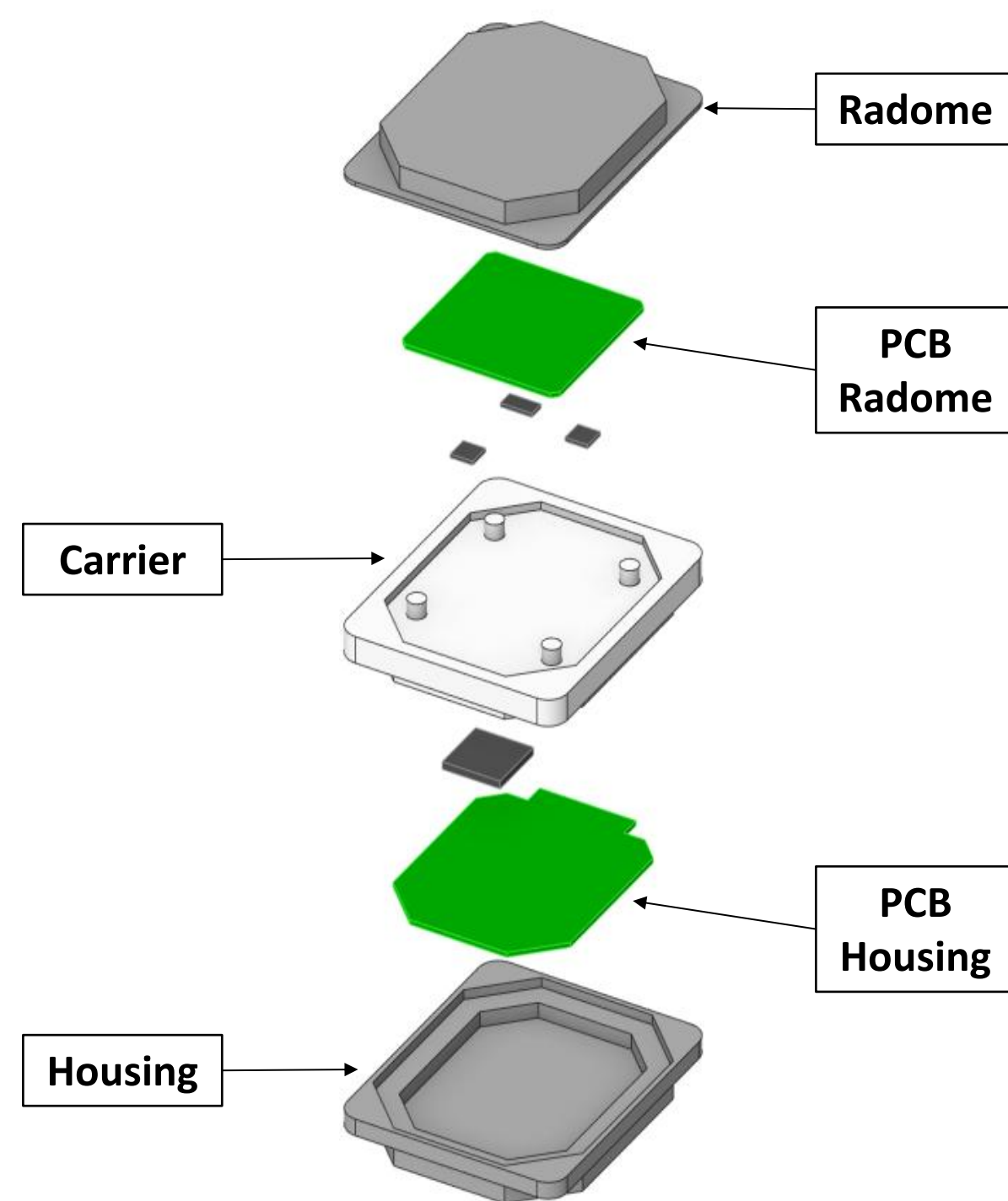


Eye diagram RXC & RTD[3:0], Minimum Case, with Mask

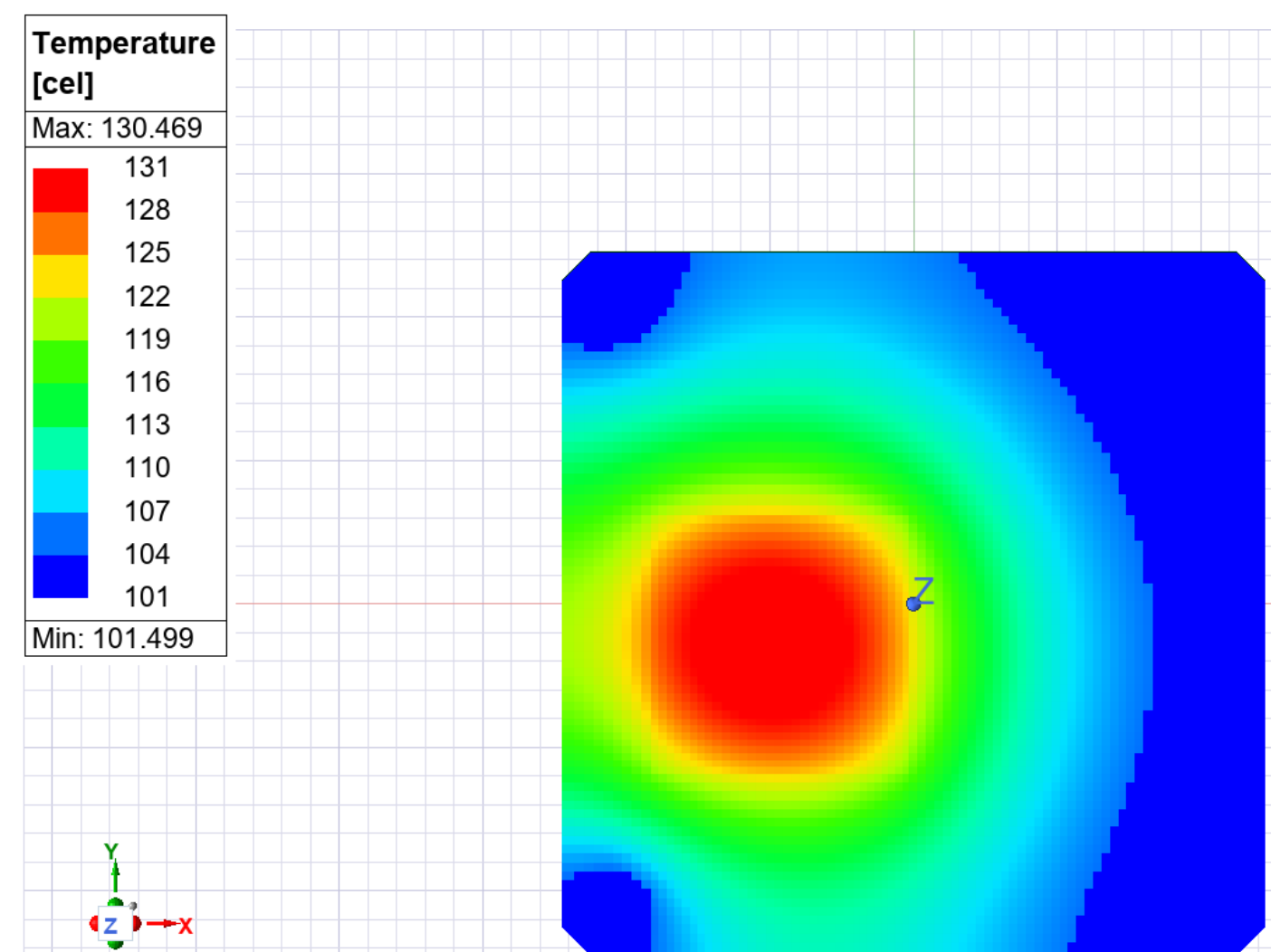


Full Analyzed Interconnect View

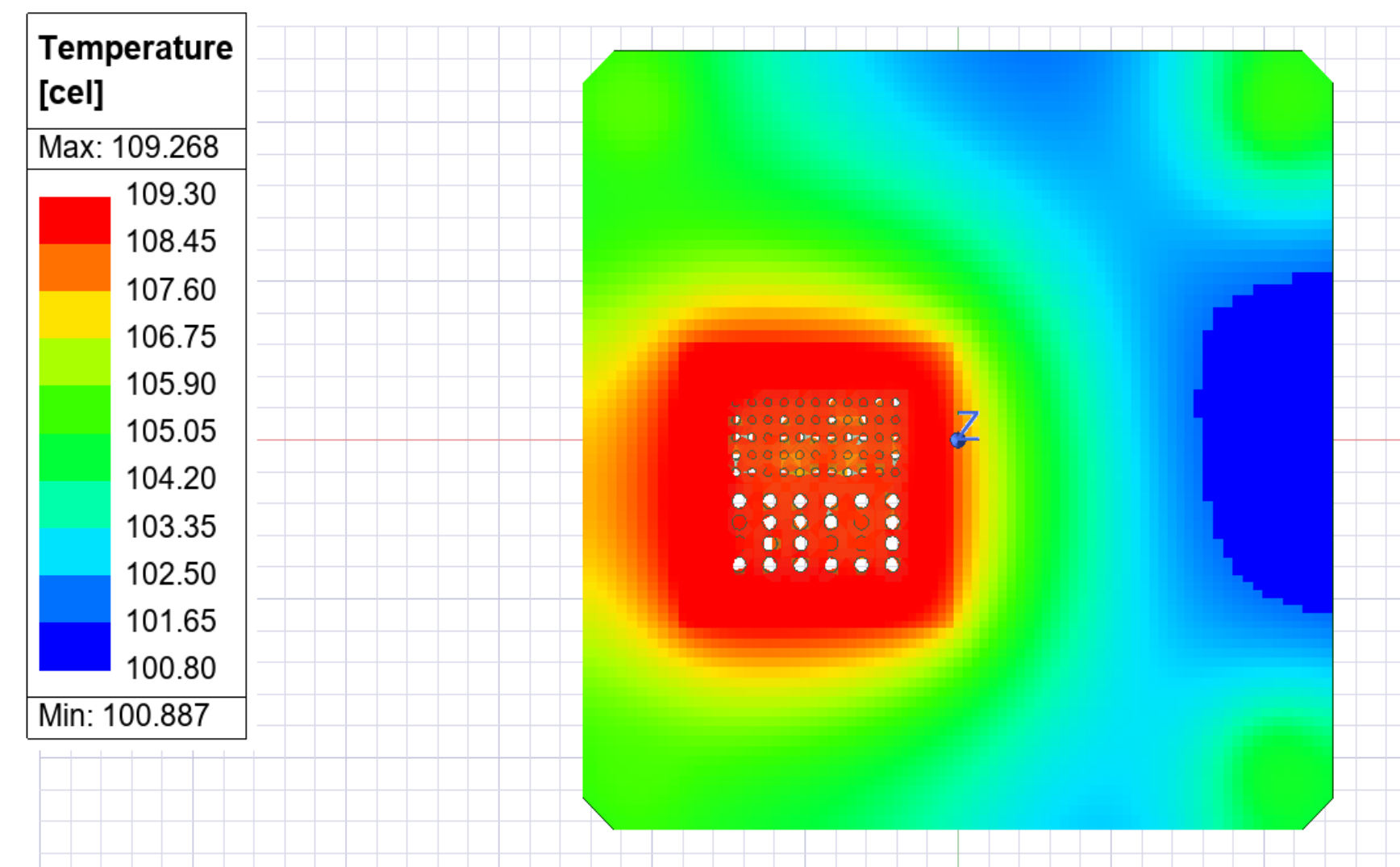
TIE_{T+}



Assembly Description

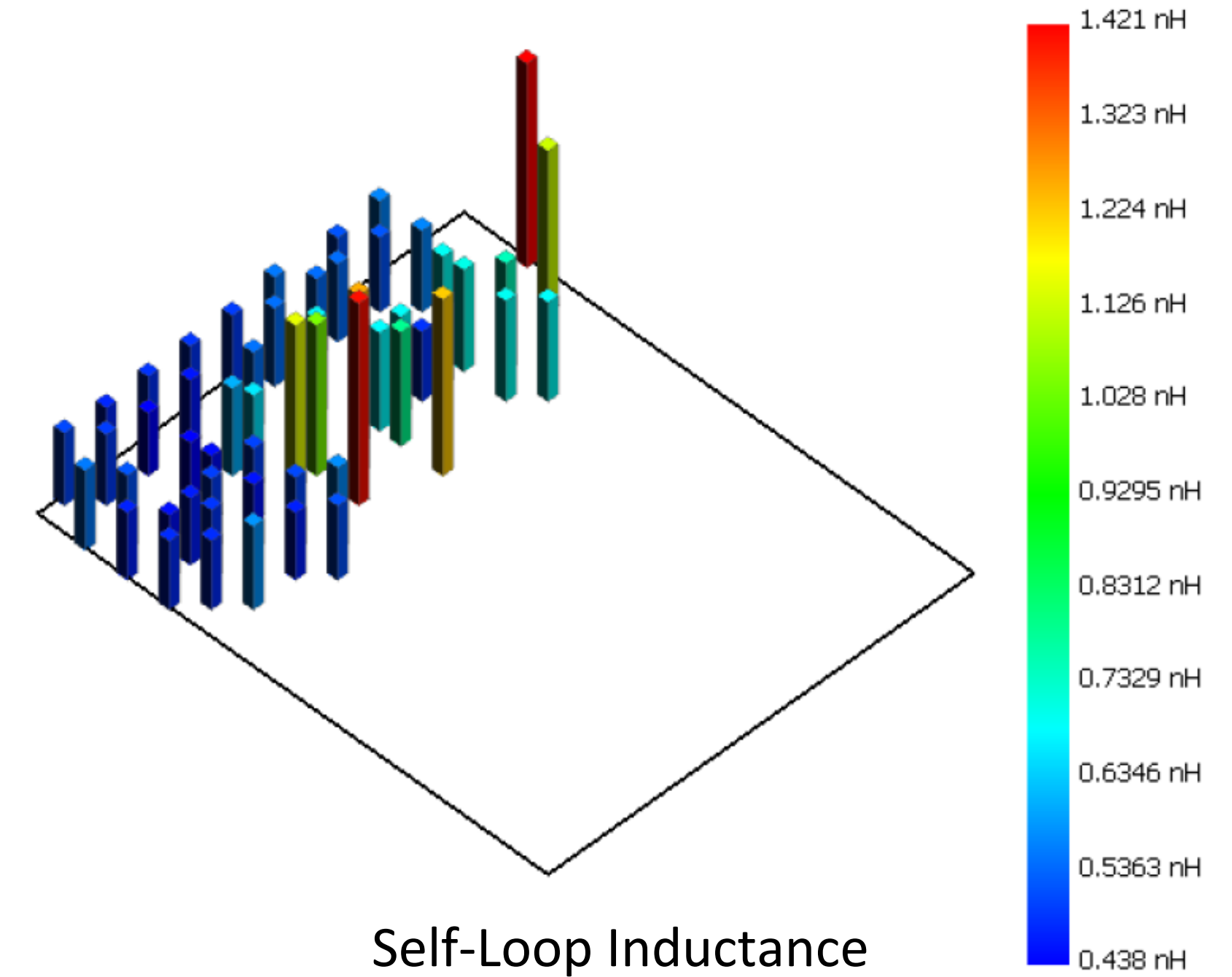
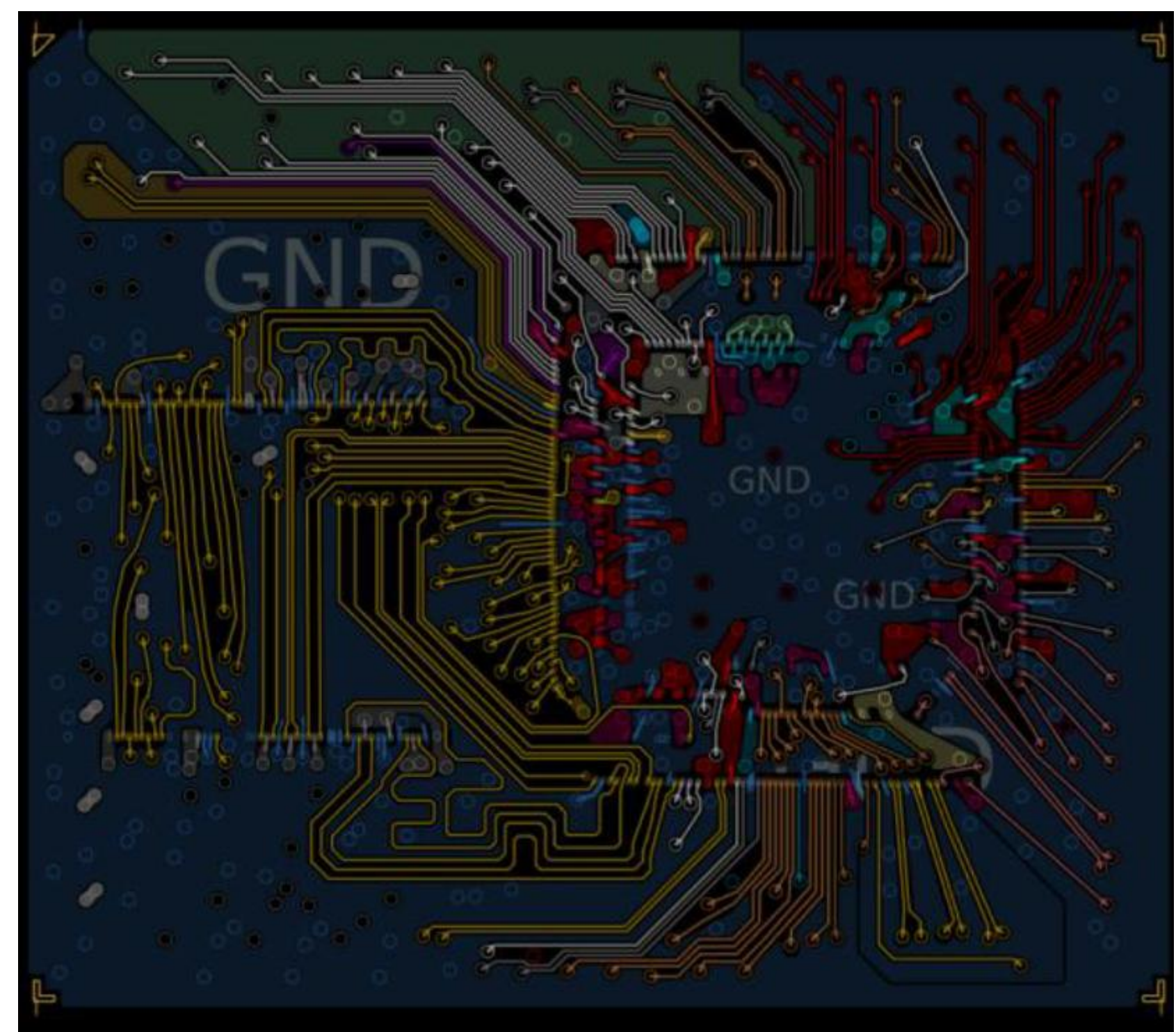


Temperature distribution in the PCB Radome BEFORE modification

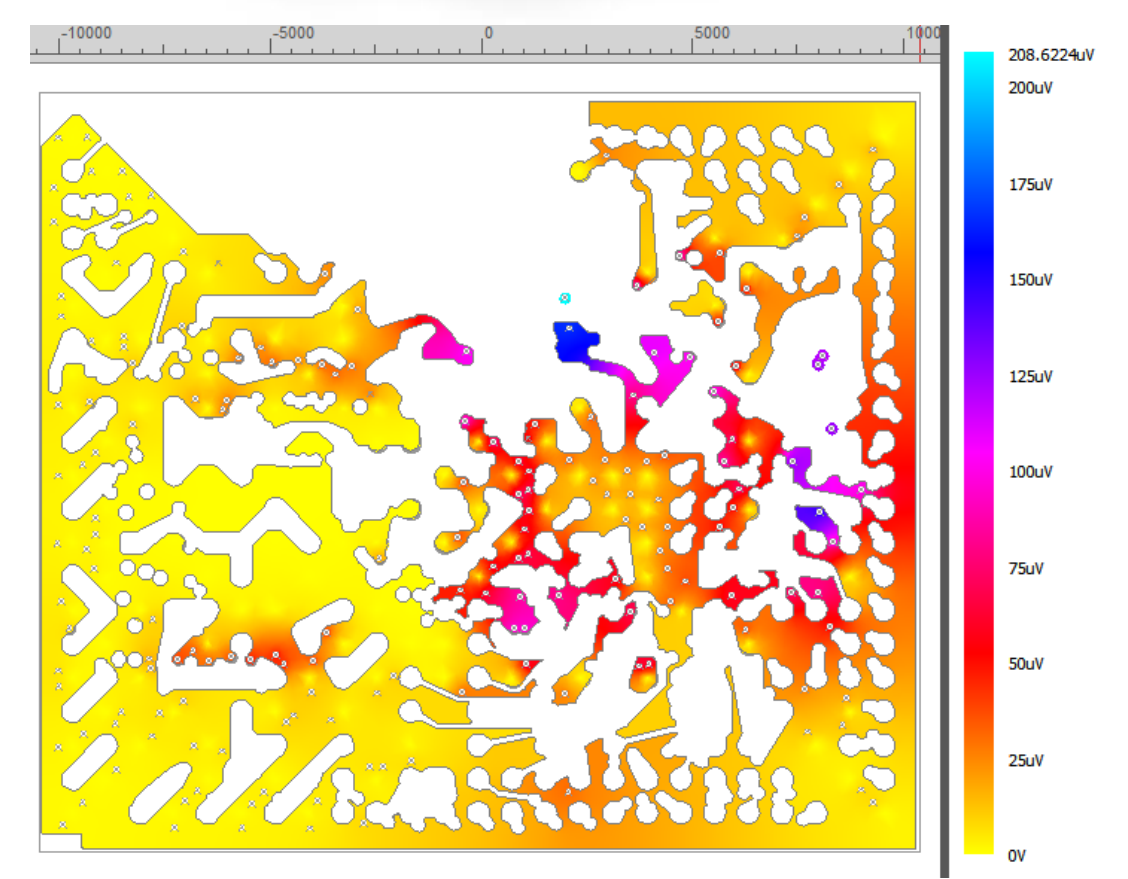


Temperature distribution in the PCB Radome AFTER modification

TIE_μ



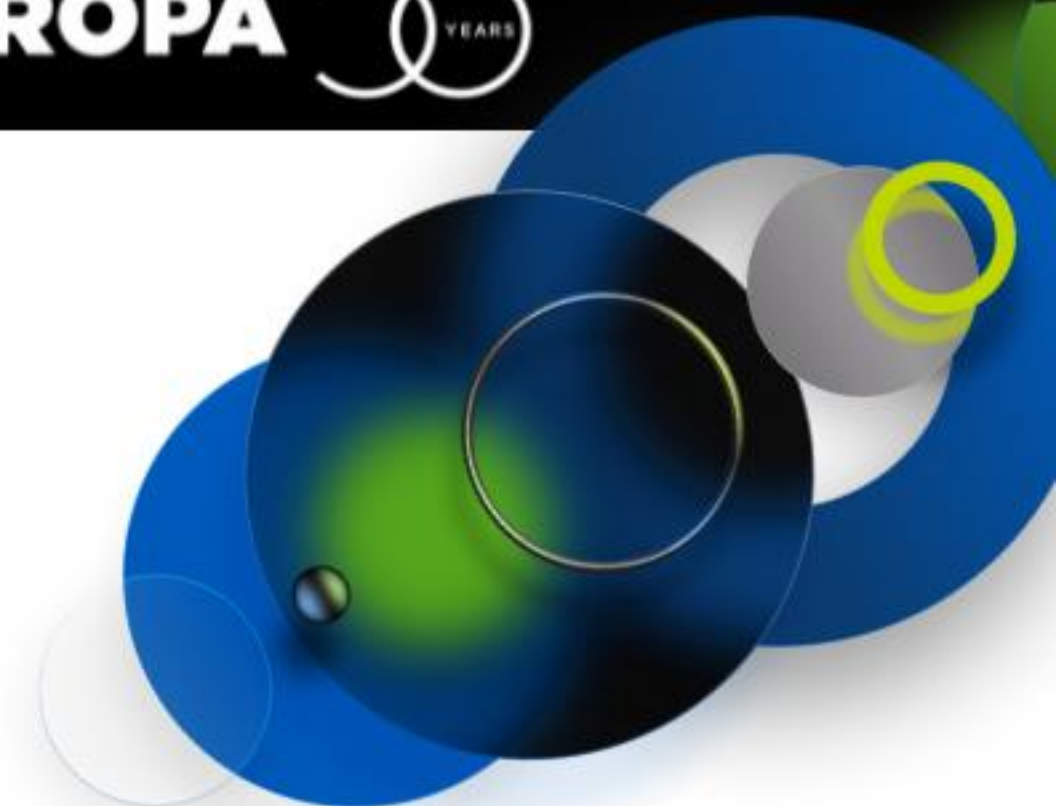
Self-Loop Inductance
Figure 25. VDD



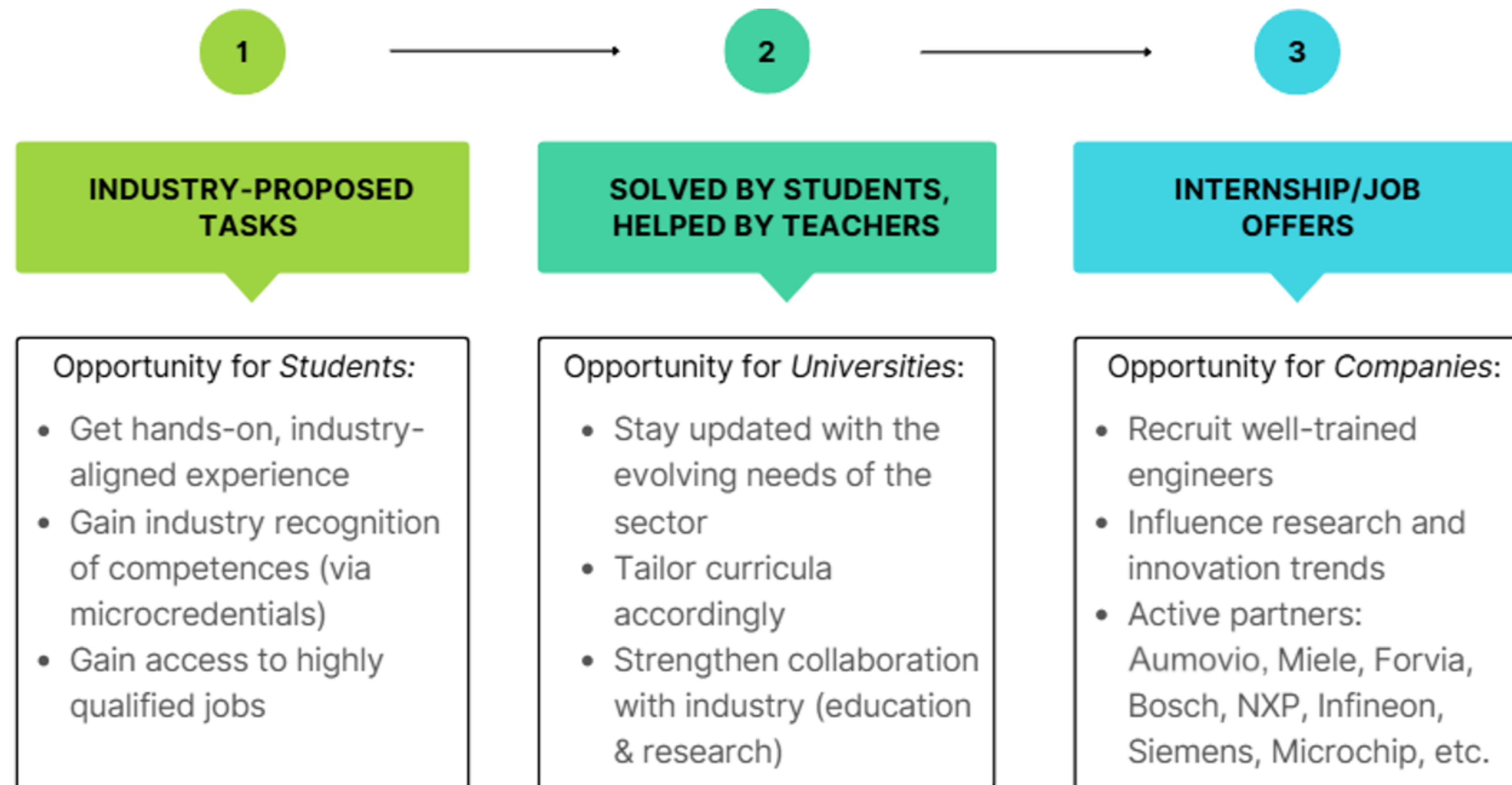
Actual Voltage (V)		Margin(%)	Positive Pin Average Voltage (V)
1.76896	✓	0.275467	1.79041
1.34363	✓	1.52781	1.34862
1.33459	✓	0.858344	1.34028
2.48442	✓	1.37664	2.49256
0.986454	✓	0.645357	0.995909

Worst Case – IR drop

TIE_μ 2025 consists of a SiP (System in Package) design, of the SAMA7G54D2G processor and the W632GU6NG DDR3 memory

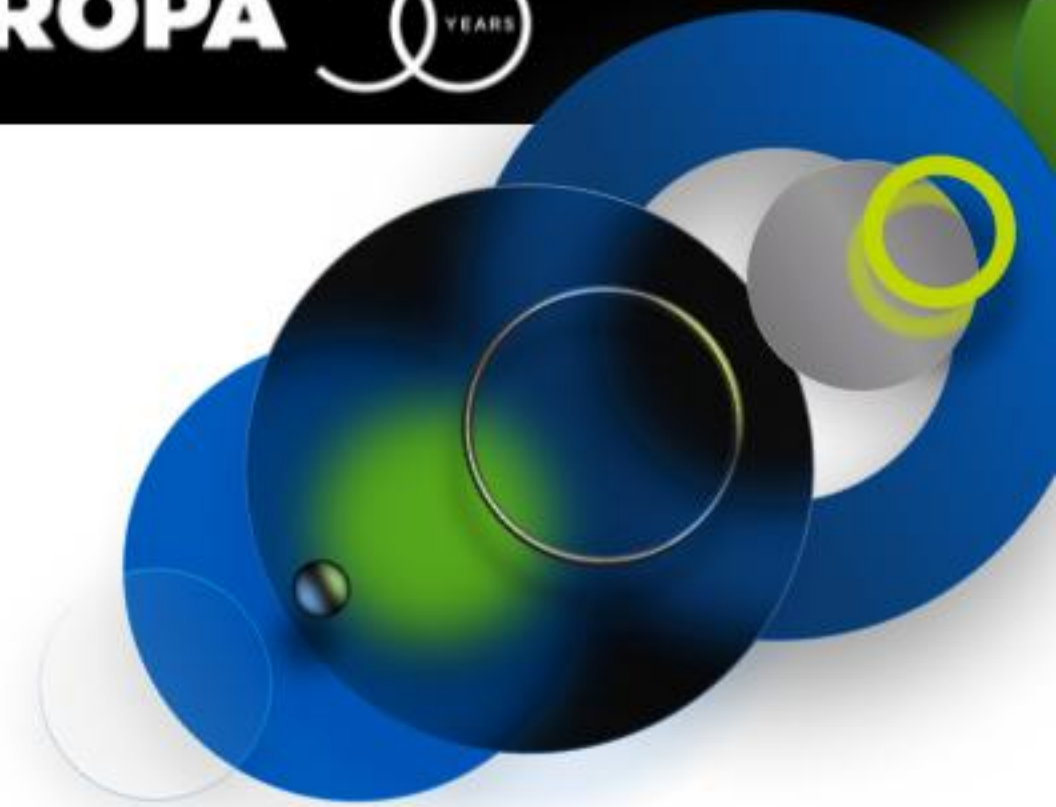


TIE – Contribution to Microelectronics Value Chain



Conclusions

- TIE is the **gateway** from **campus** to **career**, linking students with real companies, real problems and real roles.
- A close partnership between academia and industry is essential to shape the **curriculum** as the **main framework** for building a competent industry-ready workforce.
- **Industry, CAD Vendors** and **Academia** collaboration represent the **winning triangle** for shaping proper skilled workforce.



See you at TIE 2026 35th Edition
in Cluj-Napoca, Romania!

22nd - 25th of April, 2026

Thank you!

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+40748107547

