



vertical
compute

AI infra - not on a sustainable trajectory

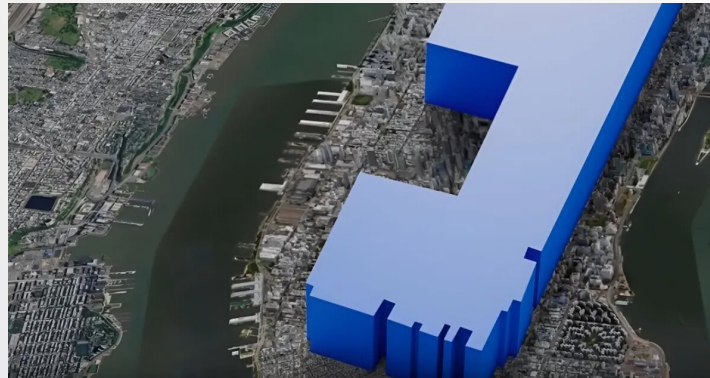
Market dominance of few players

Nvidia becomes first company to reach \$5 trillion valuation, fueled by AI boom

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[CNBC - Oct 29th 2025](#)

Manhattan-scale data centers and massive power needs



[Bloomberg - Aug. 24th 2025](#)

Helion Energy starts construction on nuclear fusion plant to power Microsoft data centers

By Stephen Nellis

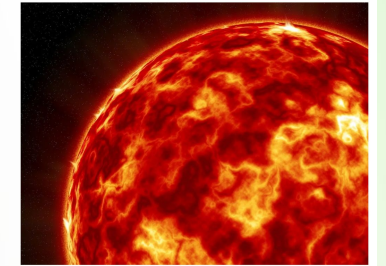
July 30, 2025 6:20 PM GMT+2 · Updated July 30, 2025



[Reuters - July 30th 2025](#)

How is Google Backing Fusion Future Data Centres?

By Ben Grasse
July 03, 2025 · 5 mins



[Datacentre mag. - July 2nd 2025](#)

AI infra becomes a societal, economic and geopolitical challenge

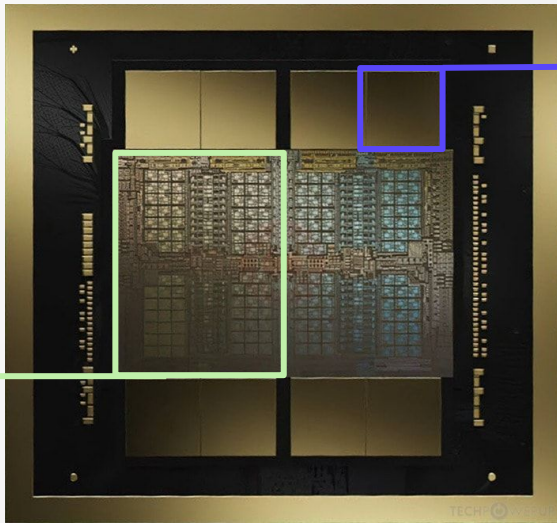
AI hardware - compute has a memory problem

GPU silicon chip

**65% of the
chip is
memory**

for the 1st gen

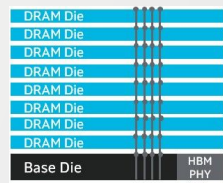
2 AI Compute dies



Nvidia B200 die shot

10,000\$ HBMs
100\$/GB

8 HBMs of 16 DRAM dies



because of that, AI is kept in the cloud,
not in customers' hand

Our solution

Magnetic Vertical **I**ntegrated **M**emory

A fundamental architecture shift reusing the best of three technologies already in mass production



Re-uses 3D-NAND fabrication processes
→ high density, cost-effective and proven.



Re-uses magnetic domain walls physics
→ fast, low energy and unlimited endurance



Delivered as 3D chiplets
→ high bandwidth, modularity & scalability

our secret sauce:

100s of bits stored
in vertical magnetic wire
read at nanosecond speed

Density (0.5 ~30 Gbit/mm²)

Energy (no refresh, 0.2 pJ/bit)

Performance (2~10ns latency)

Endurance (unlimited)

Retention (years)

High temp support (>125 degC)

40X cheaper than SRAM

20X cheaper than DRAM

1

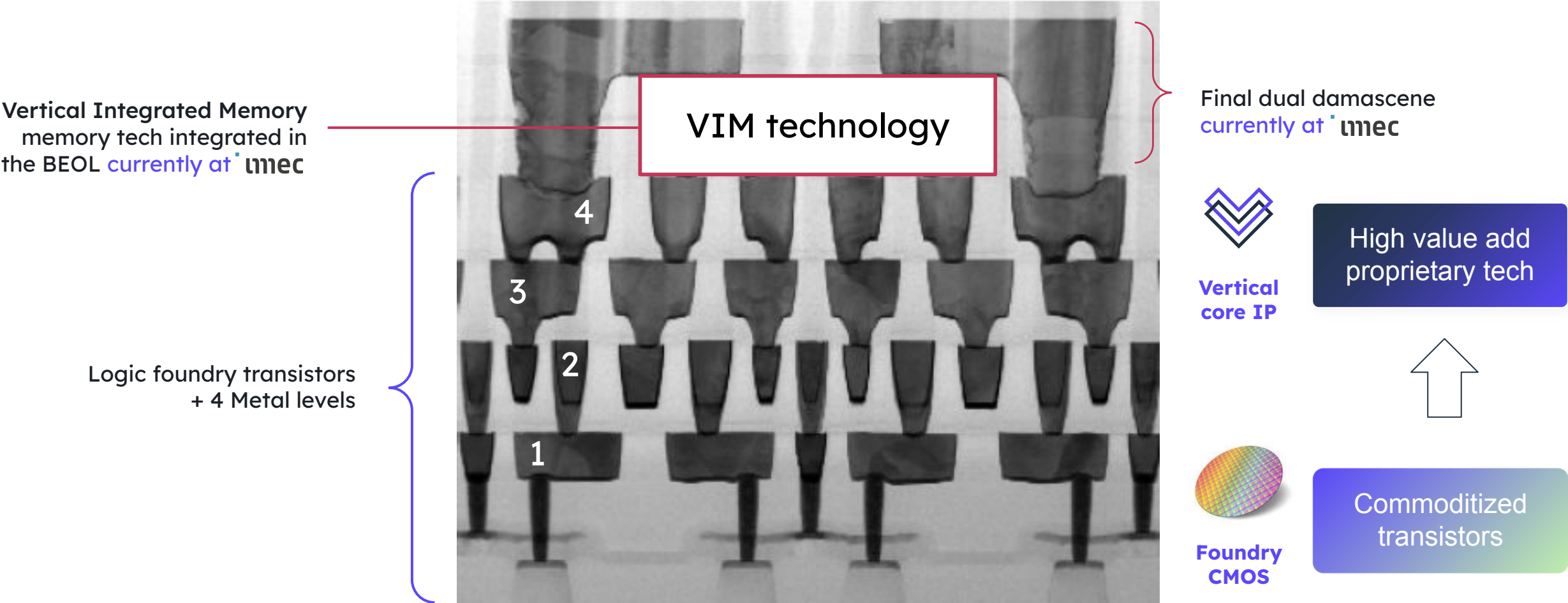
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1

0

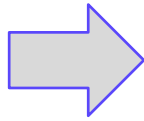
1

seamless integration on transistors



BEOL: Back-end of the line - the Cu connections part of CMOS process

manufacturing opportunity in the EU



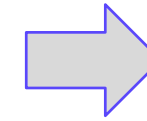
The funnel

300mm R&D (almost any tech possible)

Going towards prototyping lines



No high volume production capabilities



The business(es)

Back-end FAB

Back-end foundry for profit business model

Avoid re-inventing the transistor
Transistor wafers become commoditized

High value added, unique tech, is produced and remain in Europe

Relative smaller capex than full fledge transistor fab, easier and faster to deploy

Adv. packaging fab

2.5D & 3D capabilities built on EU expertise

Integrate new tech in advanced systems

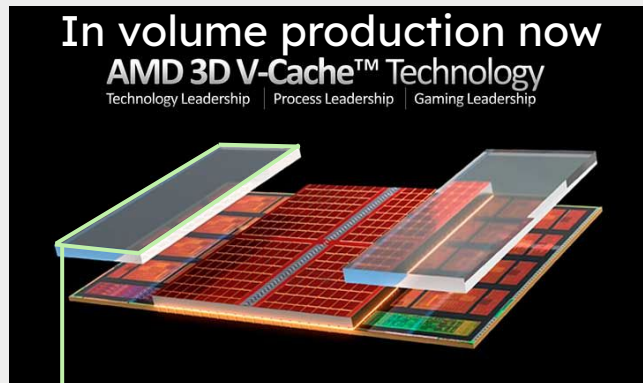
AI
Automotive
Defense
Client
Robots

Go to market product

Breaking the memory wall with a VIM 3D chiplet

Reference product - exists today

AMD 3DVcache 3D chiplet

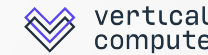


64 MB SRAM

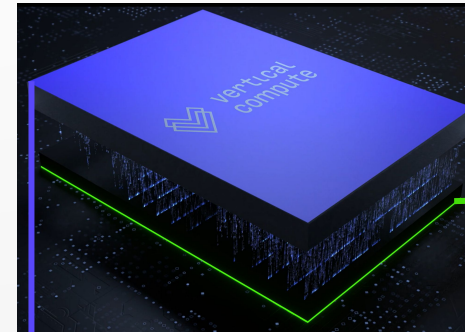
TSMC N7 optimized (reduced BEOL)
9um Cu-Cu hybrid bonding
> 16K TSV connections @ 1.5GB/s

x50
for the 1st gen

First volume product in 2028



VIM 3D chiplet



5 GB VIM

N7 (integrated in BEOL)
Hybrid bonding

Targeted customers

AI compute (N5-N2,...)
Automotive (N28-N7, ...)
Mobile & client (N16-N2, ...)
Defense in-field context gen (...)



now AI can run in customers' hand
and save AI infra challenges

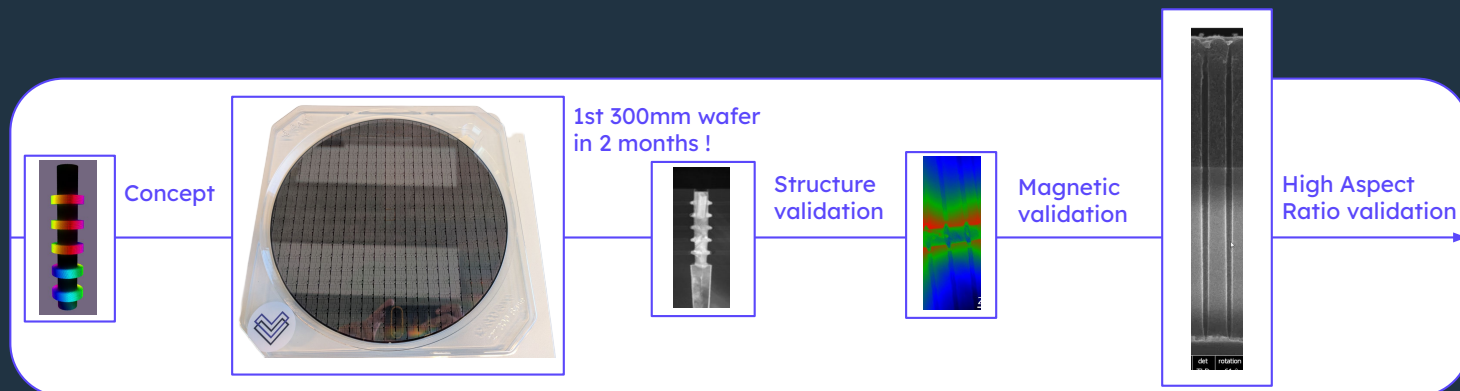
First tech unlocks – it is all about fast execution

Operations launched
(Imec spin-off)

Dec. 24

Pre-seed raised
at inception

€20M



Technology Readiness Level 1

Basic Principles observed



Technology Readiness Level 5

Technology validated in lab in relevant environment (tools, foundry, process)

Wafers successfully
produced & tested

100

Patent
portfolio

16

Proof of Concept
vertical memory
elements de-risked
(write/push/read)

Q3-25

Test-chip design
layout tape-out
(TSMC+imec)

Q4-25

The team

Sylvain Dubois

CEO & Co-founder

- Experienced semiconductors business exec
- Ex Advanced Technology sourcing @Google
- Early employee and VP @Crossbar (\$136m raised)
- **+20 years exp** in semiconductors



Sebastien Couet

CTO & Co-founder

- Worldwide expert in magnetic memory
- Ex Program Director magnetics @Imec
- **PhD in nano magnetism** (140 papers, 18 patents)
- **+15 years exp** in magnetic memory



BOARD OF DIRECTORS

Chairman of the board | **Christophe Frey**

Managing Director @ARM, France & Germany, VP EU partnerships

imec

imec xpanse

EURAZEO

XAnge
/ Siparex Group

VECTOR GESTION
30ans 1994—2024

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AMD Senior Fellow, 3D-Vcache SRAM chiplet architect



Pierre Fazan

Ex Micron Fellow, Innovative Silicon CTO



Eric Beyne

Imec Senior Fellow 3D Integration

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→ Senior Director HGST
@Western Digital



Luc Thomas

Head of technology

→ Senior Director @Applied
Materials

→ Principal @Headway



Virgile Jarveliac

Head of chip design

→ Founder @Neurxcore

→ Memory design @ARM



Vincent Huard

Head of Product

→ CTO @Dolphin Design

→ Manager @ST Micro



Catherine Van Begin

Head of people

→ HR @EMAsphere

--> Team members in Belgium & France

25

Next steps - tech dev, product



2025

Launch & build

€20m in pre seed funding

25 TEAM MEMBERS

Consolidation of IPs portfolio
(1 acquisition)

PoC of vertical memory elements
(write/push/read)

Test-chip design tape-out finalized



2026 - 2028

Partnership & acceleration

€30m in seed funding

+40 TEAM MEMBERS

MVP - First selling product
(50x SRAM density)

- finished wafers compute & logic
- full characterisation array
- Eval kit

First partnership signed
with low volume back-end fab

Strengthening of the IPs portfolio

International expansion US/Asia

Manufacturing optionality
verticalfoundries in the EU



2028 - 2030

DRAM MARKET (\$)



200B

DRAM chip 3GB
at 0.3Gb/mm²

HBM MARKET (\$)



100B

8 x 16 DRAM chips
at 0.3Gb/mm²

VALUE PROPOSITION



100x

VIM chip 5GB+
at 30Gb/mm²

DENSER THAN DRAM
FOR HIGH VOLUME PRODUCTION



vertical
compute

CONTACT

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