



Cesar RODA NEVE
R&D Program Manager

III-V Engineered Substrates, beyond classical SOI substrates

SEMICON EUROPA (MUNICH) | 18th Nov. 2025



AGENDA

SUBTITLE GOES HERE

SOITEC INTRODUCTION	01
SOI SUBSTRATES	02
III-V ENGINEERED SUBSTRATES	03
Key Messages	04



SOITEC IN NUMBERS

IN OUR SOIL GROWS AN AMAZING FUTURE



1992

Soitec is founded

531

Patents filed worldwide each year

4,300

Active patents

17,1%

of revenue dedicated to gross R&D

2200

Employees (35% women)
industry average 20-25%

€891M

Revenue (Fiscal year 2025)

SOITEC in the value chain of the semiconductor industry

EXPERTISE FOR 3 MAIN MARKETS



**BULK
MATERIALS**



soitec
TECHNOLOGY EXPERTISE



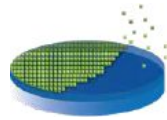
Smart Cut™



Interface
engineering



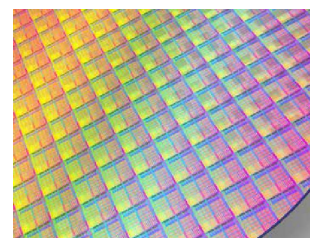
Compound



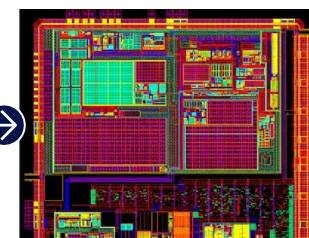
Epitaxy



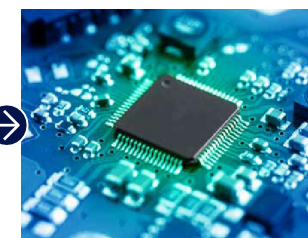
Engineered
substrates



FOUNDRIES



DESIGN



FABLESS



MOBILE
COMMUNICATIONS



AUTOMOTIVE
& INDUSTRIAL



SMART
DEVICES

GLOBAL PRESENCE & INDUSTRIAL STRENGTH

SOITEC FOOTPRINT



150mm

200mm

300mm

SOITEC BERNIN FRANCE

B1 : SOI 200mm
IATF 16949

B2 : SOI 300mm
IATF 16949

B3 : POI 150/200mm
LNOI 150mm

B4 : SmartSiC
150/200mm
SOI refresh 300mm

>20 years of high volume manufacturing experience - Site ISO 9001:2015 certified



200mm

SIMGUI SHANGHAI (Partner) CHINA

SOI 200mm

Site IATF 16949 certified

SOITEC BESANÇON FRANCE

POI SAW filter pilot line

Site ISO 9001:2015 certified



150mm

200mm

SOITEC BELGIUM N.V. HASSELT BELGIUM

GaN Si GaNSiC 150/200mm
Site ISO 9001:2015 certified



300mm

SOITEC PASIR RIS SINGAPORE

PR1 : SOI 300mm

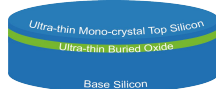
Site IATF 16949 certified

SOITEC PRODUCTS PORTFOLIO

MOBILE COMMUNICATIONS

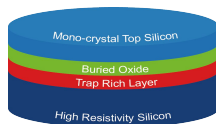
Connect FD-SOI

Highly efficient mmW RFFE



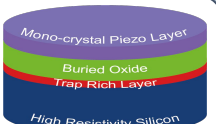
Connect RF-SOI

Highly efficient mobile communication



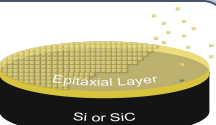
Connect POI

High performance 5G filters



Connect GaN

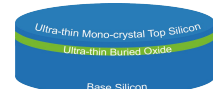
High performance power amplifiers



AUTO & INDUSTRIAL

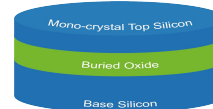
Auto FD-SOI

MCUs, ADAS-Radar
ADAS-Vision



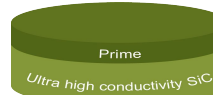
Auto Power-SOI

Power management IC,
In-vehicle netw. & gate driver



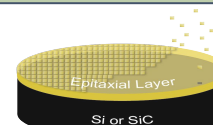
Auto SmartSiC™

Automotive electrification



Auto GaN

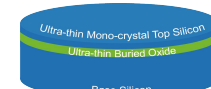
DC-DC 48V converters



EDGE & CLOUD AI

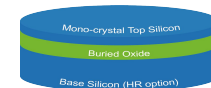
Smart FD-SOI

Crossover MCU, connected
MCUs, scalable FPGAs



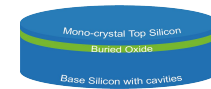
PD-SOI

High speed processing



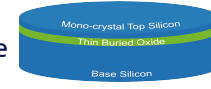
MEMS-SOI

High performance sensors



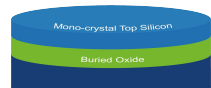
Imager-SOI

improved imager performance
in NIR



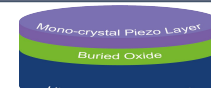
Photonics-SOI

Optical transceivers and
bio-sensing



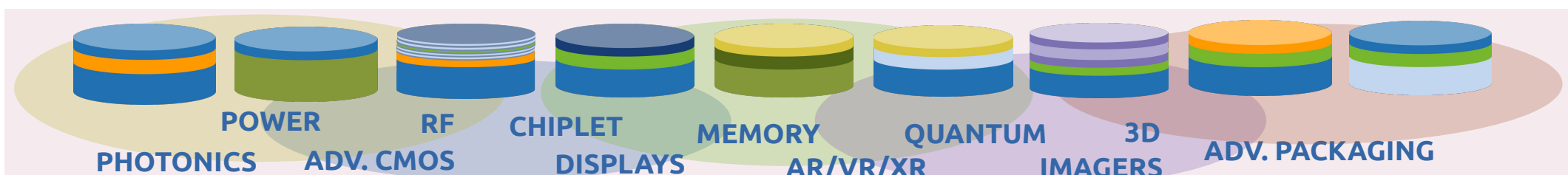
Photonics-LNOI

High speed data center
interconnect



PRODUCTS

R&D



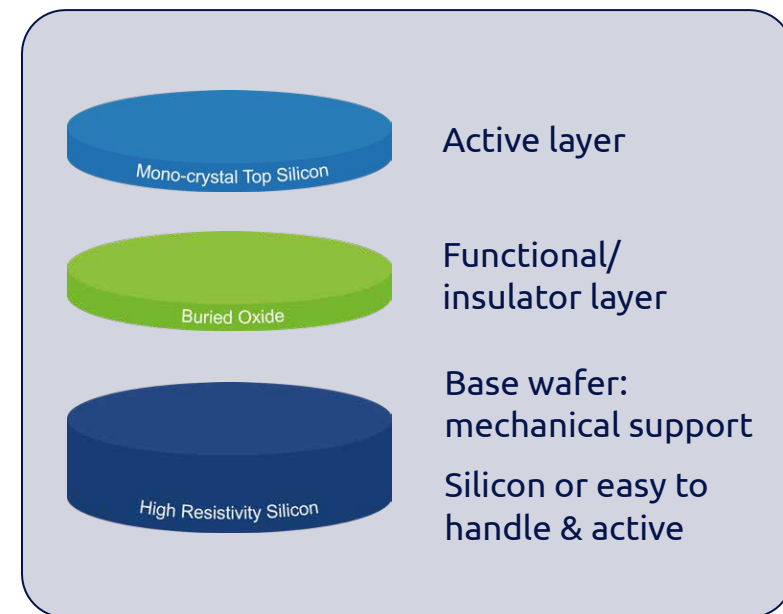
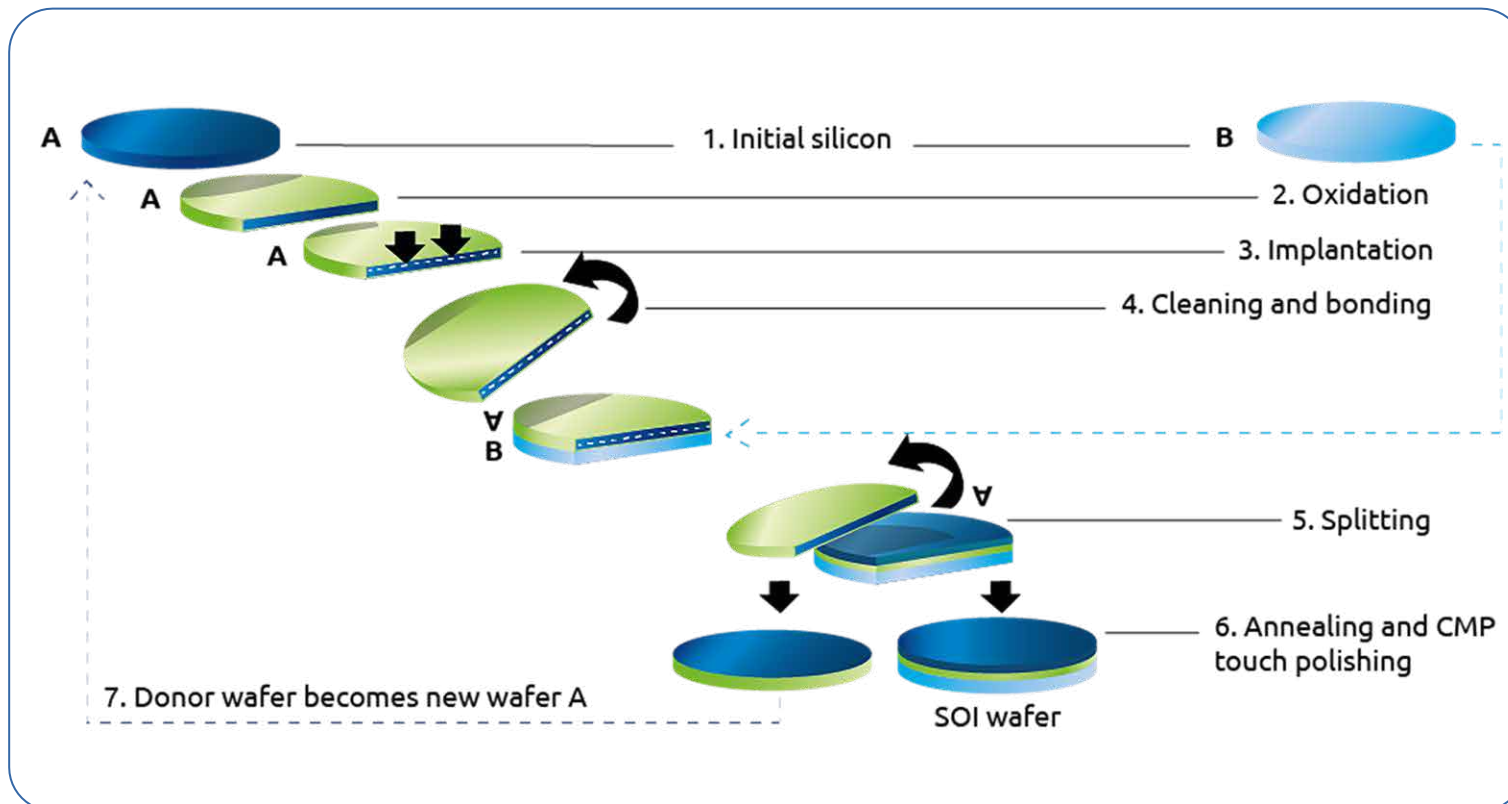
Prototypes targeting several applications

SECTION 01

SOI Substrates



SMART CUT™ AND SOI SUBSTRATES



TECHNOLOGY

- Industrial manufacturability of SOI – high yield
- Drastic improvement in uniformity & quality
- Re-use of donor wafer increases cost efficiency
- Flexibility of material integration

SOI SUBSTRATES

APPLICATIONS

- Smartphones radio-frequency front-end modules
- Networking base stations

- 3D sensors/Facial recognition
- Data centers and AI clusters
- Healthcare monitoring
- Smart home & Smart cities
- Wearables and hearables

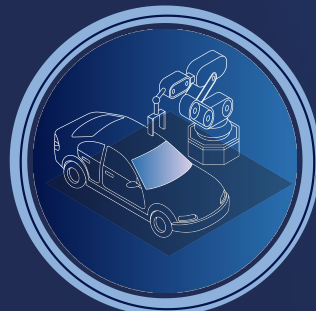
- Autonomous driving systems
- Connected car
- Vehicle electrification
- Industry 4.0



MOBILE COMM.



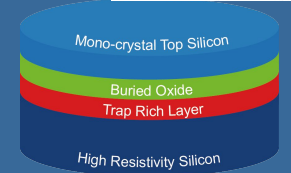
EDGE & CLOUD AI



AUTOMOTIVE & INDUSTRIAL

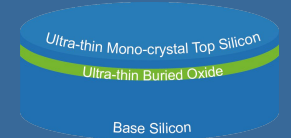
RF-SOI

For highly efficient mobile communication



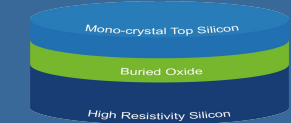
FD-SOI

Integrated technologies
MCUs, ADAS radar / vision



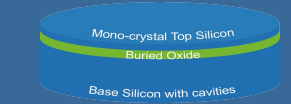
Photonics-SOI

Optical transceivers and
bio-sensing



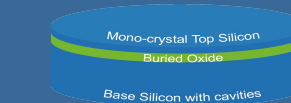
Imager-SOI

For improved imager
performance in NIR



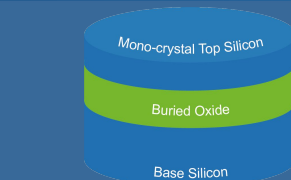
MEMS-SOI

High performance sensors



Power-SOI

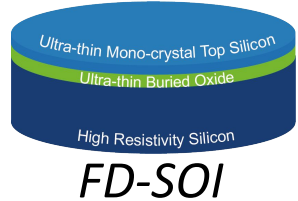
Power management IC,
In-vehicle netw. & gate driver



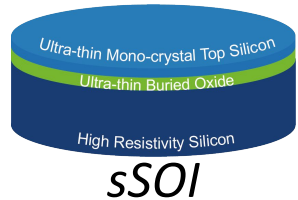
SOI substrate evolution to address new applications and better performance

*Selected
examples*

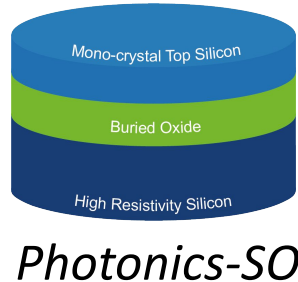
Introduction of new base material



Introduction of engineered top Si



Better material quality and new specs



HR Si base

- Support extended spectrum >100GHz with better RF passives, higher on-chip antenna efficiency and Noise reduction
- SATCOM: reduce LNA noise figure and increase PA efficiency

strain SOI

- significant performance boost: $f_t \rightarrow +50\%$, $f_{max} \rightarrow +40\%$, $G_m \rightarrow +10\%$
- 40% power reduction and 40% mobility boost
- Major improvement for PAE (PA) and lower noise (LNA)
- Higher stability under high temp operation

SOI enhancement

- Top Si lower roughness, crystal quality and thickness control
- Higher manufacturing yield and waveguide performance
- Better mechanical stability and packaging compatibility

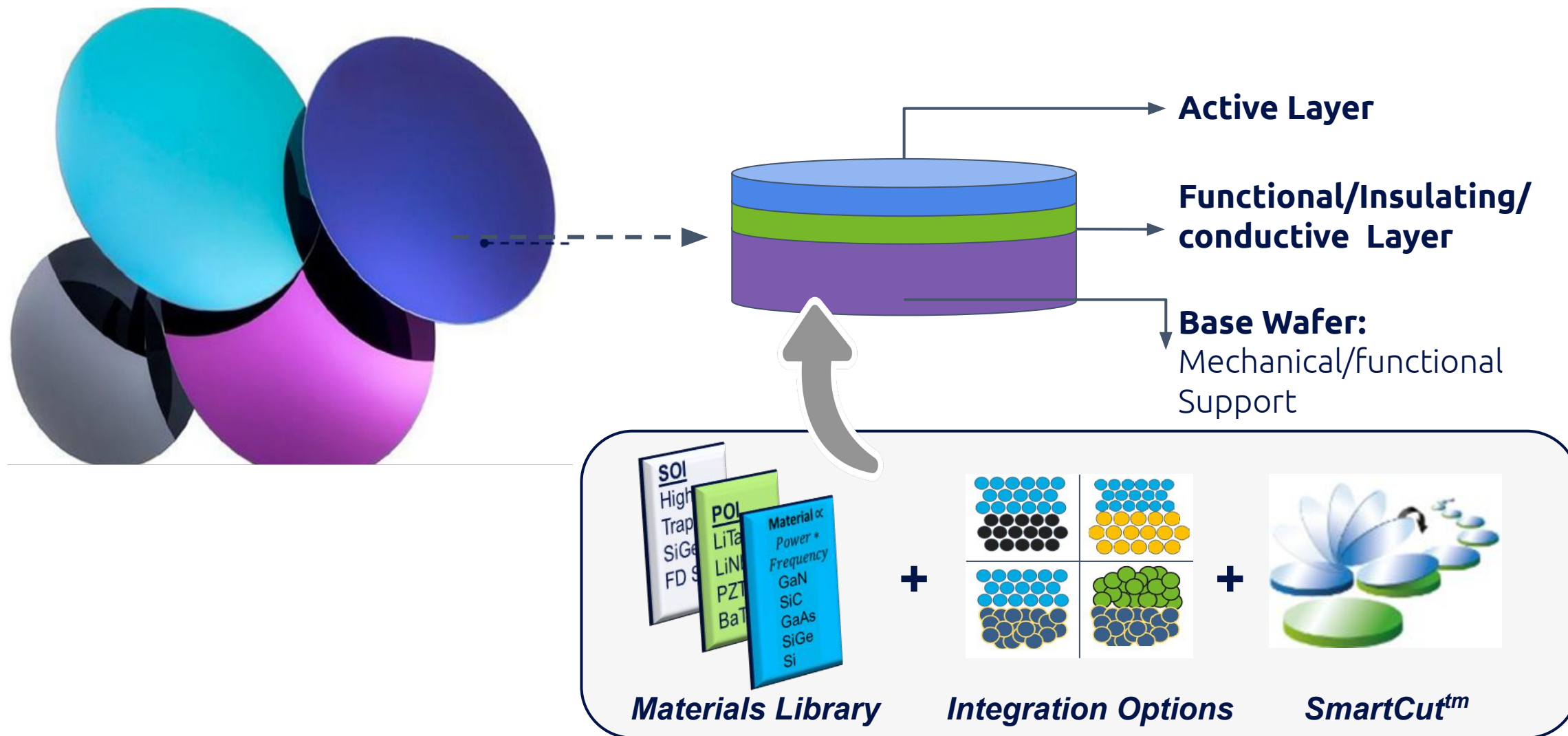
SECTION 01

III-V

Engineered Substrates



What is an Engineered Substrate?



Substrates engineered to extremes

An engineered substrate is a **purpose-built**, multi-layer foundation designed to optimize **thin-film** growth and device **performance**

III-V *bulk* challenges (generalities)

- **Expensive** material
- Chemical **crystal** quality
- **Brittle** material
- Poor **availability**
- Manufacturability
- **Low diameter** bulk substrates
- **Thermal** conductivity

Engineered Substrates

Each layer (and bonding interface) is designed for specific functional and/or mechanical purposes

Combine materials and layers that are not physically compatible or possible to built using conventional deposition methods

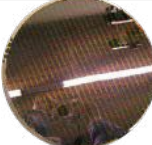
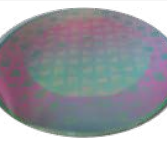
Built from bulk materials or pseudo donors using layer transfer, bonding, and/ or epitaxy techniques

Foundry or epi-ready industrial grade substrate for high-volume manufacturing (including large wafer size, availability, and cost considerations)

Enable the fabrication of devices with performances that surpass those made using only bulk materials

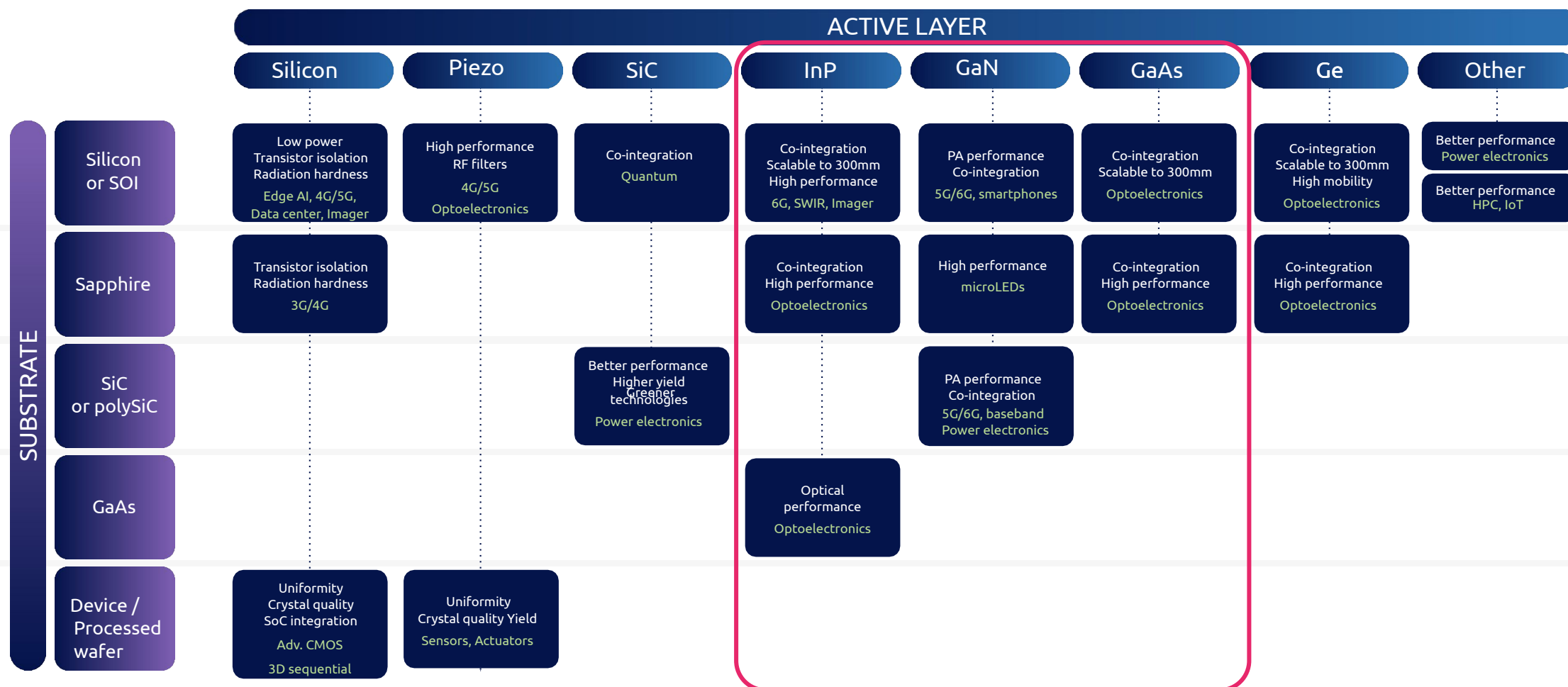
ANYTHING-ON-ANYTHING

BEST ACTIVE LAYER(S) ON FUNCTIONAL SUBSTRATE

		ACTIVE LAYER							
		Silicon	Piezo	SiC	InP	GaN	GaAs	Ge	Other
SUBSTRATE	Silicon or SOI								Diamond GaxOy 2D materials
	Sapphire								
	SiC or polySiC								
	GaAs								
	Device wafer								

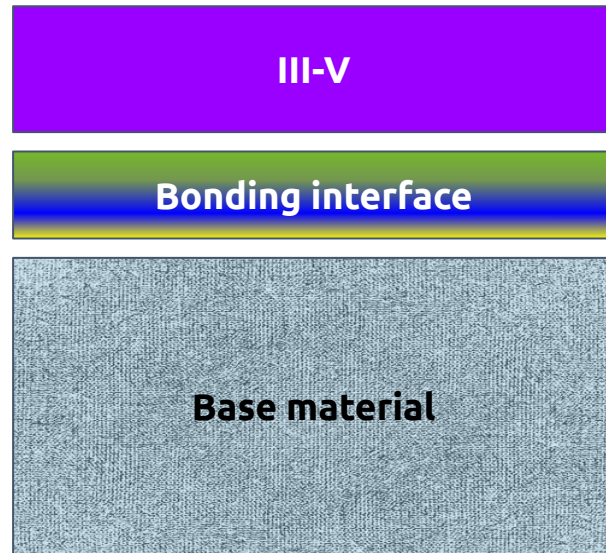
ANYTHING-ON-ANYTHING

ENABLING NEW PROPERTIES FOR SPECIFIC APPLICATIONS

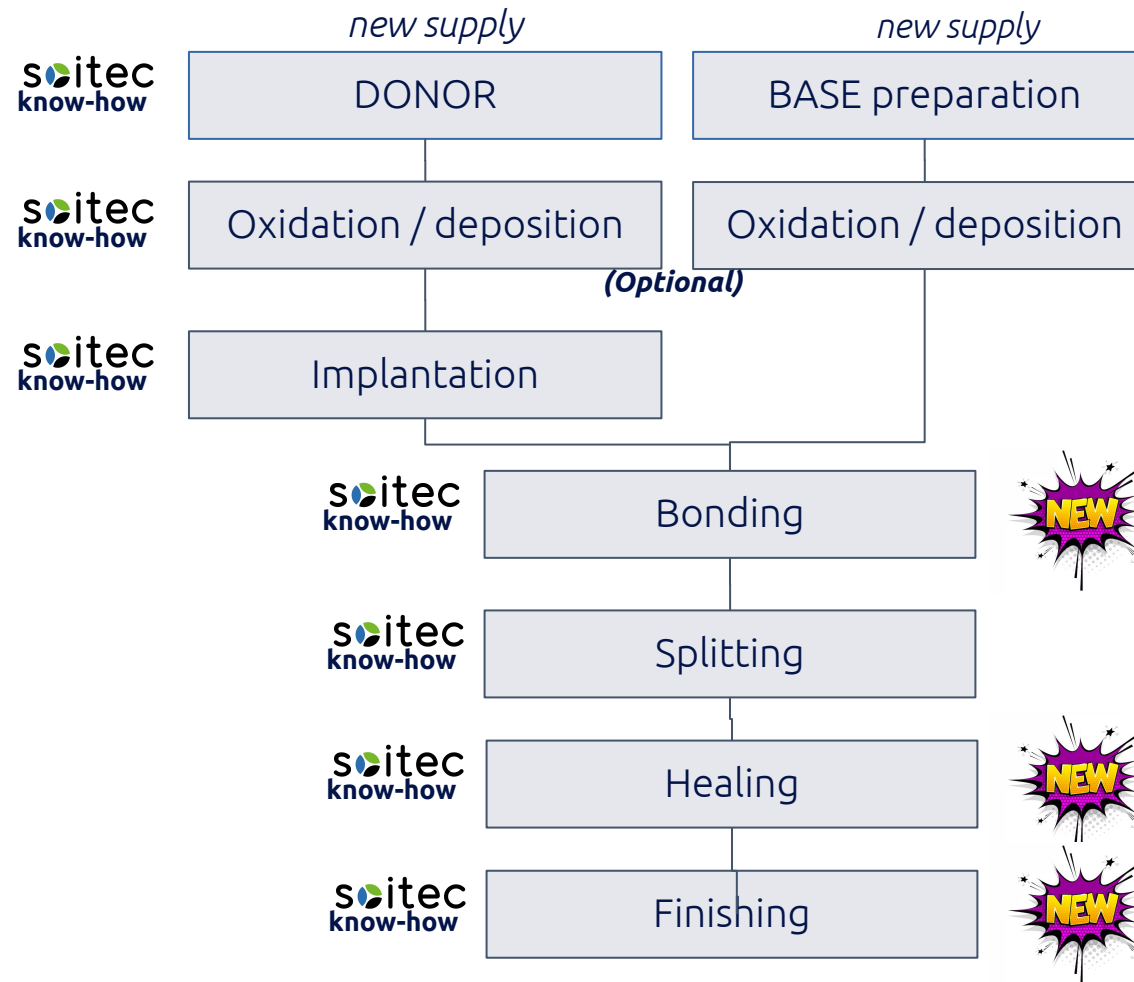


Smart Cut of III-V materials

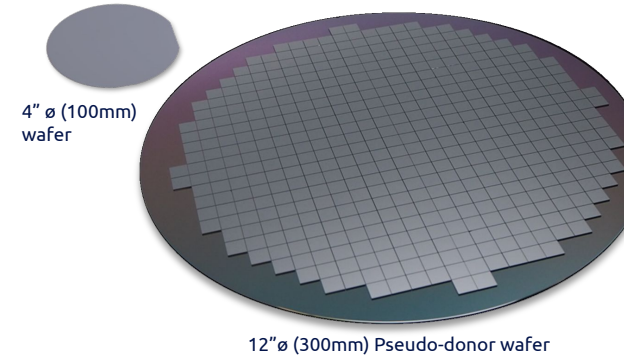
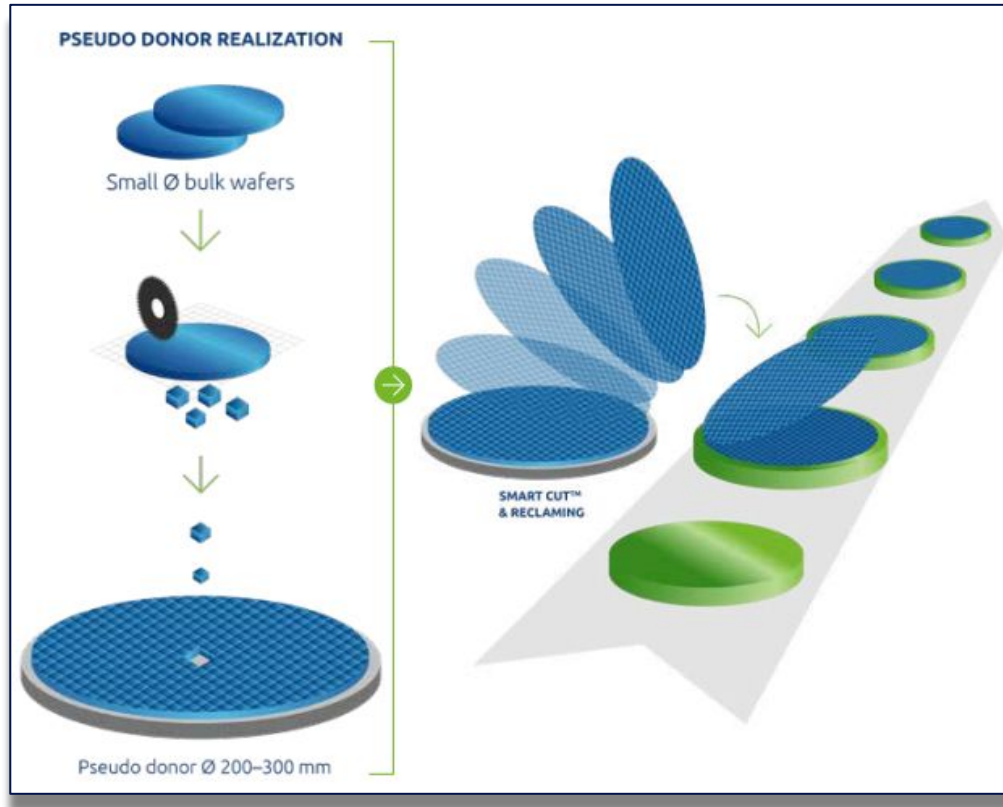
Requires introduction of new materials, bonding techniques, chemical compatibilities, process flows, into the Smart Cut™ process



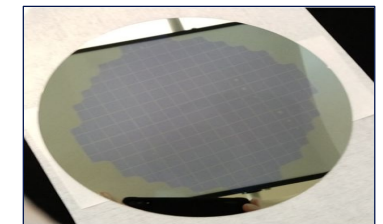
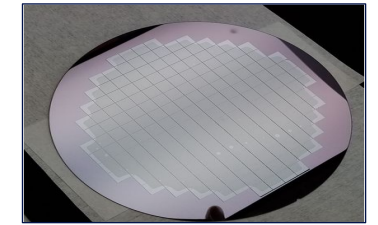
Designed for best performance,
at electrical, thermal, mechanical,
processability and reliability
level



Tiling: bringing up all materials up to 300mm



200mm PSD after Smart Cut™
(OK for reclaiming)

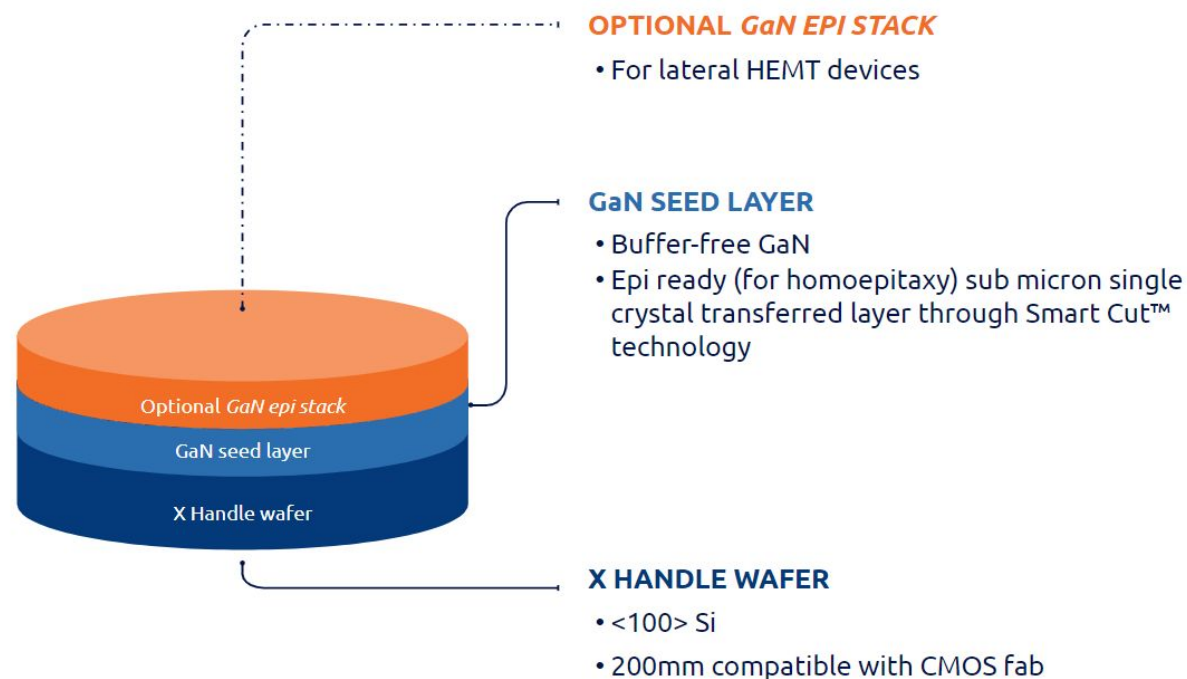


200mm InPOsi

C. Roda Neve on behalf of C. Maleville, "Engineered Substrates and Connectivity: Navigating the Future of Wireless and Mobile Communication Challenges (Industrial Keynote), EuMIC 2025, EuMW

Smart Cut™ GaN (SmartGaN) TECHNOLOGY

UseCase: GaN for RF

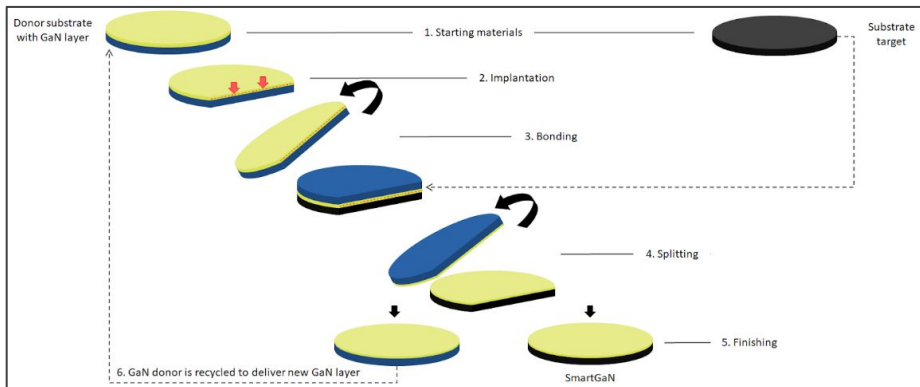


- ✓ • *Better crystalline quality of GaN layer (lower TDD)*
- ✓ • *Significantly cheaper device EPI stack (optimized epi device stack)*
- ✓ • *No buffer induced effects*
- ✓ • *Lower thermal resistance, better heat dissipation*
- ✓ • *Reduced RF losses, better substrate linearity*
- ✓ • *Wafer cost and size (200mm, 300mm compatible)*
- ✓ • *Sustainable solution (refresh, materials)*
- ✓ • *Purposeful solution for N-polar HEMT technology*

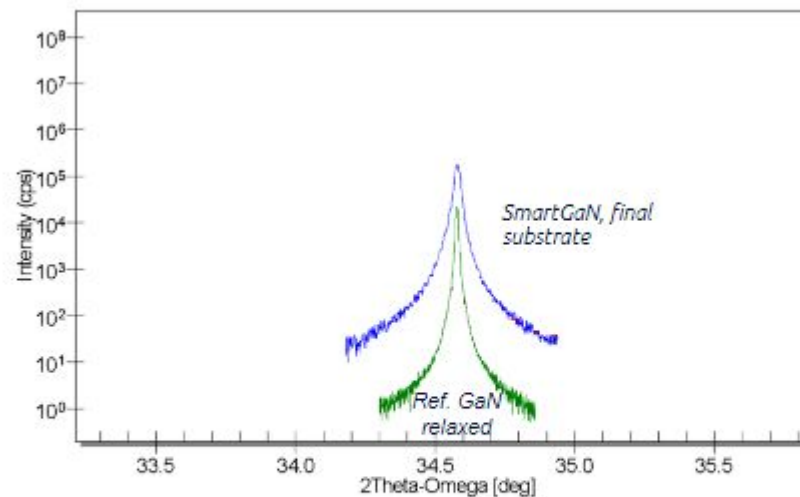
SmartGaN technology aims at increasing GaN HEMT operation frequency (>100GHz), higher power density, better PA efficiency and linearity, as well as reducing memory effects, current collapse and self heating.

Smart Cut™ GaN (SmartGaN) TECHNOLOGY

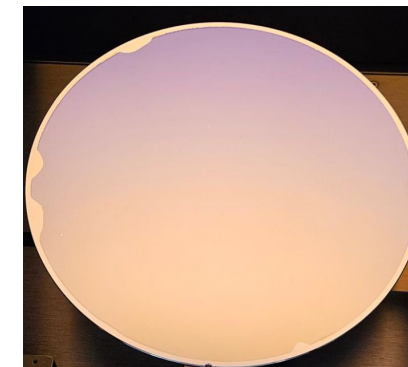
Smart Cut™ process for SmartGaN



XRD measurements of SmartGaN substrates



GaN layer fabricated by Smart Cut™ is similar to the starting GaN epitaxial layer.



8" SmartGaN on Si
(250nm-thick top
epi-ready GaN layer)

Gweltaz Gaudin, Christelle Veytizou, Jan Strate, Florence Servant, Amélie Thomas, et al.. Bufferfree GaN-on-X engineered substrates fabricated by using Smart Cut technology. ICNS-14, Nov 2023, Fukuoka, Japan. 2023. ffcea-04667600

Smart Cut™ InP (INPOSi) TECHNOLOGY

UseCase: InP for RF (HBT/HEMT)

Seed layer

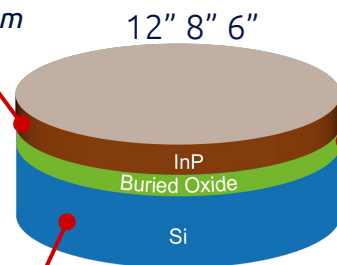
- Epi-ready InP layer
- Crystalline orientation : (100) on-axis; or off-axis
- Doping : SI (Fe) or n-type (Sulfur) or p-type
- Low TDD (<E+3/cm² range)
- Thickness : typically 0.1µm to 0.5µm

Bonding interface

- **Thick** (0.5- 2µm) or **thin** box (<0.2µm)
- **No BOX** for low thermal resistance

Handle wafer

- Up to 200/300mm wafer (CMOS compatible)
- Standard "low cost" Si
- Advanced Si (High-Resistivity, trap-rich ..)



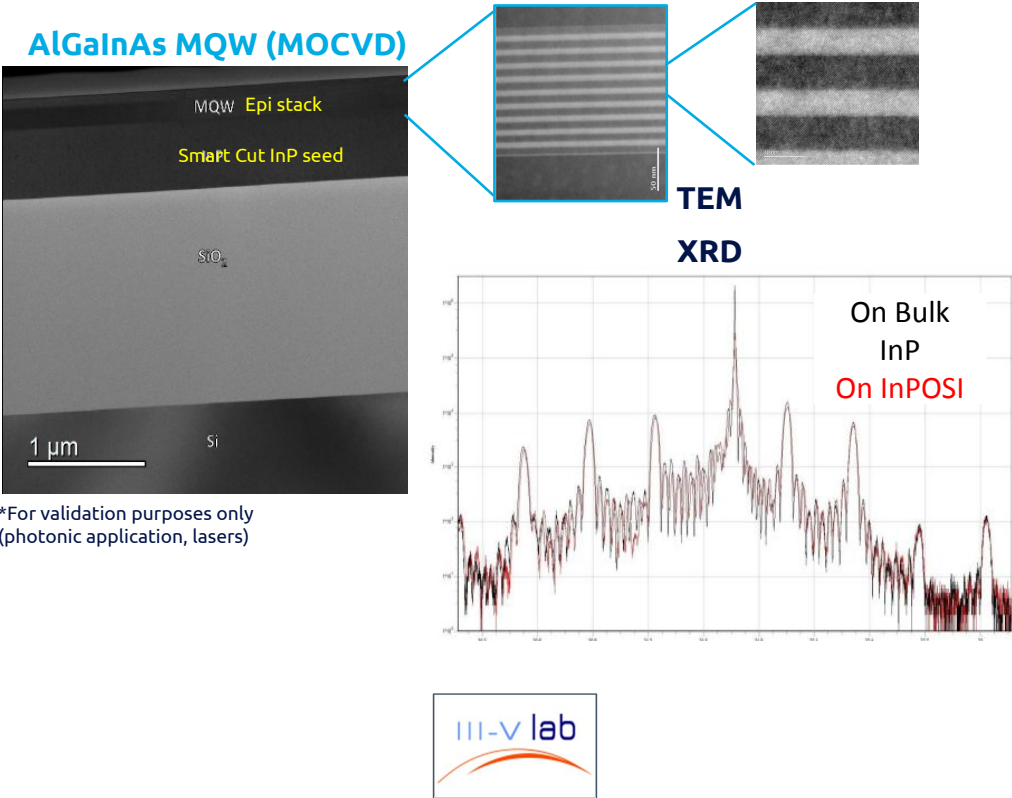
* Other handle wafer can be used (e.g. GaAs, SiC, pSiC)

- ✓ •Cost effective solution
- ✓ •Sustainable InP material solution (through reuse)
- ✓ •Better thermal conductivity than bulk InP
- ✓ •Mechanically robust
- ✓ •Crystal and epi quality as good as InP bulk
- ✓ •Mechanically robust
- ✓ •Different integration and packaging approaches
- ✓ •Up to 8", 12" for CMOS compatibility

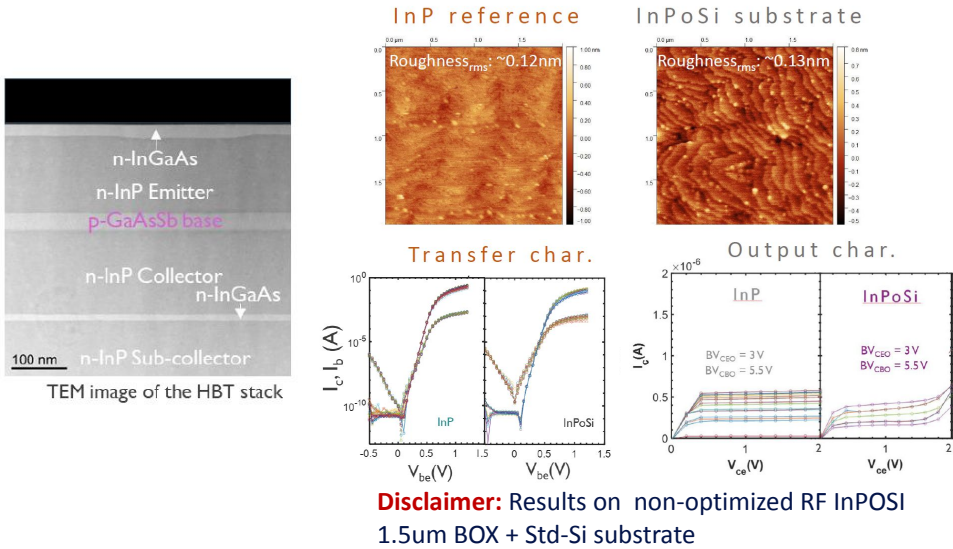
INPOSi aims to become the technology choice for high volume InP RF, providing enhanced efficiency

Smart Cut™ InP (InPOSi) TECHNOLOGY

Complex epitaxy growth on InPOSi wafer



First demonstration of HBT on InPOSi



Similar performance of InPOSi HBT vs InP bulk

A. Vais, et al "A CMOS compatible III/V-on-300mm Si technology for future high speed communication systems: Challenges and possibilities", EuMW 2024, KETCOM WS, WS-02

Engineering substrates addressing the main photonics functionalities

- Emit light

InPOSi

- Transport light

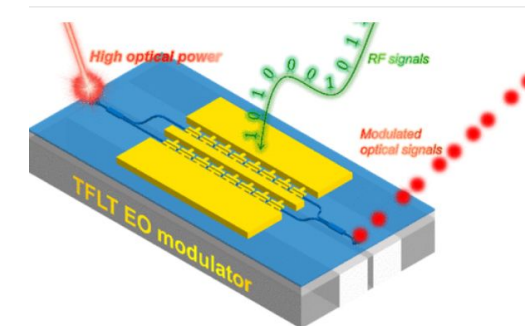
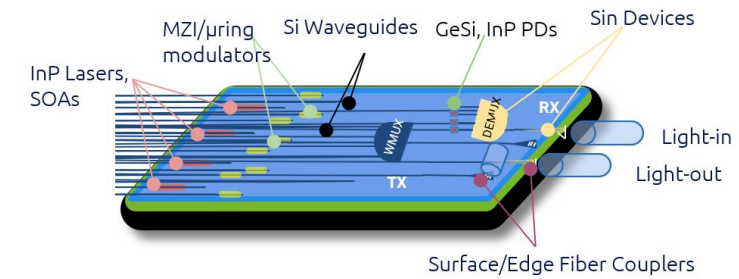
SOI

- Manipulate light

LNOi

- Detect light

InPOSi



ACS Photonics 2025, 12, 10, 5345–5351

KEY MESSAGES

III-V Engineering substrates

- Going beyond Si and SOI performance limitations
 - Pushing device performance, cost, and availability
- Needed to unblock III-V bulk material limitations
 - Require introduction of new materials and fabrication technologies
- SOITEC's know-how enabling high-quality substrates
 - SOITEC driving eng substrate from genesis to high volume production



Cesar RODA NEVE
cesar.roda-neve@soitec.com

THANK YOU

www.soitec.com

 @soitec_corporate

 @soitec_official

 @soitec_official





SOITEC PROPRIETARY

Any unauthorized reproduction, disclosure, or distribution of copies by any person of any portion of this work may be a violation of Copyright Laws, could result in the awarding of Damages for infringement, and may result in further civil and criminal penalties.

Exclusive property of Soitec. This document contains restricted information: disclosure, redisclosure, dissemination, redissemination, reproduction or use is limited to persons within Soitec and third parties which receive this document with a need to know only. Use or reuse, in whole or in part, for any purpose other than which expressly set forth in this document is forbidden.

All rights reserved. Copyright ©2024 SOITEC.

