



8" Open Innovation Silicon Carbide Pilot Line and Platform Technologies at A*STAR Singapore

Dr. Navab Singh

Deputy Executive Director (Research)
A*STAR Institute of Microelectronics (IME)

A*STAR Organization & Research Institutes

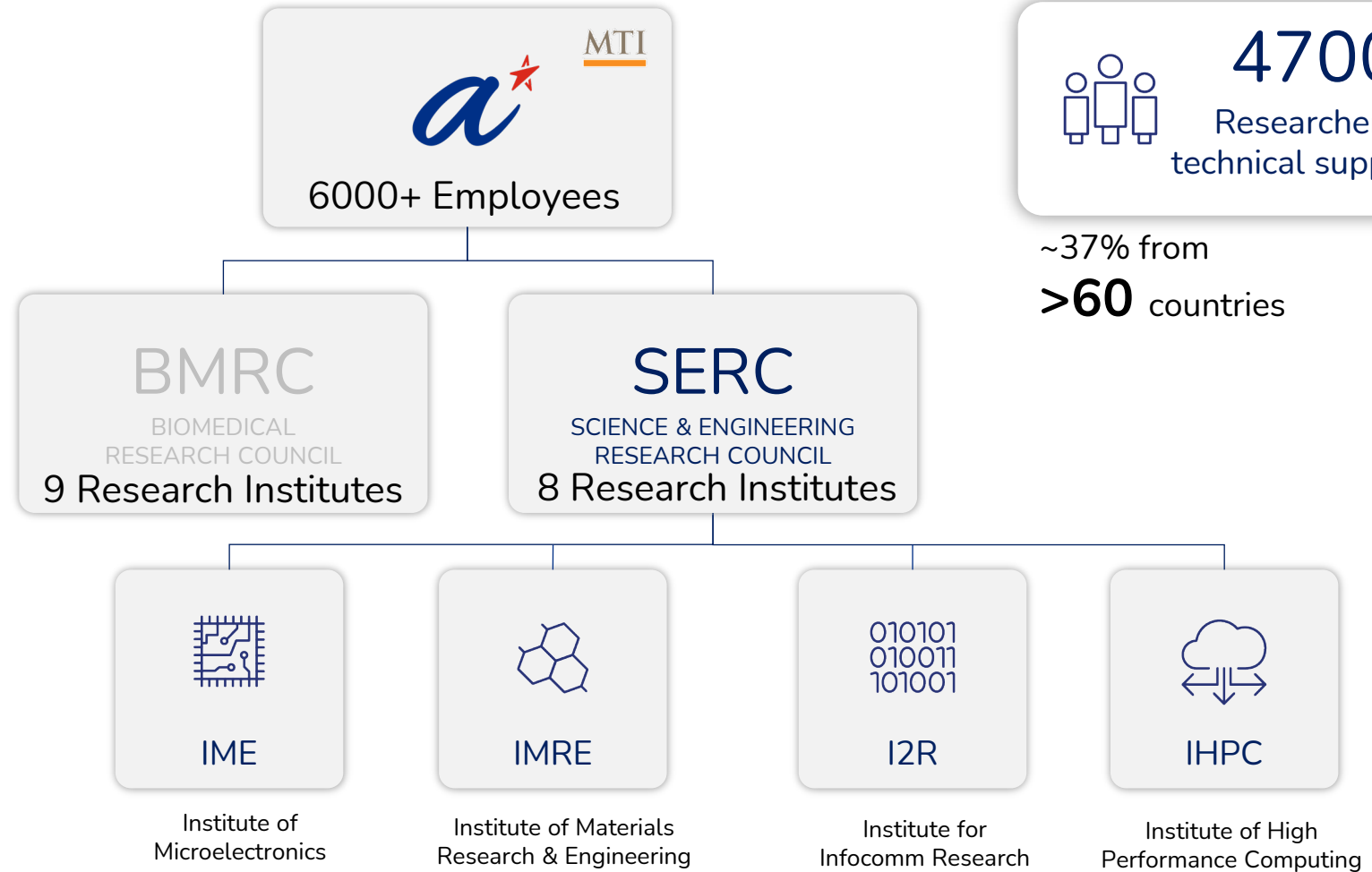
Partner
Agencies

EDB:
SINGAPORE

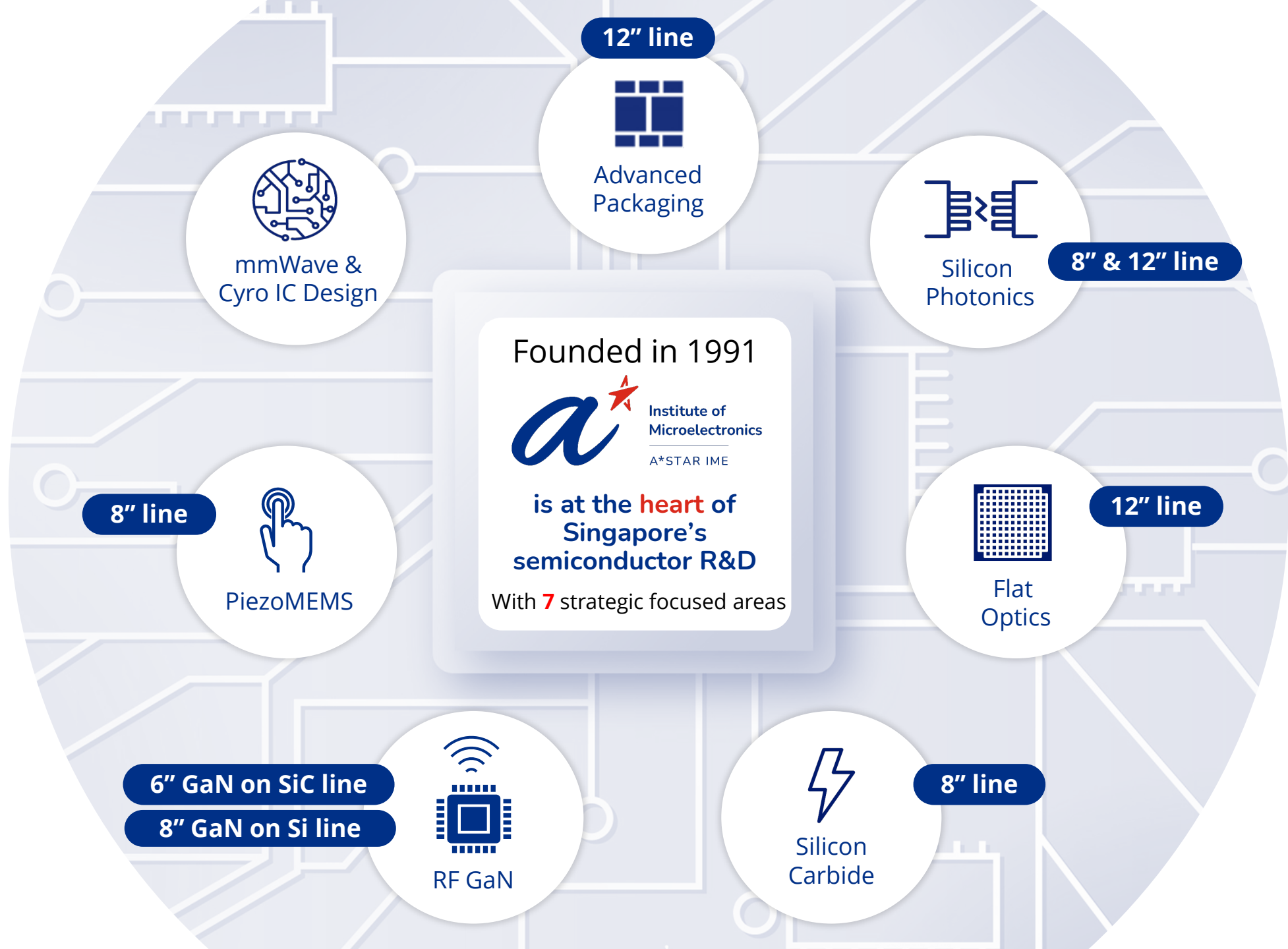
MTI

Enterprise
Singapore

MTI



Semiconductor focused... 500+



Bridging R&D and manufacturing with production-ready pilot lines

Existing 8000 Sqm

Fusionopolis



- 8" SiC
- 6" GaN on SiC
- 8" GaN on Si
- 8"/12" Si Photonics
- 12" Flat Optics

Science Park 2



- 12" Advanced Packaging

Ang Mo Kio



- 8" PiezoMEMS Joint-lab

Additional 9000 Sqm

Tampines



- 12" Advanced Packaging
- 12" Si Photonics
- 12" Flat Optics

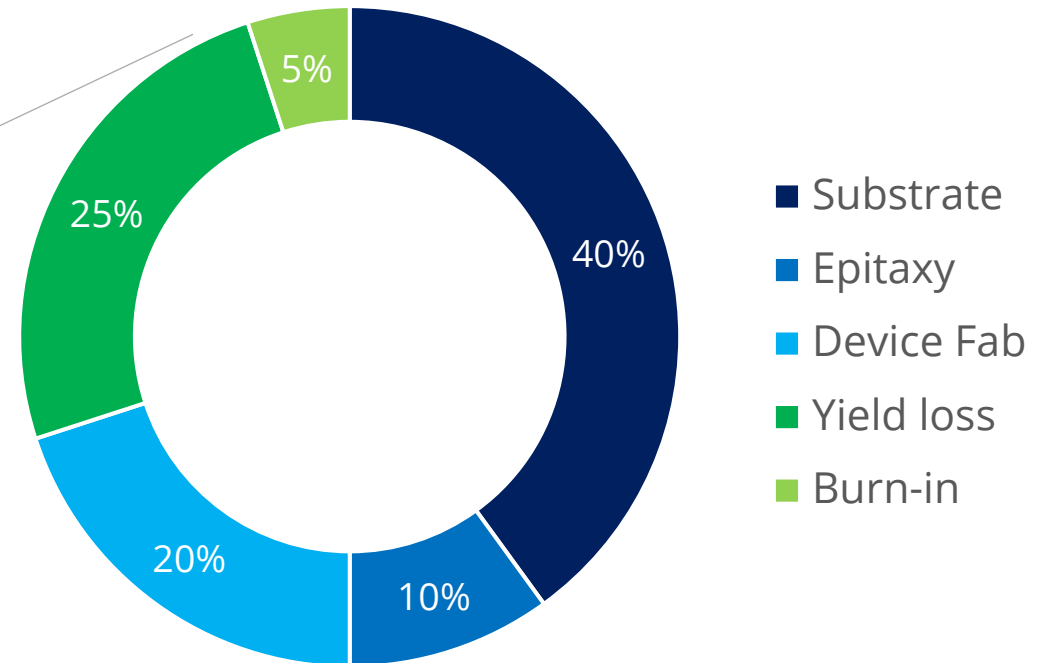
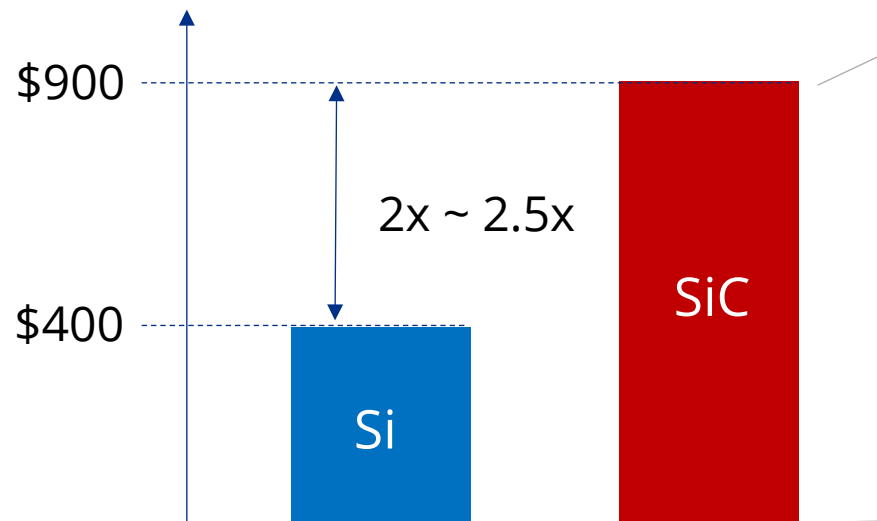
Coming in Sep 2026

2025 a turning point for SiC?

Analysis in 2024 when SiC N-type 8" substrates is ~\$1,800.

1200V

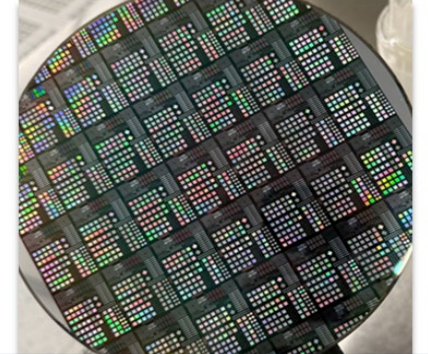
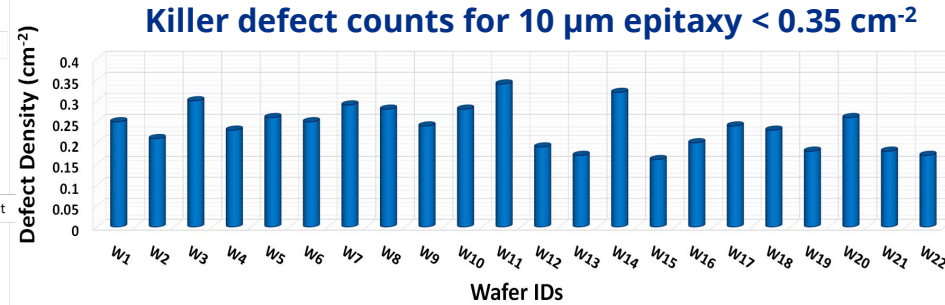
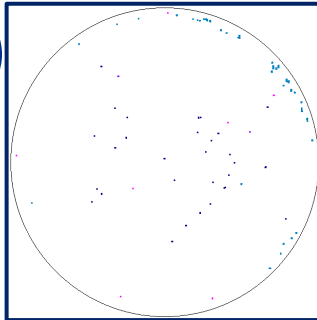
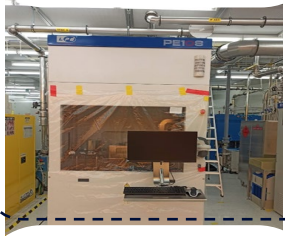
800V battery EV traction inverter
(1.2kV SiC-MOSFET or Si-IGBT device)



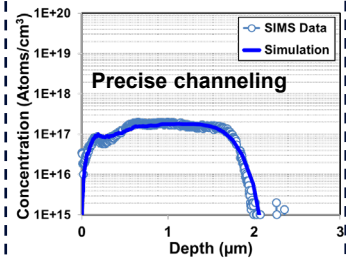
Data source: YOLE YINTR24422 - Power SiC - Markets and Applications 2024

SiC Pilot Line Status: Device design to power module package

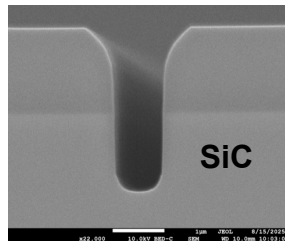
Epitaxy



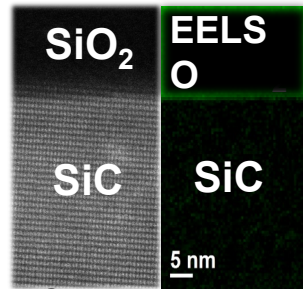
Implantation



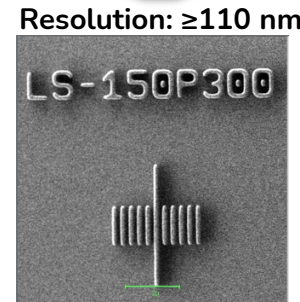
Trench etch



Gate stack



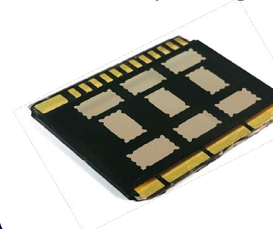
Lithography



Packaging



1200V SiC 6-in-1 power module packaging



Prototyping for Industry, RTO & academia partners

- Customize and transfer SiC process technology
- Small-scale production capabilities for rapid product demonstration

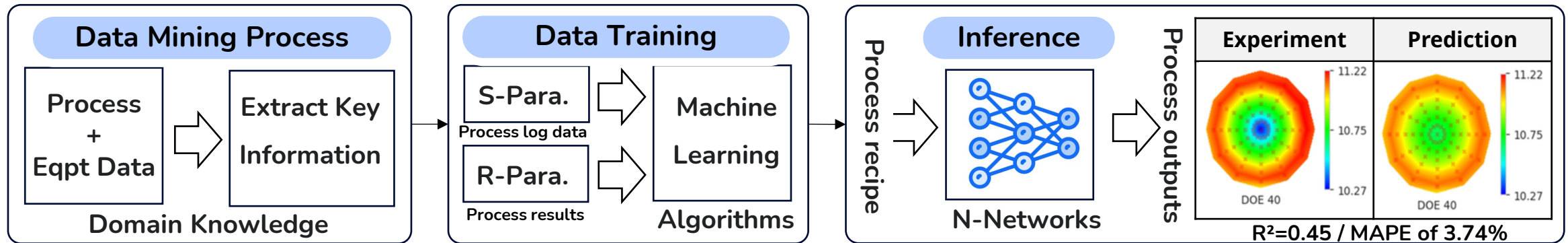
Key focus:

- Trench Gate MOSFETs
- FinFETs
- Super junction MOSFETs
- IGBT – in prep.

AI/ML-Based Improvement in SiC Epitaxy Thickness Uniformity

SiC Epitaxy Thickness Prediction Model Development:

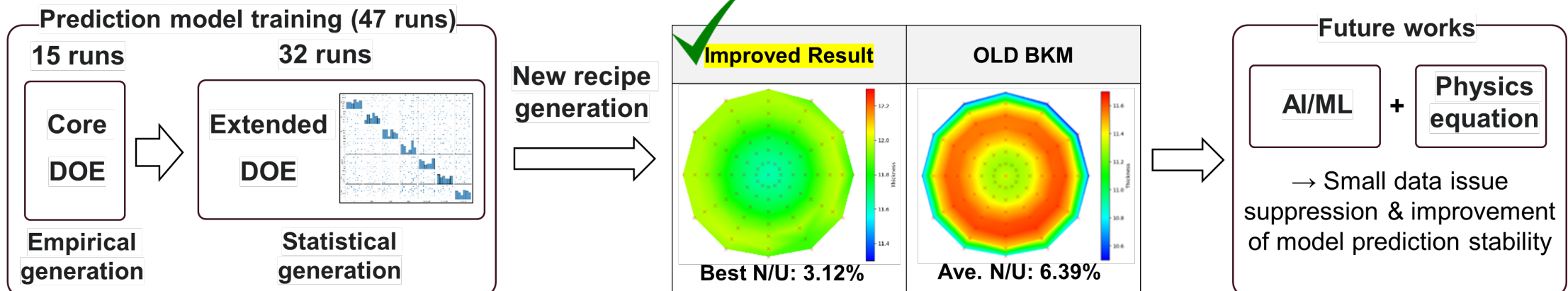
→ Neural network-based process prediction model development using ASM PE108 Equipment (6/8-Inch Wafers)



2. Process Improvement Using AI/ML Prediction Models:

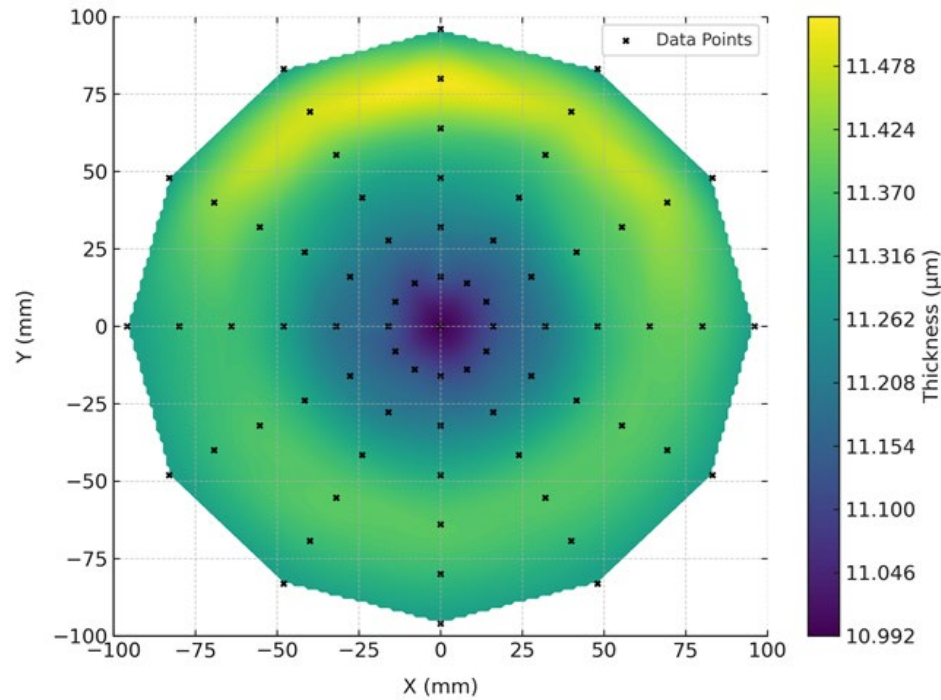
→ Prediction model-based recipe development and validation (**N/U: 6.39% → 3.12% improvement (N/U=3 σ /Mean)**)

→ Integration of physics equations in progress for further improvement of the prediction model

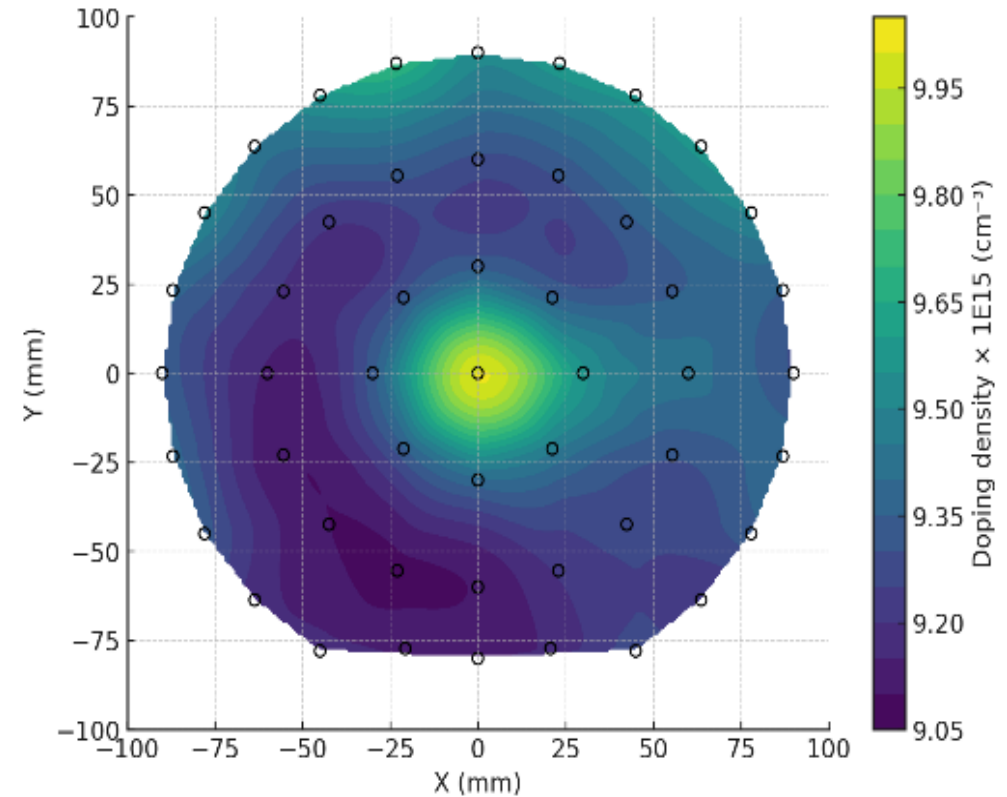


State-of-the-art SiC Epitaxy with High Throughput

Thickness nonuniformity (s/m): 0.93 %



Doping nonuniformity (s/m): 1.9 %



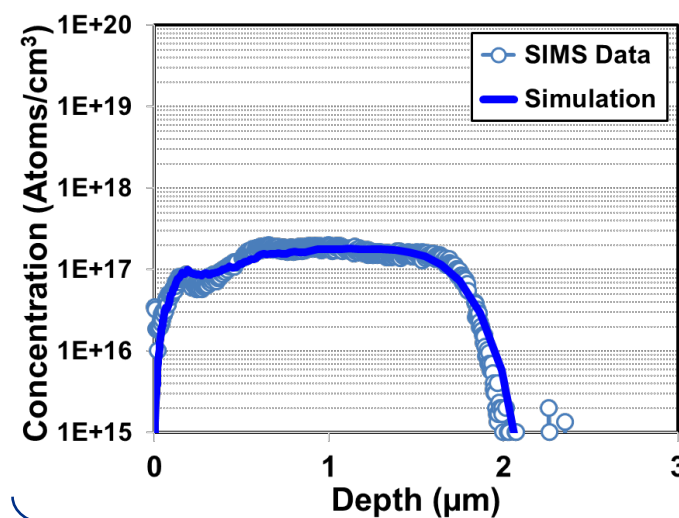
Implantation: Precise Implantation Control with In-situ XRD

Ion Implanter

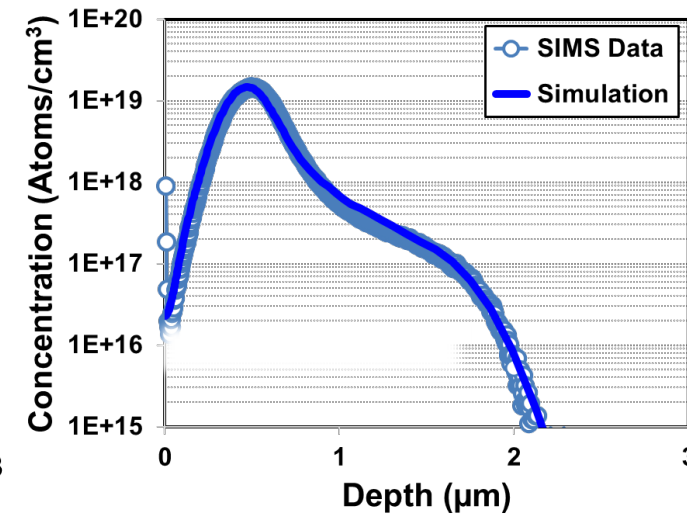


- Implant elements: B, N, Al, P and Ar
- Energy Range: 10 ~ 960 keV
- Temperature: 25-500 °C
- Tilt angle: 0-60°
- Twist angle: 0-270°
- Qualified process for 8" SiC and Si wafers

Phos Implant with channeling



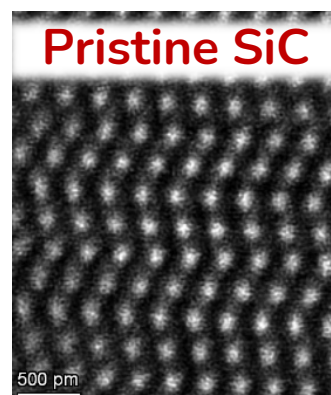
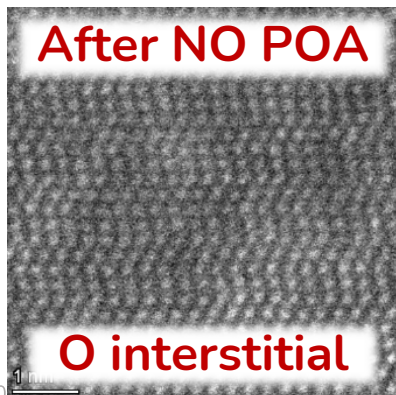
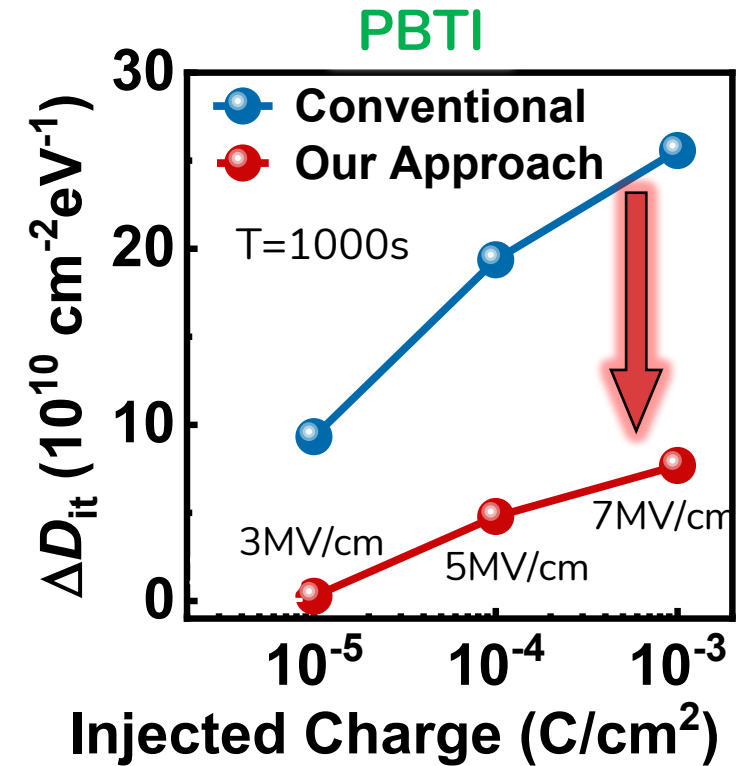
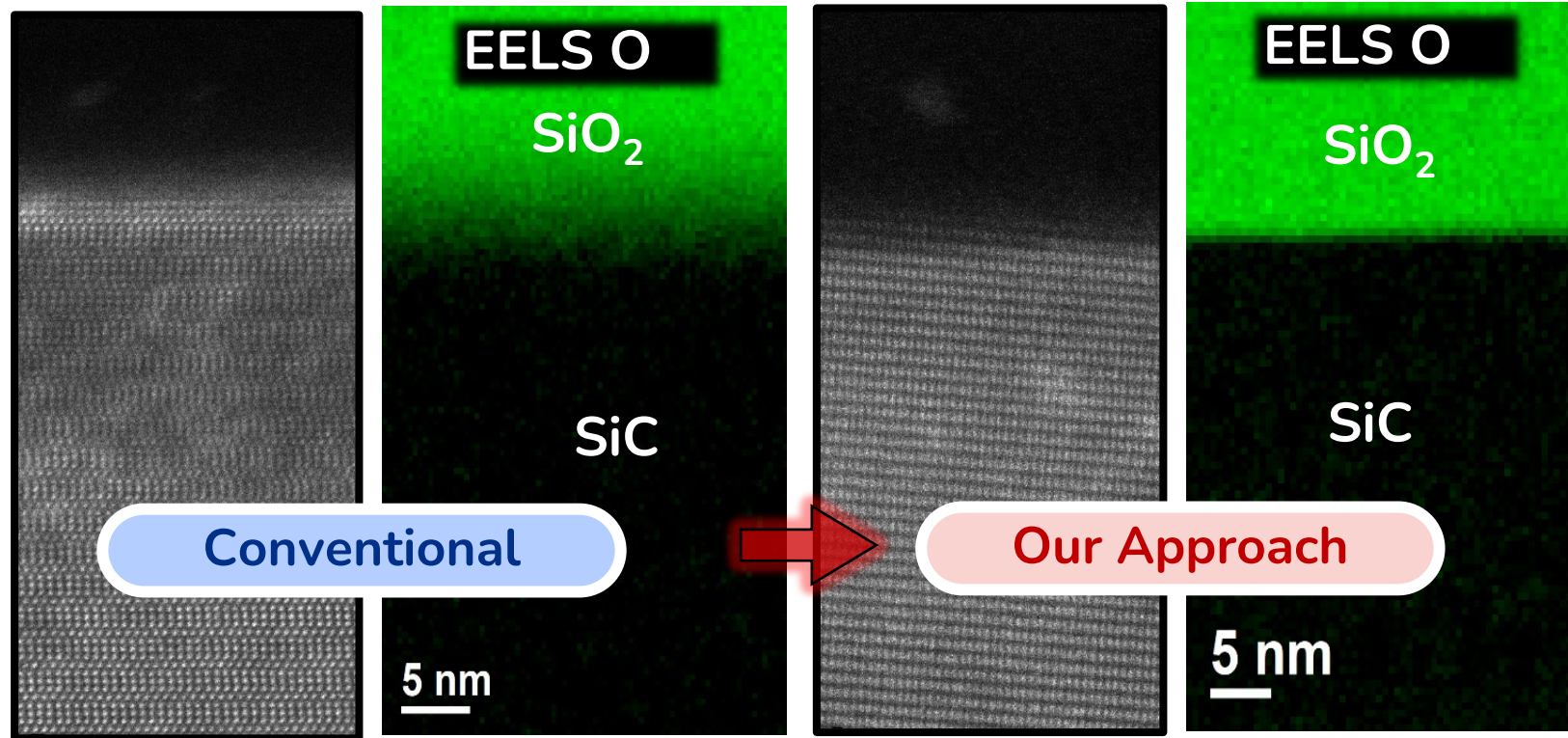
Al Implant with channeling



- In-situ X-ray diffraction system (Laue's diffraction)
- Accurately calibrate the tilt angle for channeling implantation

Excellent matching between
simulated and experimental results

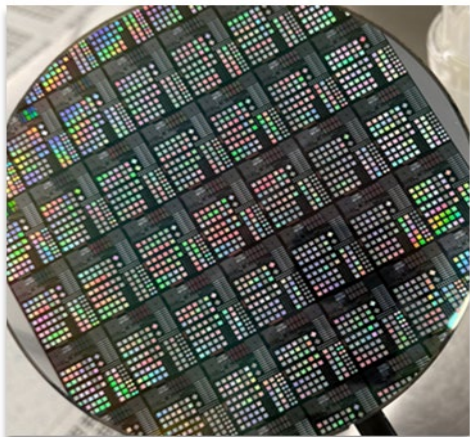
High Quality MOS interface



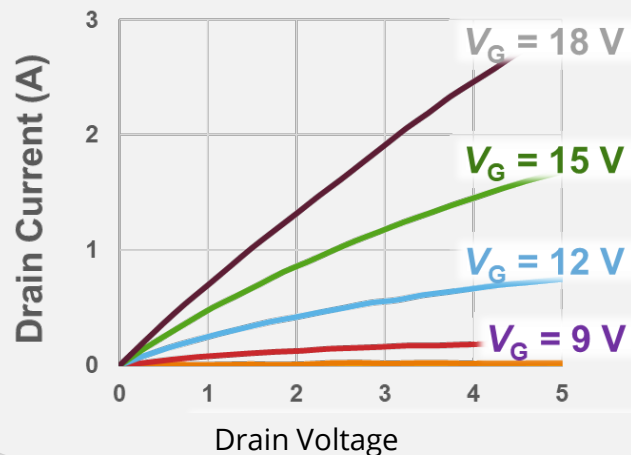
- Excellent MOS interface resulting into **10x improvement in PBTI and NBTI** has been achieved thus addressing the reliability issue with NO POA.
- Experiments are ongoing to fabricate MOSFET and measure mobility.

Planar gate MOSFET – our first demonstration

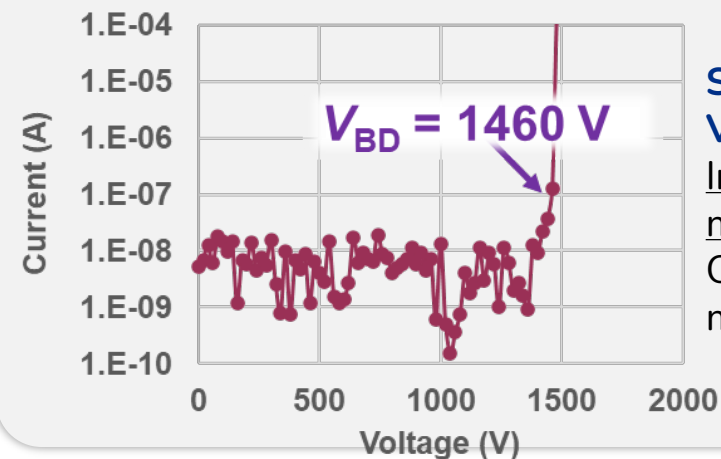
SiC MOSFET on 8" wafer



V_d vs I_d curves

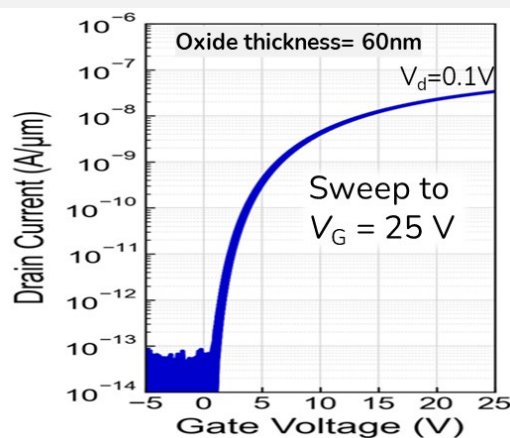


Breakdown Voltage

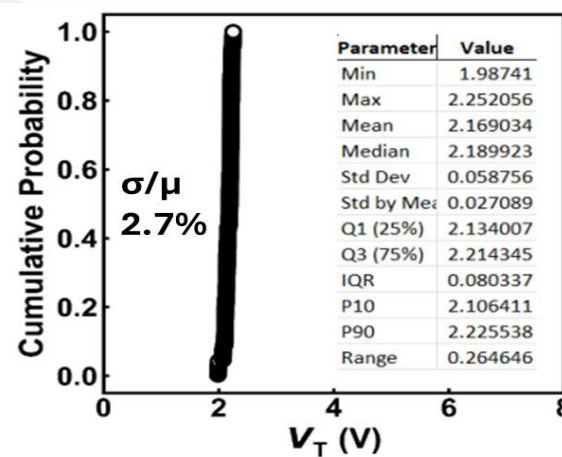


Simulated
 $V_{BD} = 1485\text{ V}$,
 Impact ionization
 model: Calibrated
 Okuto-Crowell
 model

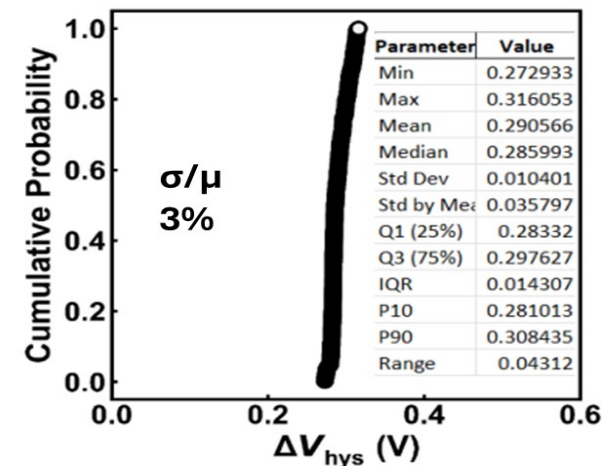
Transfer Characteristics



V_T distribution: 345 points



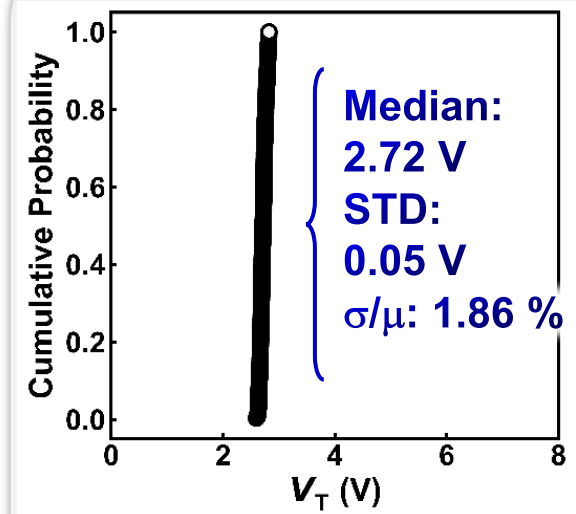
V_{hys} distribution



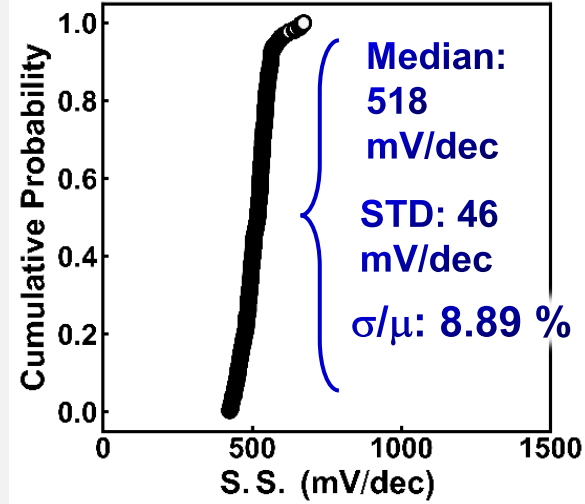
Sweep to $V_G = 25\text{ V}$
 (Eox ~ 4 MV/cm)

Trench Gate MOSFET – a step towards competing technology

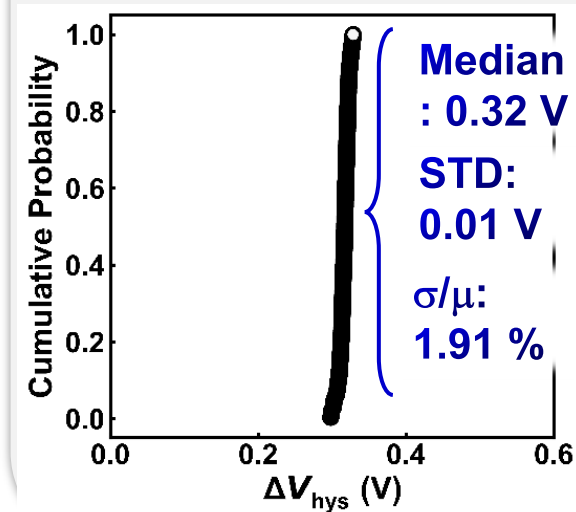
V_T



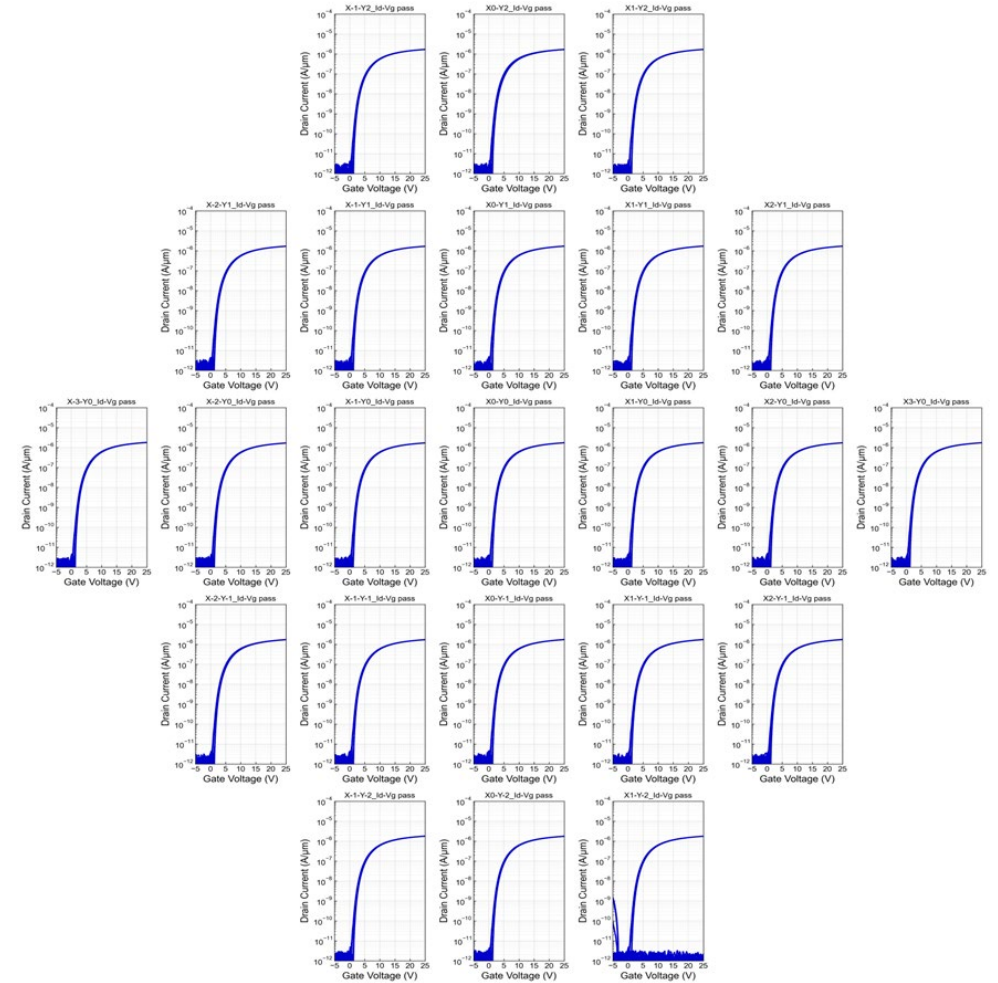
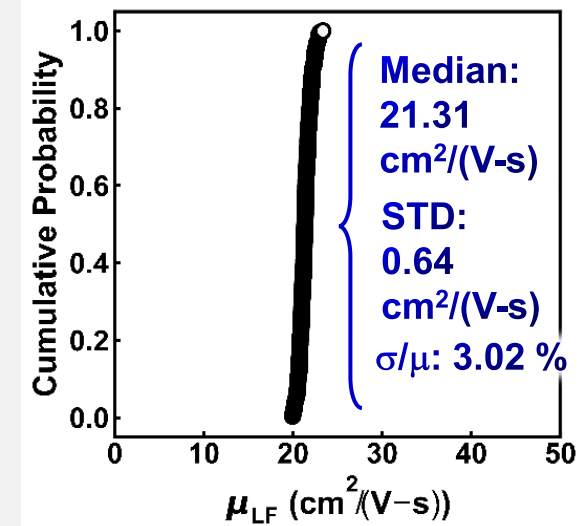
S.S.



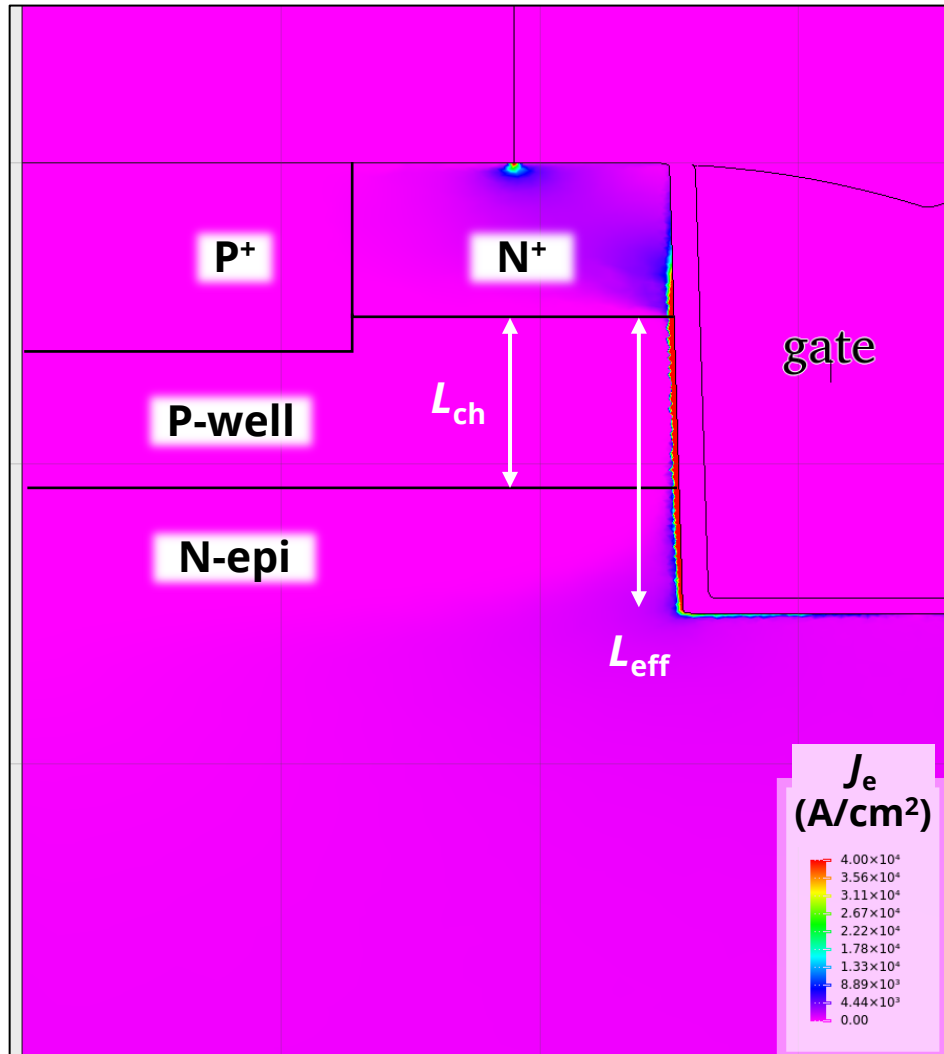
ΔV_{hys}



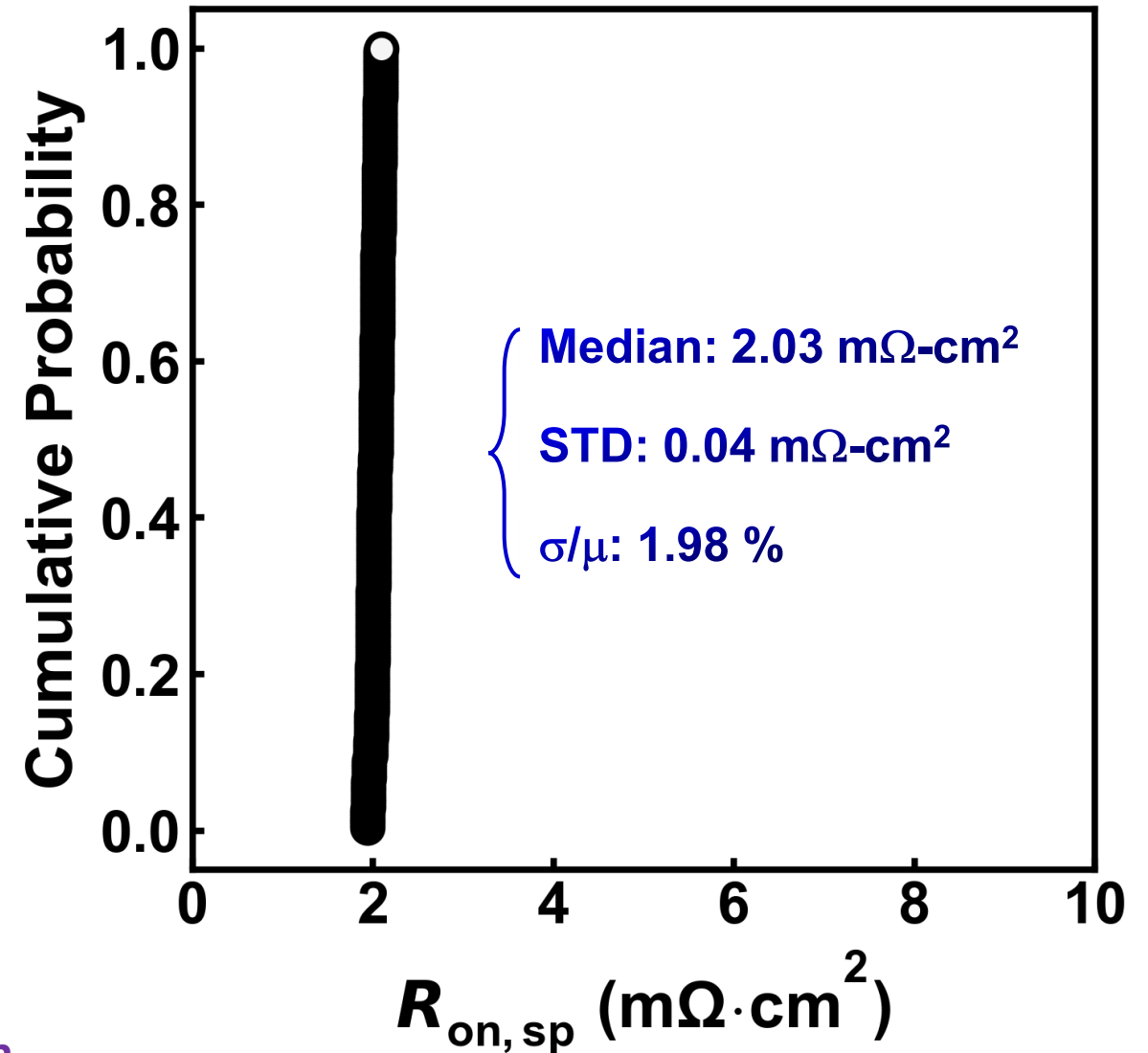
μ_{LF} (Y-function)



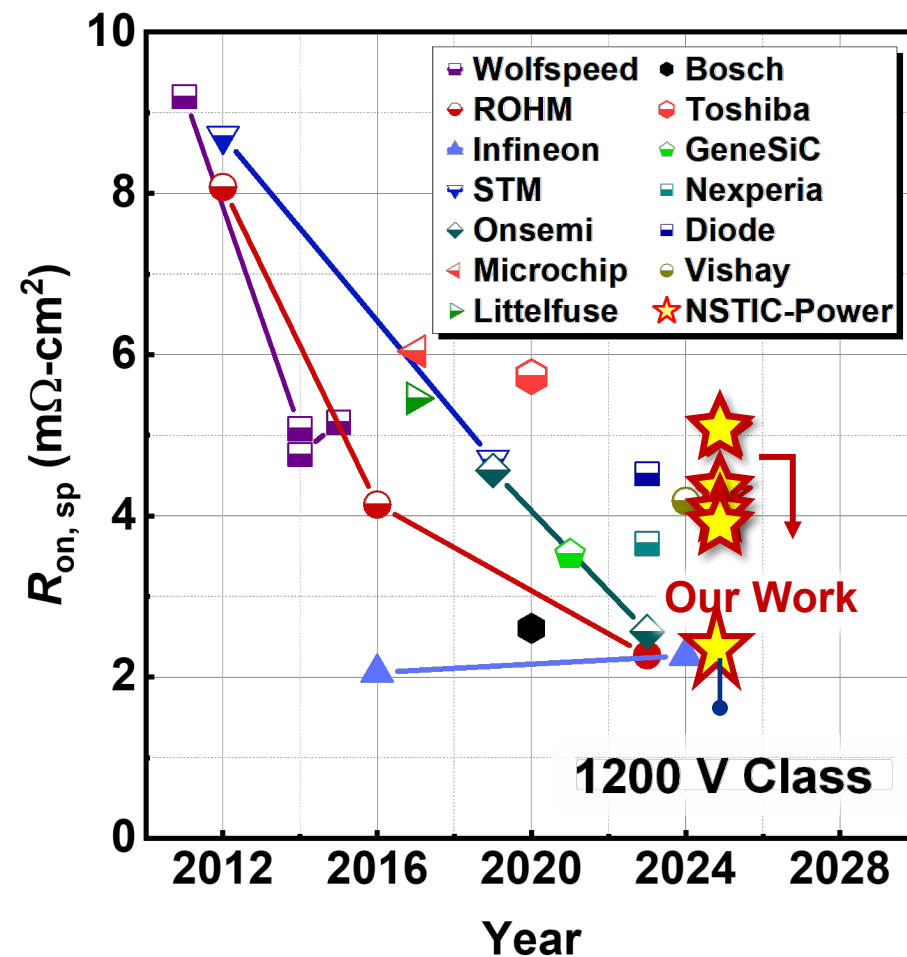
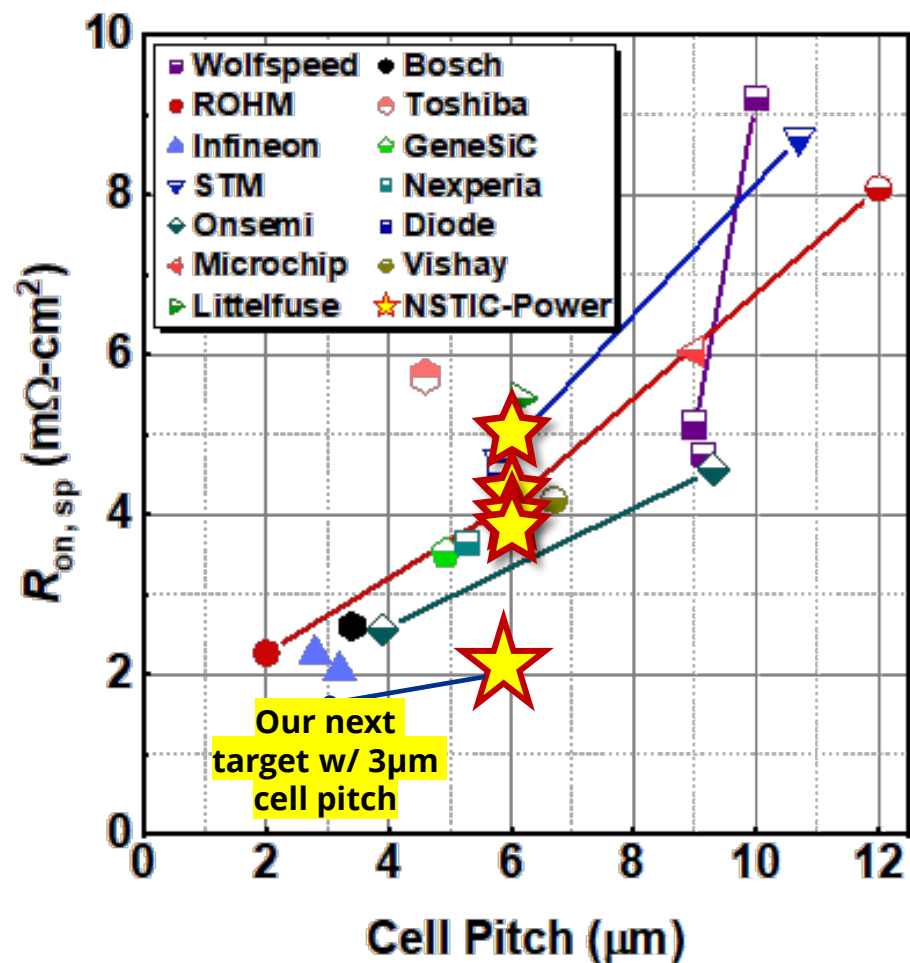
$R_{on,sp}$ of $2.03 \text{ m}\Omega\cdot\text{cm}^2$ at a cell pitch of $6\mu\text{m}$!
“Our Trench Mobility Values are Underestimated”



Uncertainty in L_{ch} leads to mobility underestimation



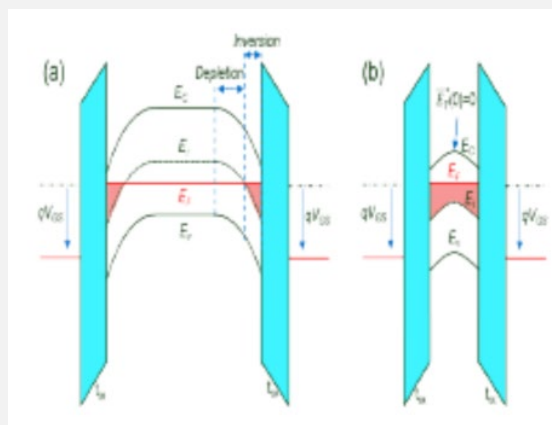
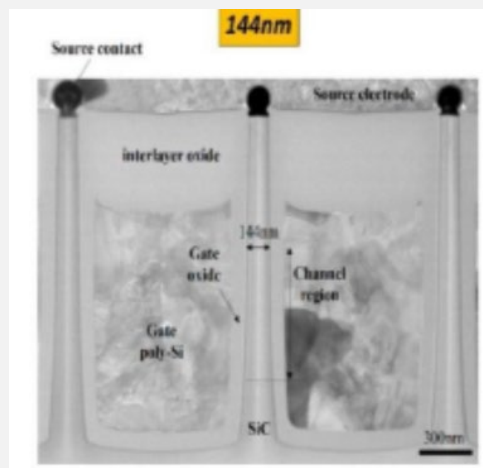
Benchmarking $R_{on, sp}$ with Commercial Products



Note: our reported $R_{on, sp}$ is for device optimized for On behavior. Blocking to be applied.

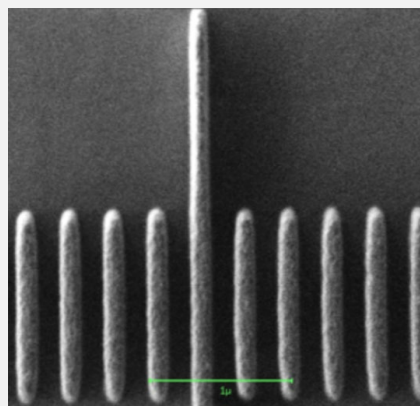
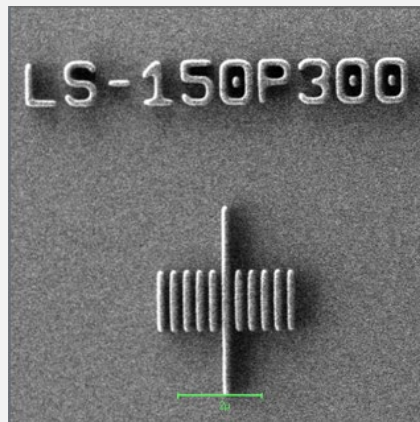
Beyond Trench gate: Power finFET and SuperJunctions

~1 μ m Fin Pitch demonstrated
(Ref.)

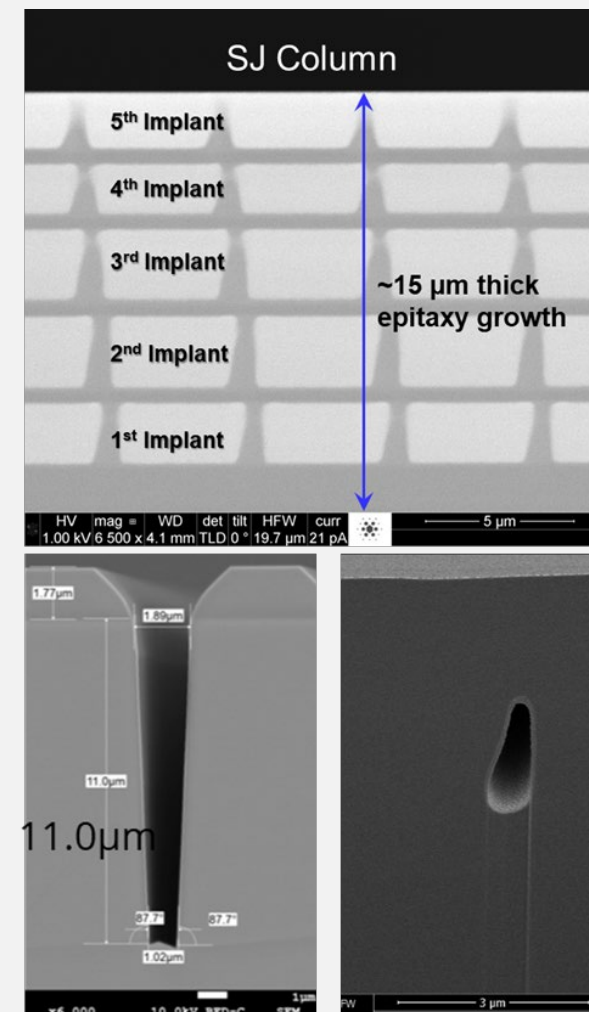


This SiC finFET, by Prof. Florin Udrea et al., ICSCRM 2024

300nm Pattern Pitch



Multi-Epi-Implant & Trench-fill Superjunctions



Summary

A*STAR has successfully established an 8” open innovation Silicon Carbide Pilot Line.

Key Features:

1. High speed, low defectivity, and highly uniform n-type SiC epitaxy. P-type coming soon.
2. Good quality MOS interface for both the planar and Trench gate MOSFETs.
3. 1200V class Planar gate MOSFET Platform technology.
4. 1200V Trench gate MOSFET Platform Technology with well rounded gate trench corners and very competitive ON function ($R_{on,sp}$ of $2.03 \text{ m}\Omega\cdot\text{cm}^2$ at a cell pitch of $6 \mu\text{m}$, leaving huge room for improvement through cell pitch reduction).
5. Process modules for FinFET (including CMOS like integration) and Superjunction MOSFET devices.
6. Wire bond and DBC free, 3-phase power module packaging technology with double side cooling.

*A*STAR is committed to advance SiC industry with a learning cycle time of 3 months!.*

“We invite you to collaborate with us”





**STRATEGIC.
BOLD.
TRUSTED.**



**Ready to innovate together and
explore new growth opportunities
with confidence?**

Connect with A*STAR IME

