

Designing Chiplets & 3DIC for Silicon Lifecycle Management

Yervant Zorian, Chief Technologist & Fellow, **Synopsys**

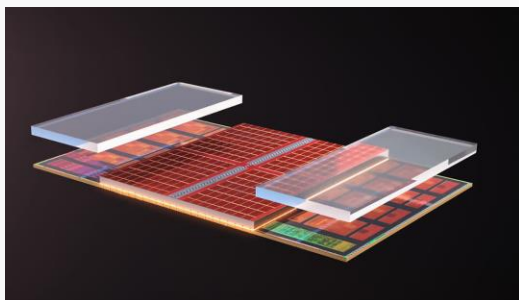
November 2025



Multi-Die Enabling Truly Transformative Products

Examples of commercial multi-die systems

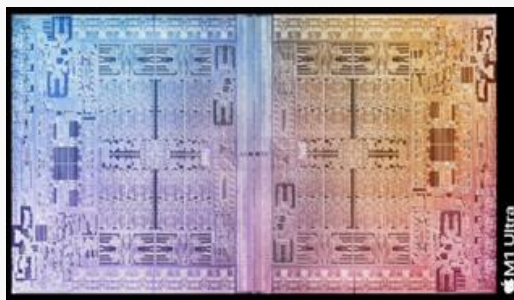
AMD



3D V-Cache: Hybrid Bonded

3x Energy Efficiency, 15x Interconnect Density (v. μ bumps)

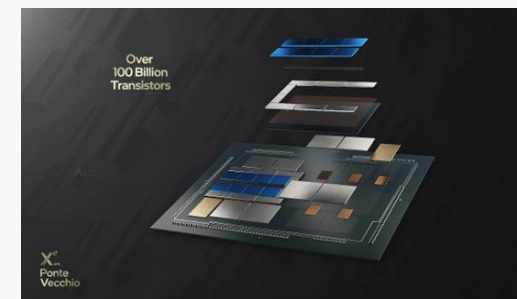
APPLE



Personal Computing

2x Dies, 114B Transistors, 2.5TB D2D BW, Silicon Connected

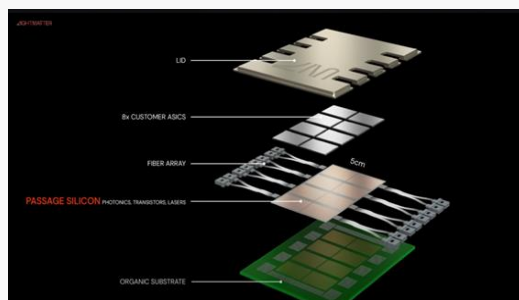
INTEL



Exascale Computing / AI

100B+ Tr's, 47 Active Tiles, 5 Process Nodes, EMIB/Foveros

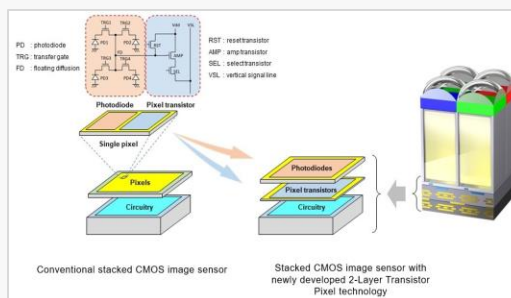
LIGHTMATTER



Photonics, Silicon, Lasers

8x Customer ASICs, Fiber Array

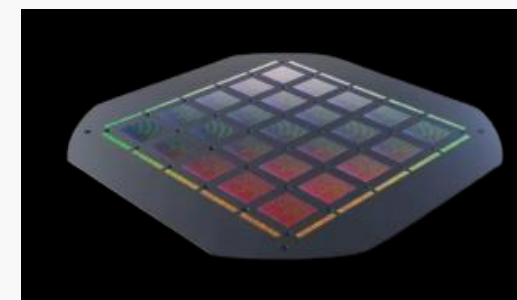
SONY



CIS with 2-layer Transistor Pixel Tech.

2x Electron Storage Capacity (Pix), Less noise, wide dynamic range

TESLA



9 Peta FLOPs AI-Training Tile

25x 50B Transistors, Reconstructed fanout wafer

The era of **PERVASIVE INTELLIGENCE**

Artificial Intelligence

Exponential productivity
and efficiency gains

But pushing the energy
and compute limits

Silicon Proliferation

More silicon content
everywhere

But productivity and
talent gaps

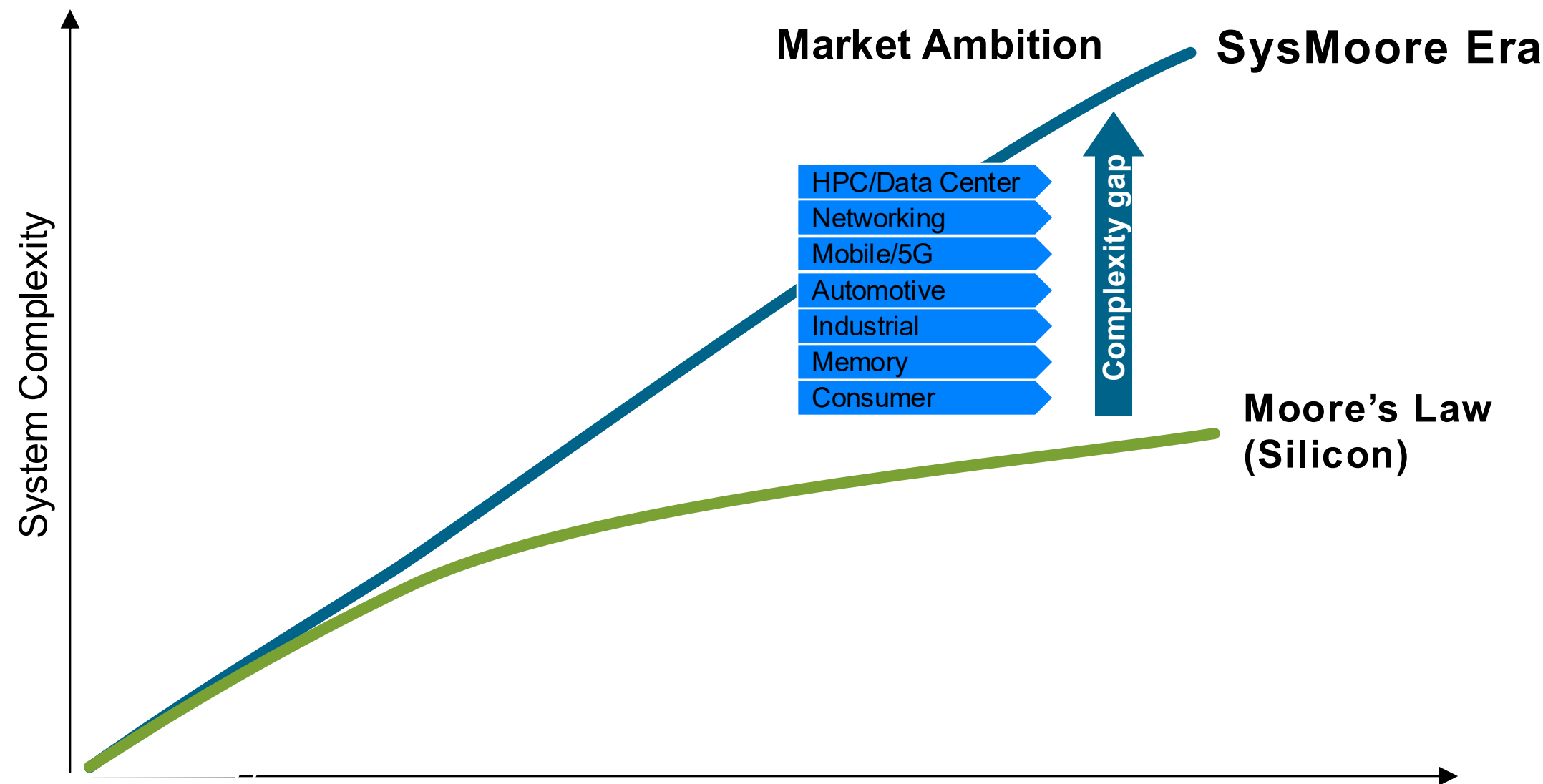
Software-Defined Systems

New applications,
new methodologies

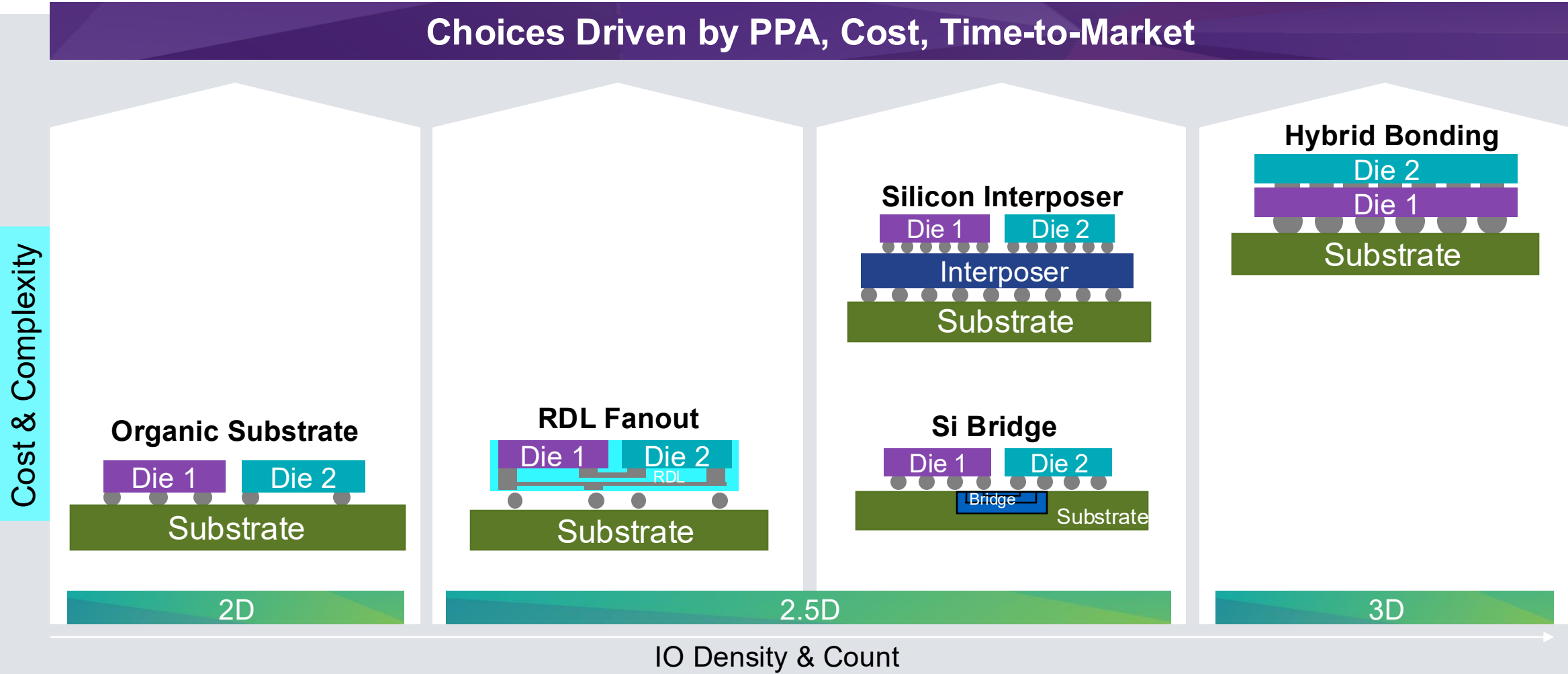
But increased complexity,
enablement of

Silicon to Systems Design Solutions

Multi-Die: Moving Beyond Moore's Law

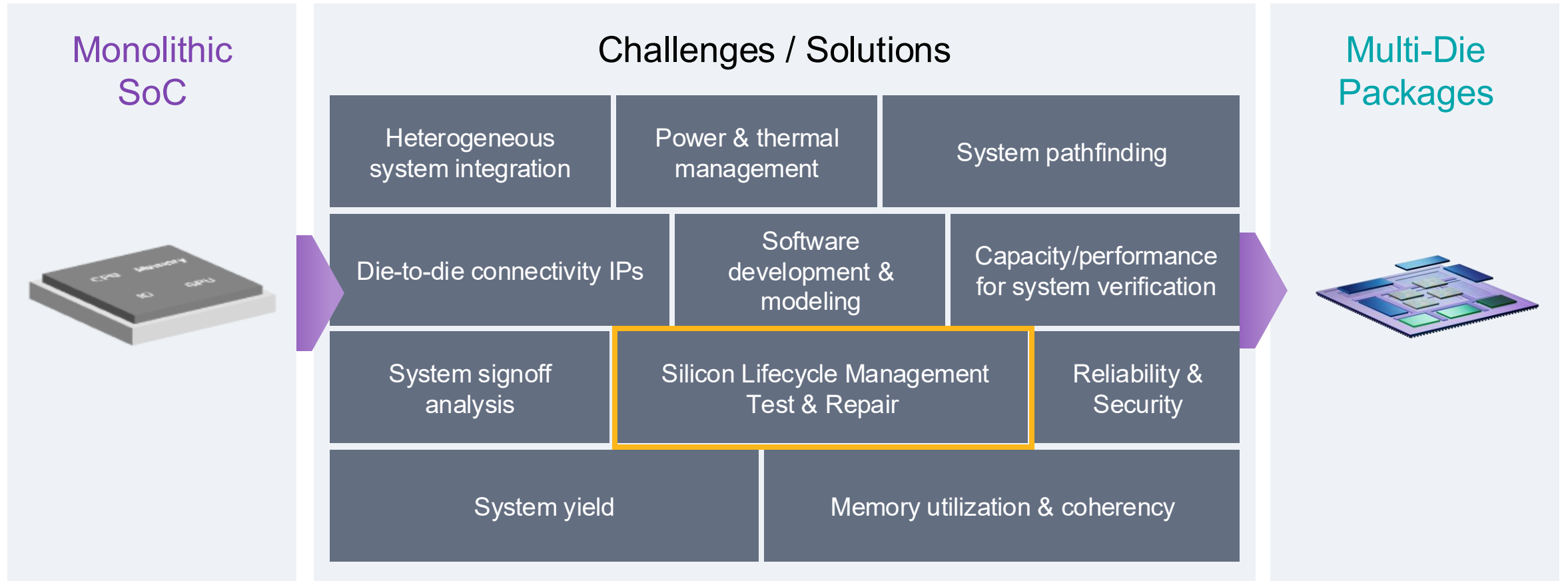


Multi-Die Systems Enabled by Packaging Advances

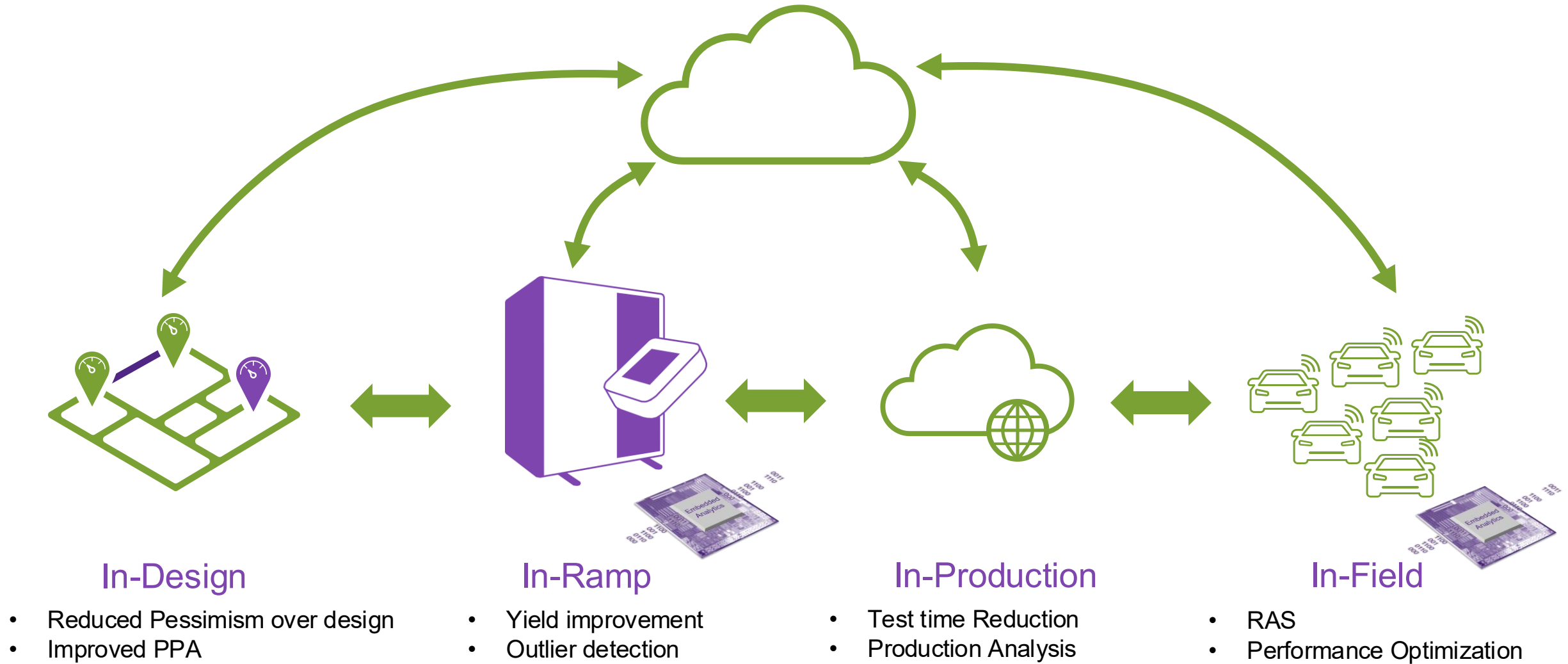


Synopsys Multi-Die Design Paradigm

Transformation from monolithic SoC to multi-die packages

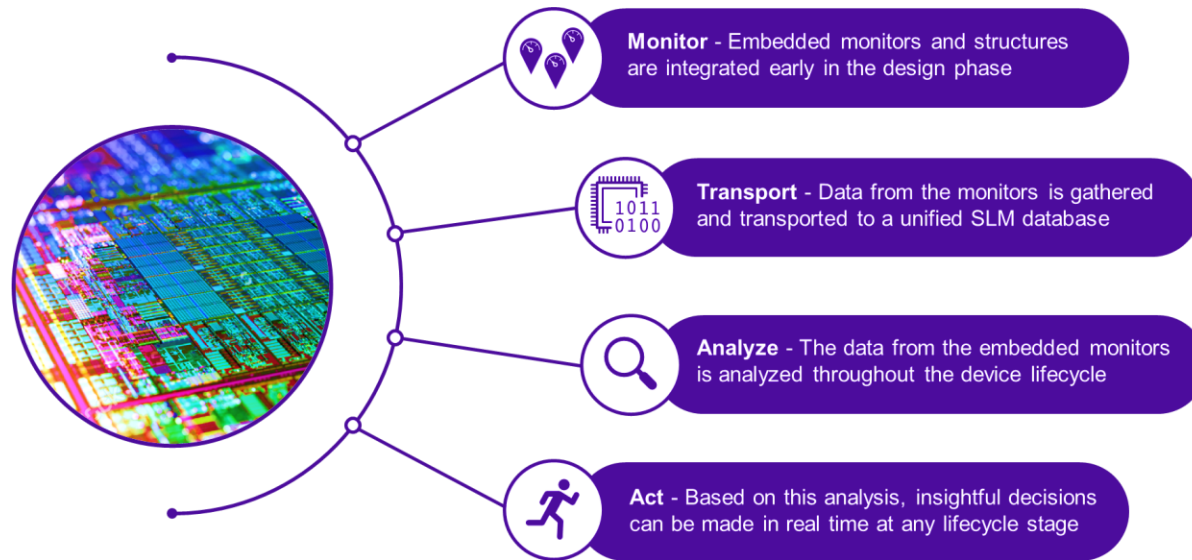


Silicon Lifecycle Management (SLM)



Health Monitoring | Lower DPPM | Reduced Costs | Failure Prevention

Silicon Lifecycle Management: Monitor, Collect, Analyze & Act

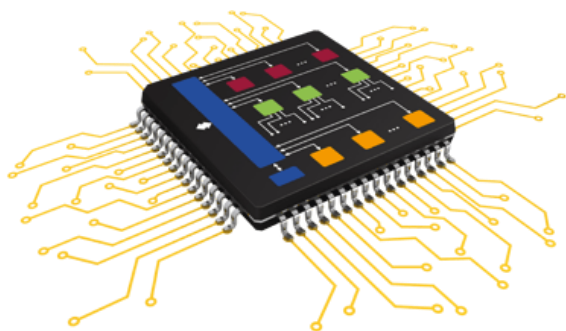


Silicon Lifecycle Management IP enables capabilities to

- 1) Monitor the health of the part
- 2) Detect symptoms of a degrading fault
- 3) Predict an SDC error before it occurs and
- 4) Take the necessary corrective action to improve availability

SLM IP Categories

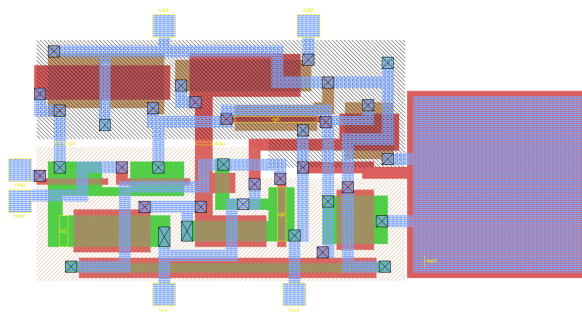
Environmental



Process Detector
Voltage Monitor
Temperature Sensor
PVTc

D2D (MTR, LTR, EXTRAM)

Structural

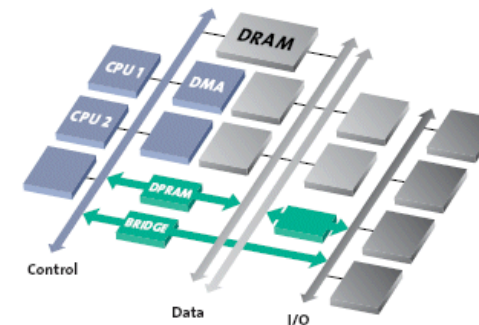


SMS Family,
LBIST, XLBIST, HSAT,
PMM (Path Margin Monitor)
CDM (Clock & Delay Monitor)

NOC: SHS
(SLM Hierarchical Subsystem)



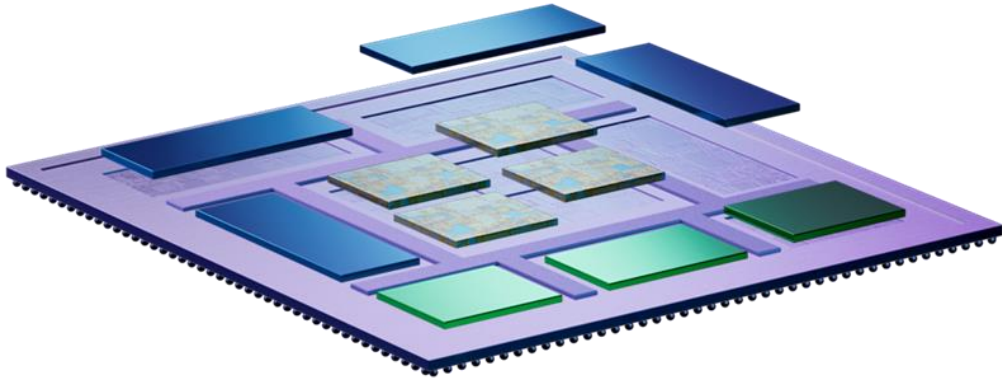
Functional



Signal Integrity Monitor
STAR ECC

FuSa / Security / RAS

SLM Challenges for Multi-Die Systems



❖ **Chiplets** (wafer sort, pre-bond stages)

- Test Access: probing dedicated/shared test port
- Quality/Yield: SLM for Known Good Die
- Performance/Power Optimization with SLM

❖ **Interconnects** (mid/post-bond stages)

- Die-to-die algorithmic test & incremental repair
- In-field signal integrity monitoring, self-test, repair

❖ **Multi-die System** (post-bond stage)

- System Level Test: stack/package test management
 - Reliability: in-field SLM - degradation monitoring
- Availability: in-field reconfiguration & repair
- Serviceability: remote debug & diagnosis

Synopsys SLM Solutions for Multi-Die Designs

IEEE 1838

- DFT access architecture
- **Individual dies and D2D interconnects test**
- Integration with on-chip hierarchical management (SHS)

UCIe MTR

Monitoring, Test, Repair

- MTR supports **logic-to-logic** PHY standard: UCIe (or HBI/AIB)
- **At-speed inter-die lane BIST and signal integrity monitoring (SIM) & repair of interconnects**
- Multi-die level MTR & calibration

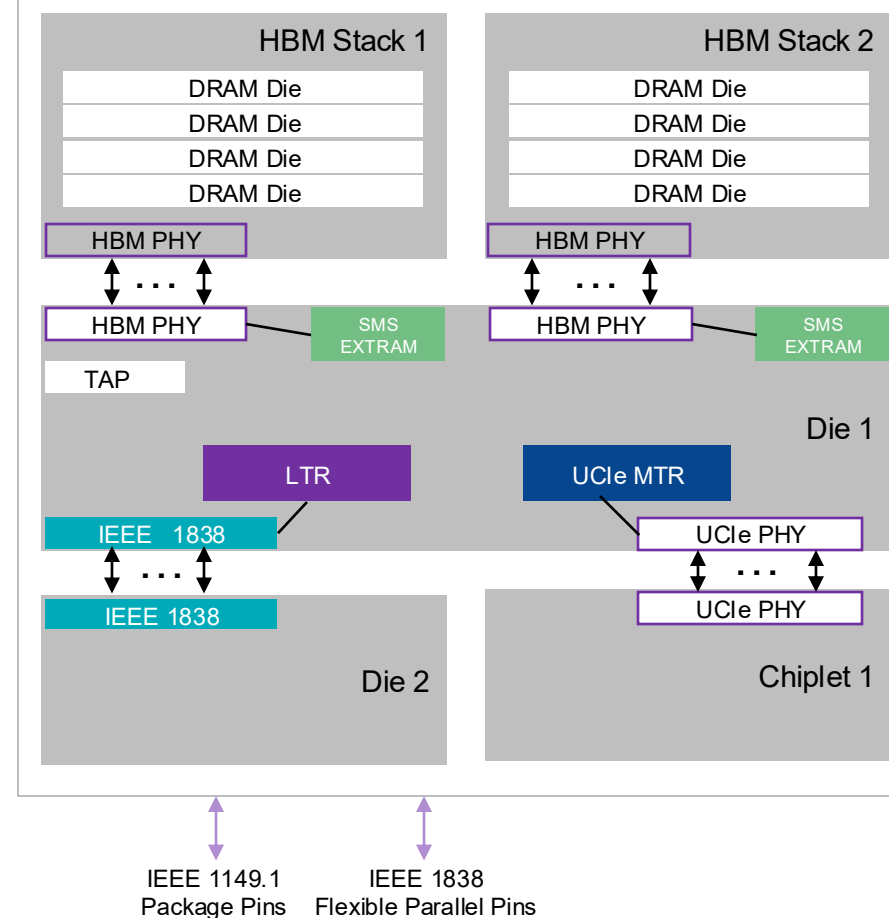
SMS EXTRAM

- Supports **logic-to-memory** PHY standards (HBM, DDR)
- **At-speed interconnect monitoring, test, and repair**
- Programmable at-speed External DRAM test
- System level repair, calibration

Lane Test & Repair (LTR)

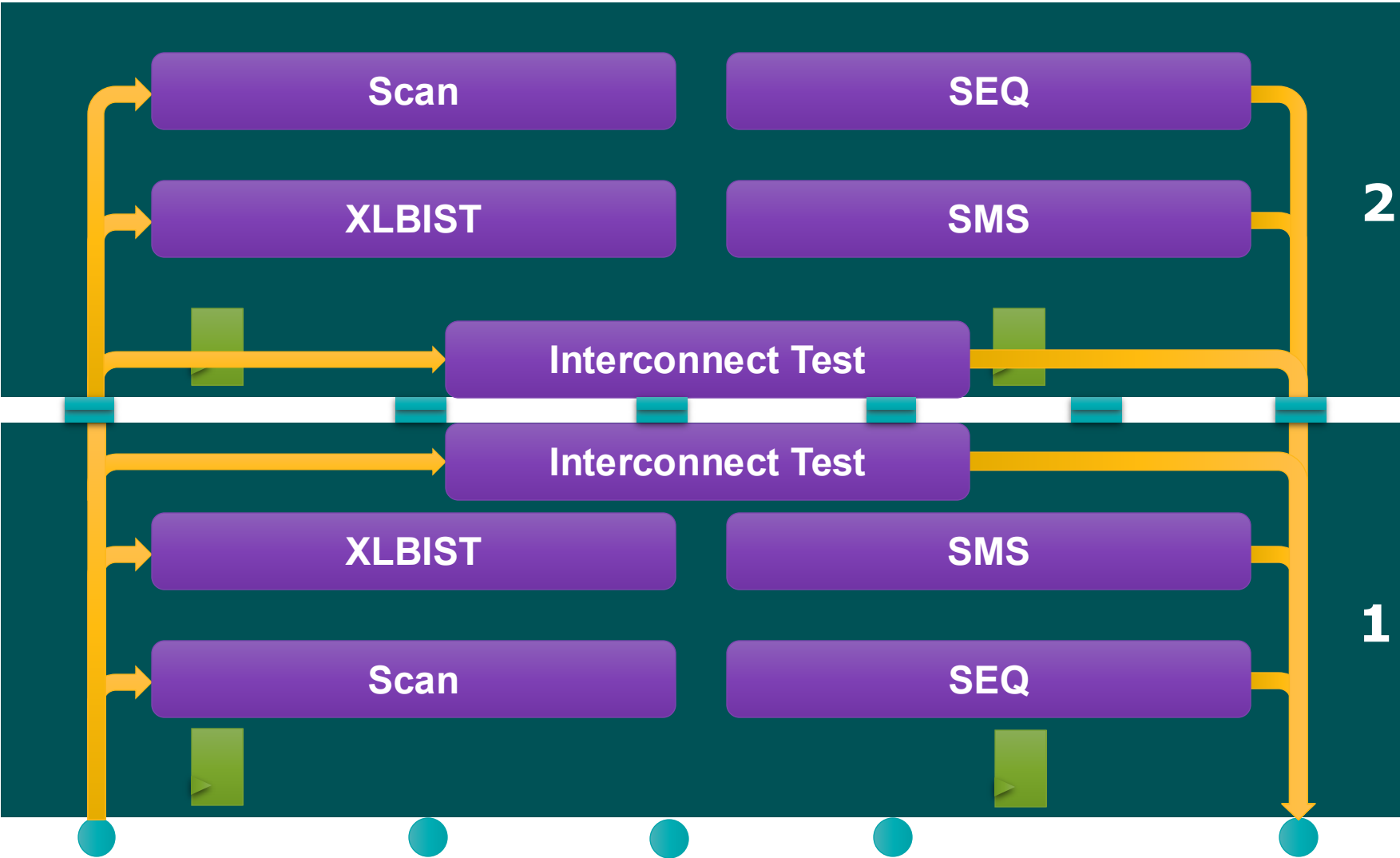
- Provides system level Built-In Self-Test for D2D high-volume lanes
- Performs reconfiguration & repair using redundant lanes

Multi-Die System



IEEE 1838 DFT Access

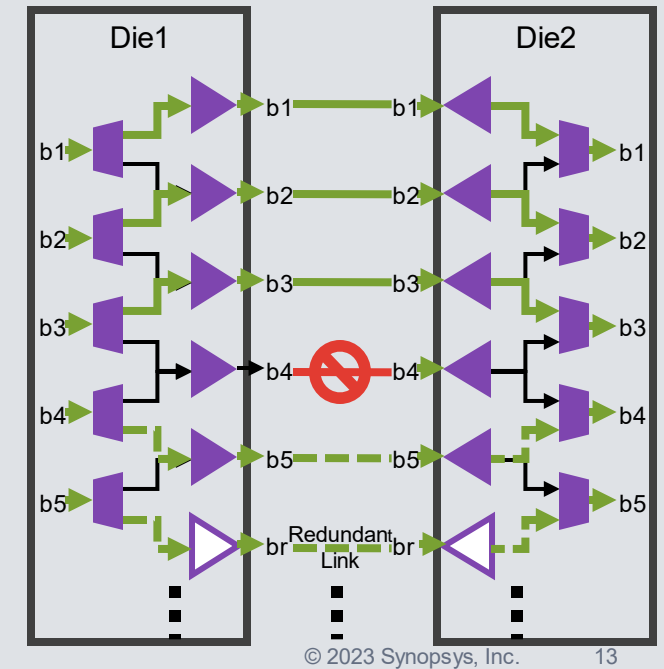
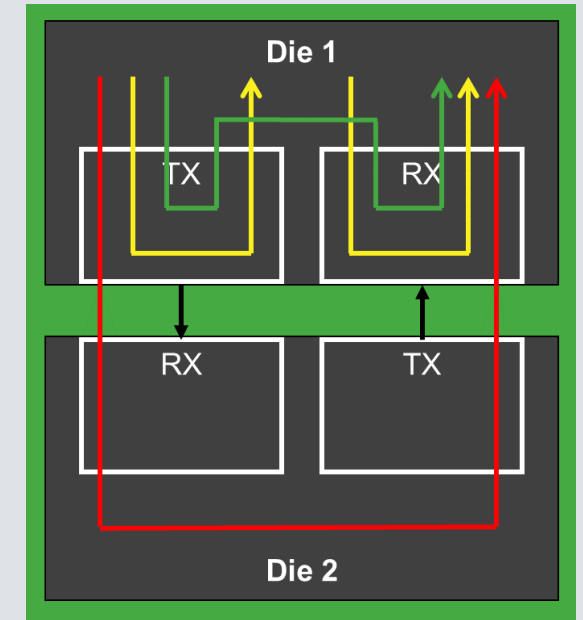
Functional (DFT) logic



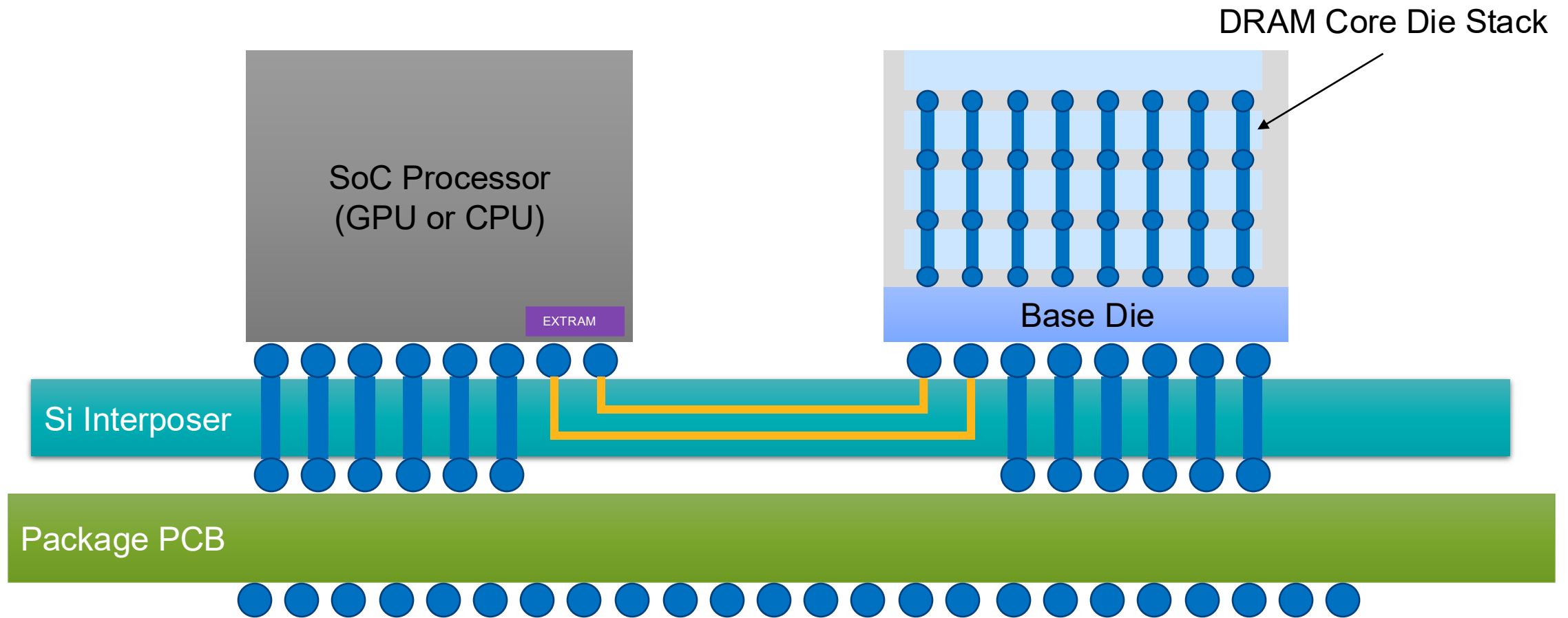
D2D Test

Lane Test and Repair, Loopbacks

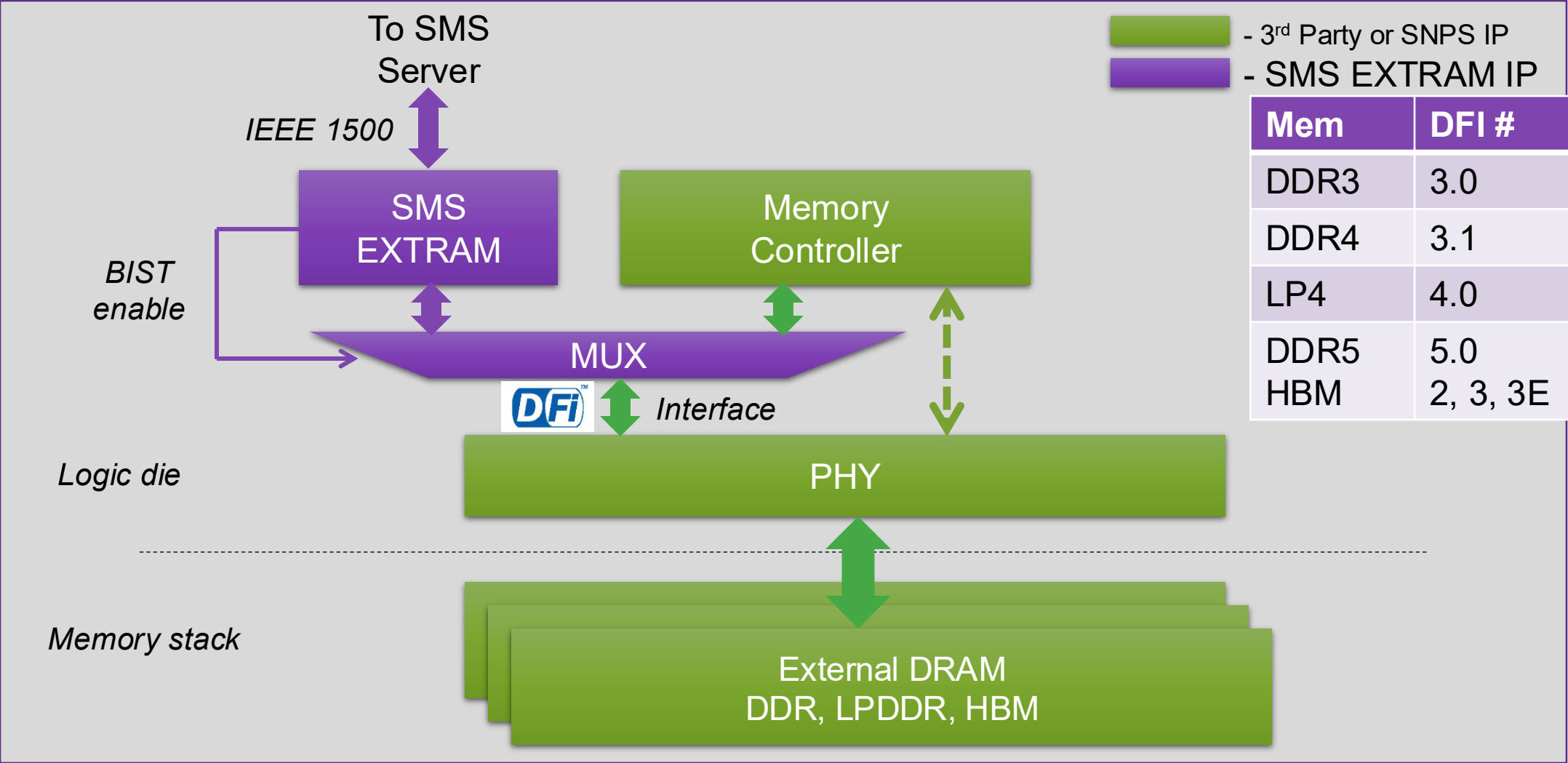
- Three levels of loopbacks
 - Internal TX and RX loopbacks (yellow)
 - Loops back pre-TX/RX, for each TX and RX
 - Near end loopback (green)
 - Shallow loopback between TX/RX on same die
 - Die-to-die loopback (red)
 - Loopback between die1 and die 2
- Lane Repair Method
 - Signal shifting between the faulty lane and spare lane (green)
 - The lane shift is implemented for both dies
 - Faulty lane output IO is placed into standby mode



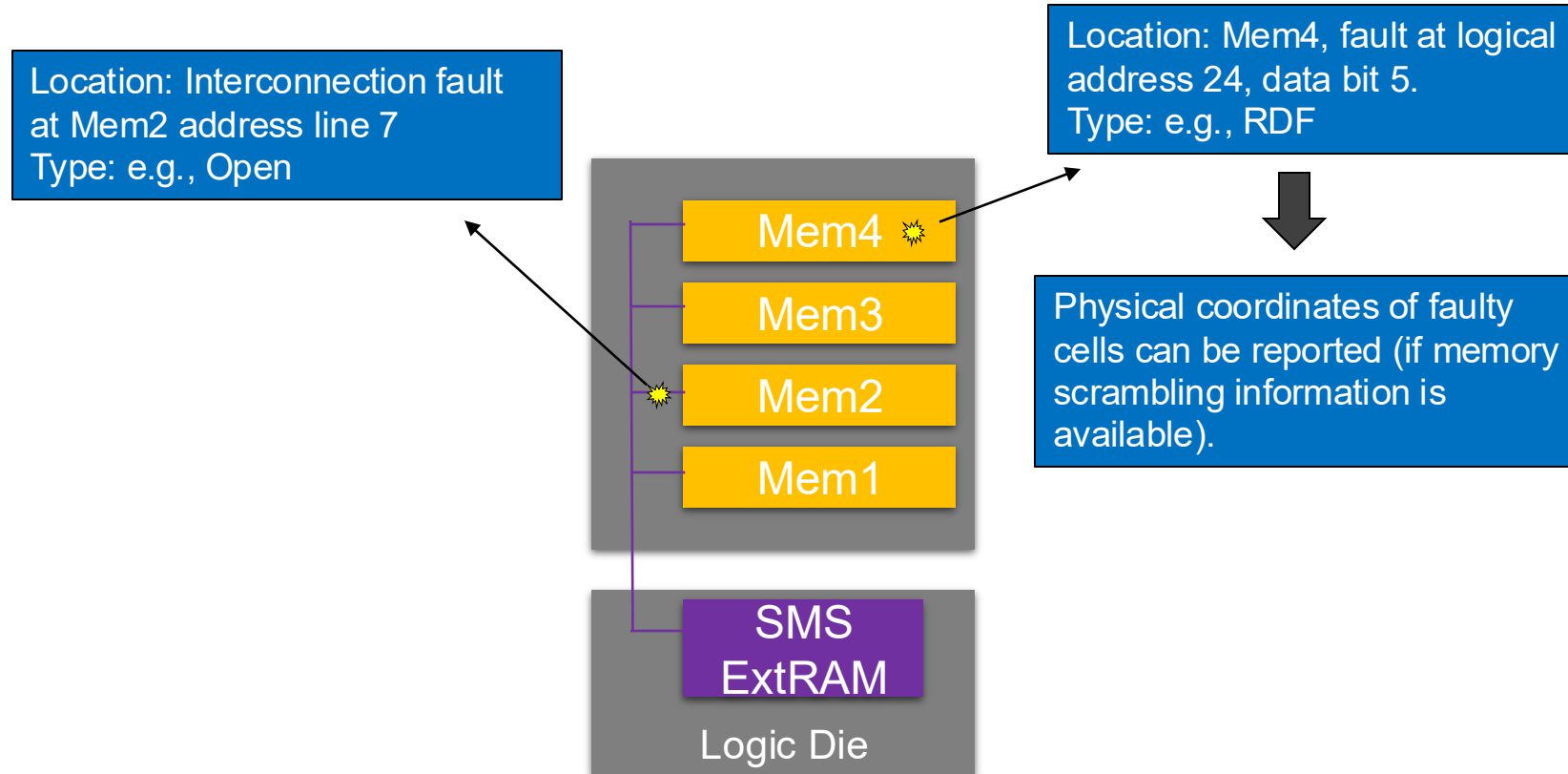
Traditional HBM Stack



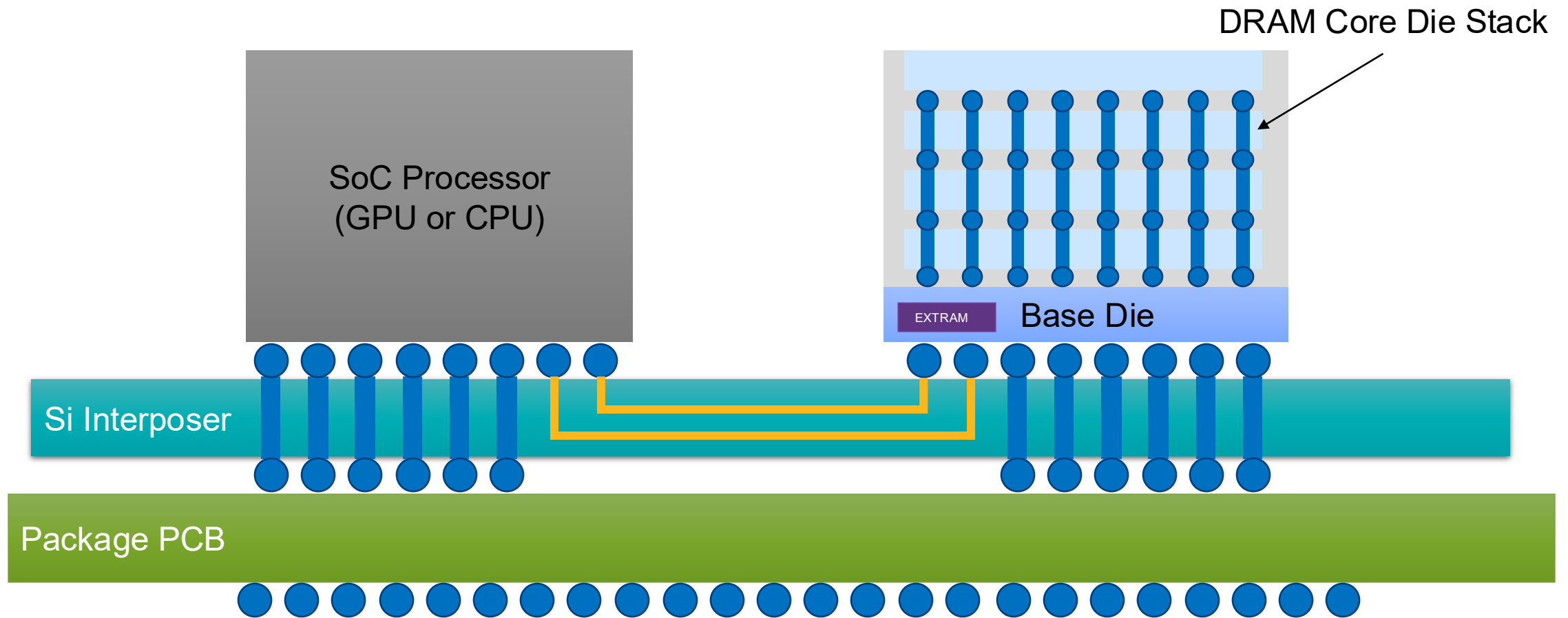
SLM EXTRAM Architecture (in Host Die)



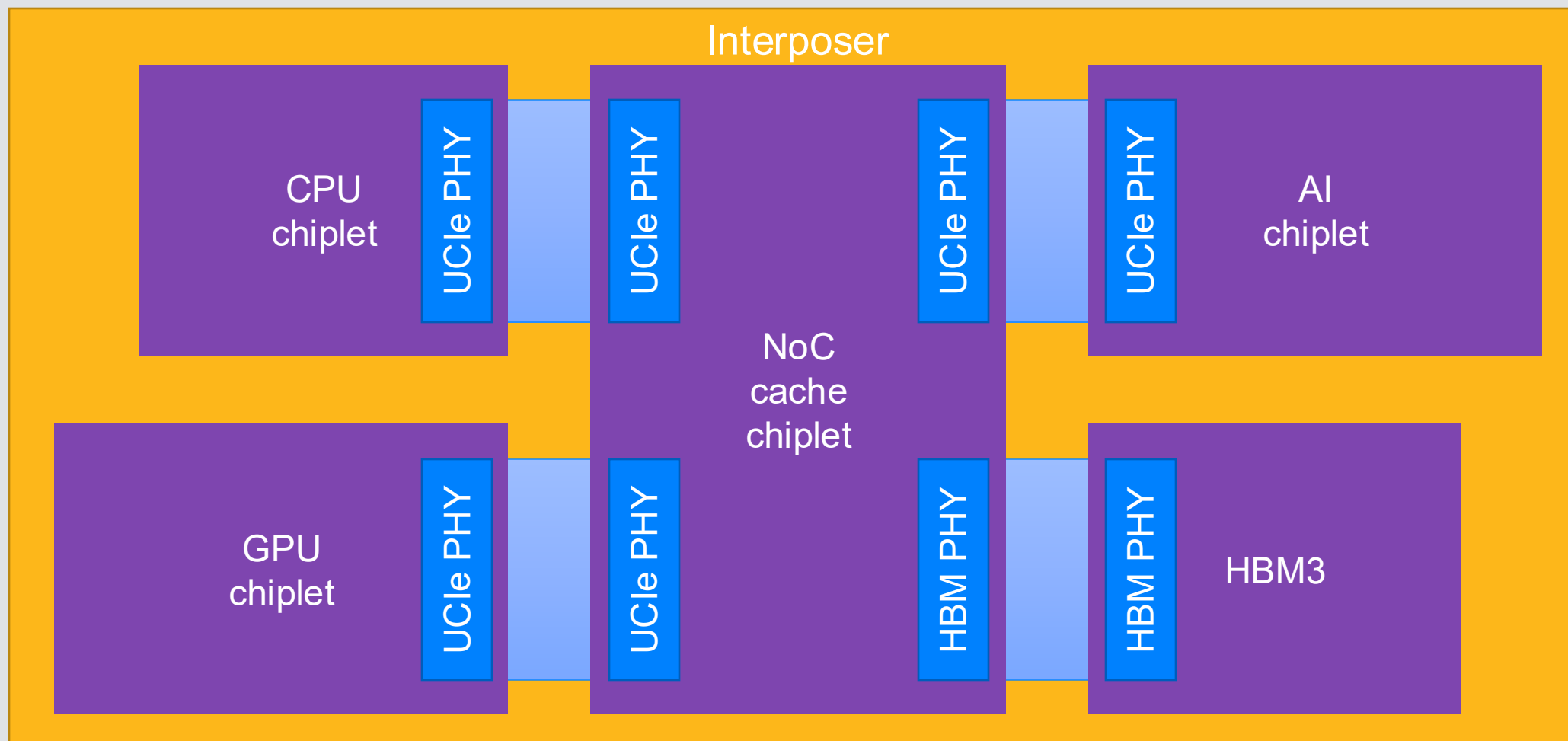
External Memory At-Speed Test & Diagnosis



Custom HBM Stack

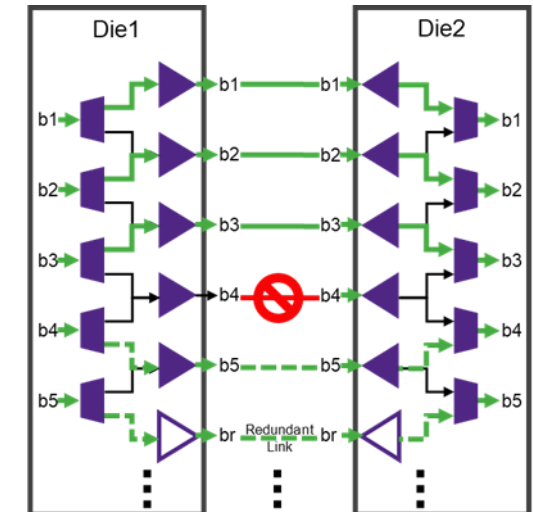


Example of a UCle-based Multi-Die Design



UCIe SLM Challenges

1. Bump pitch standard package 100-130um, Advance 25-55um
 - probing challenge for advanced packages
2. Interconnect SI and defect/fault coverage
 - LFSR-based loop back test challenges -> algorithmic
3. Lane redundancy & remapping (repair)
 - incremental multi-corner test in manufacturing and in-field aging/degradation challenge -> Cumulative



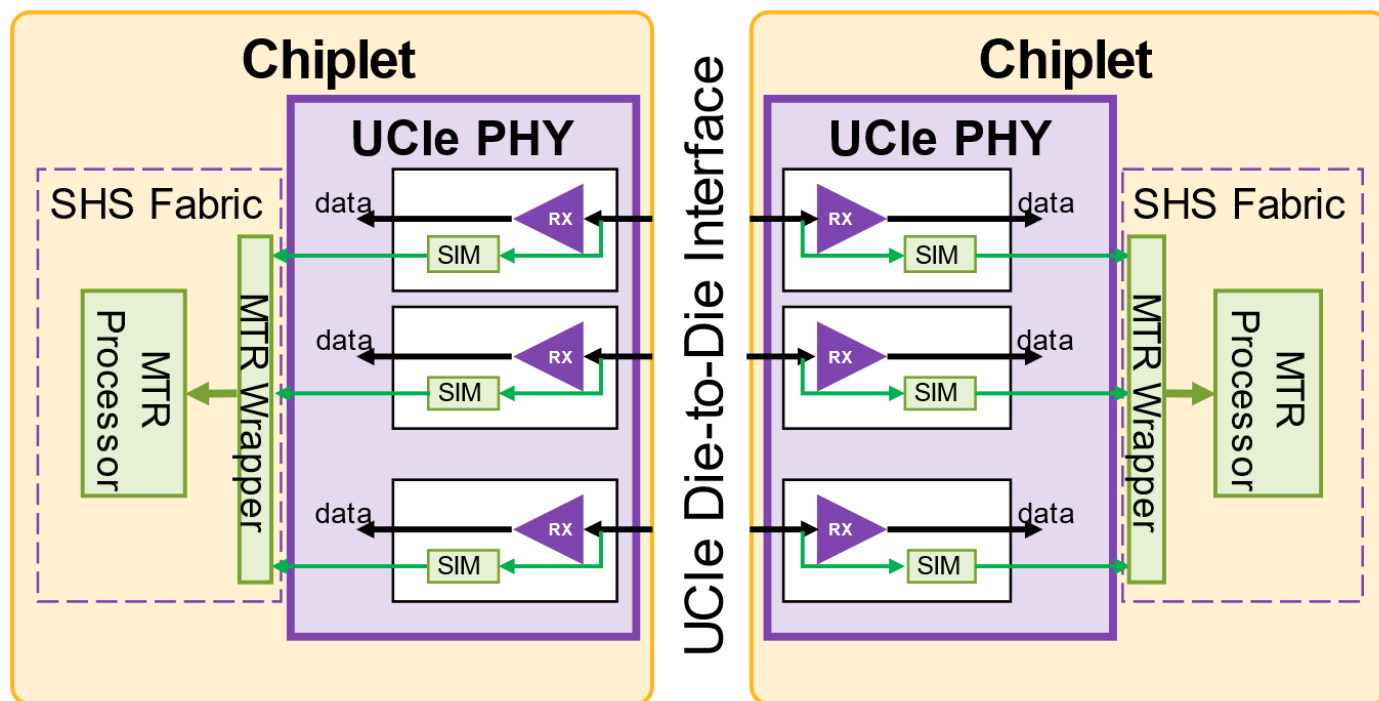
Advanced Package Configurations



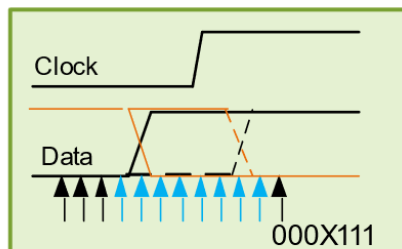
- 4SE

D2D Interface Failure Prediction & Repair

With Synopsys UCle and SLM Solution



Signal Integrity Monitor
Operation Concept



Targets High Reliability Applications

- Automotive ADAS
- Mission critical compute
- Life support

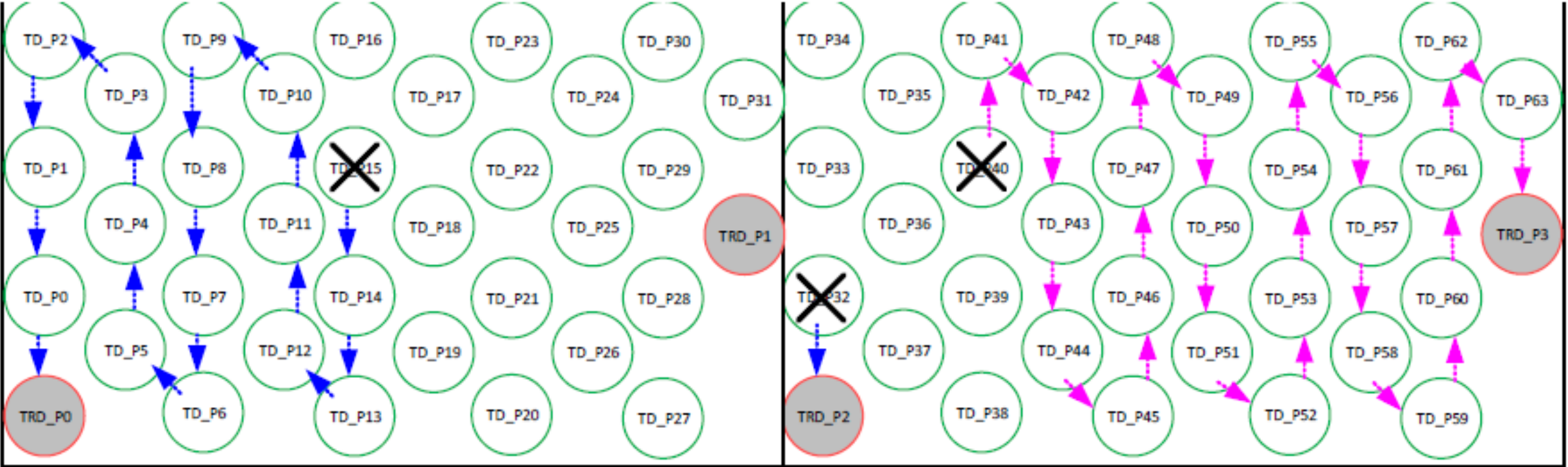
Avoids System Outage w/

- Per-lane health monitoring
- Lane Testing (algorithmic)
- Lane Repair (cumulative)

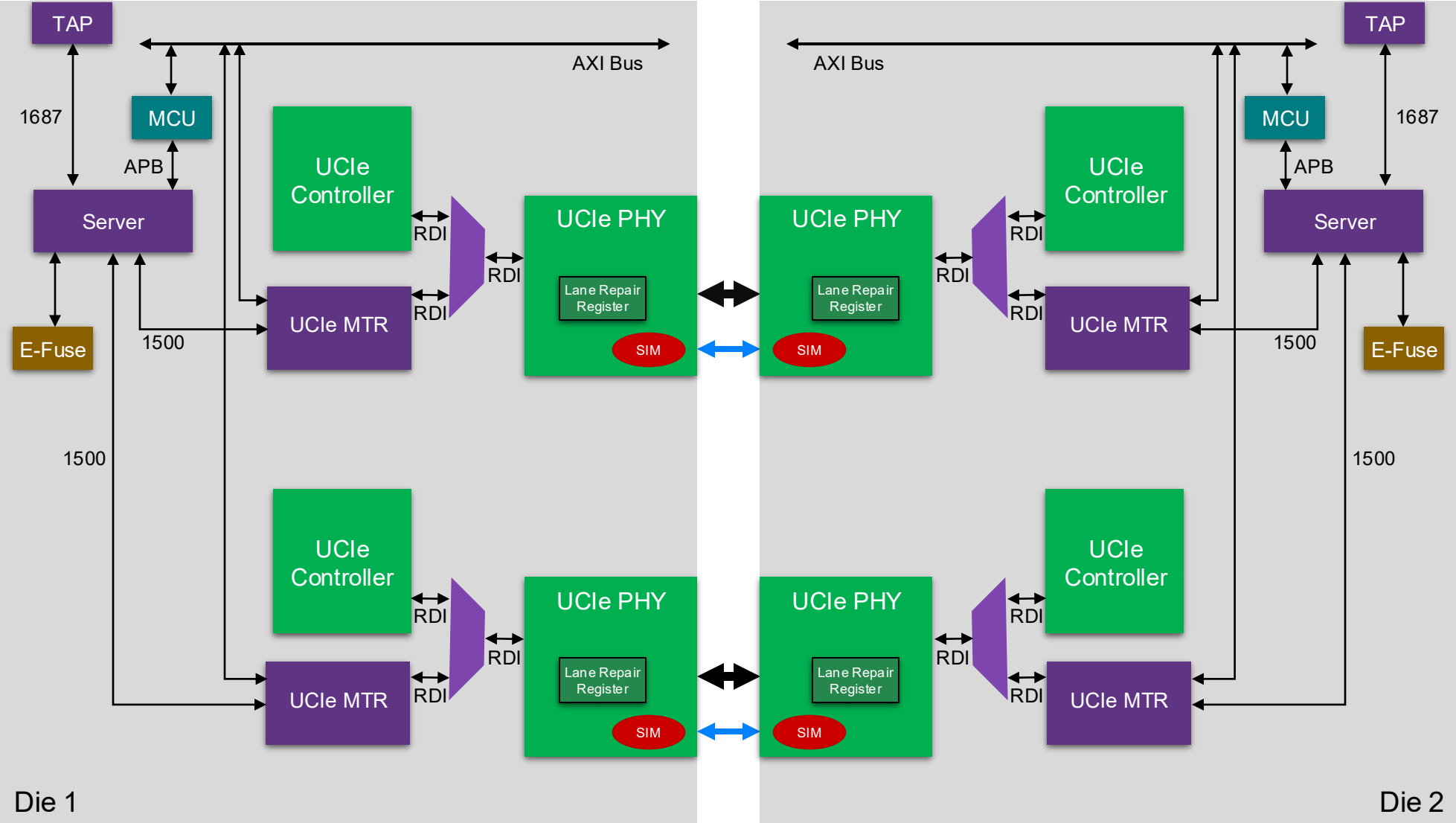
Synopsys Architecture w/

- Built-in SIM in UCle PHY
- Mission mode eye -diagram monitoring & repair
- Power-on Self-Test & Repair
- Embedded and cloud analytics for real time control & fleet statistic

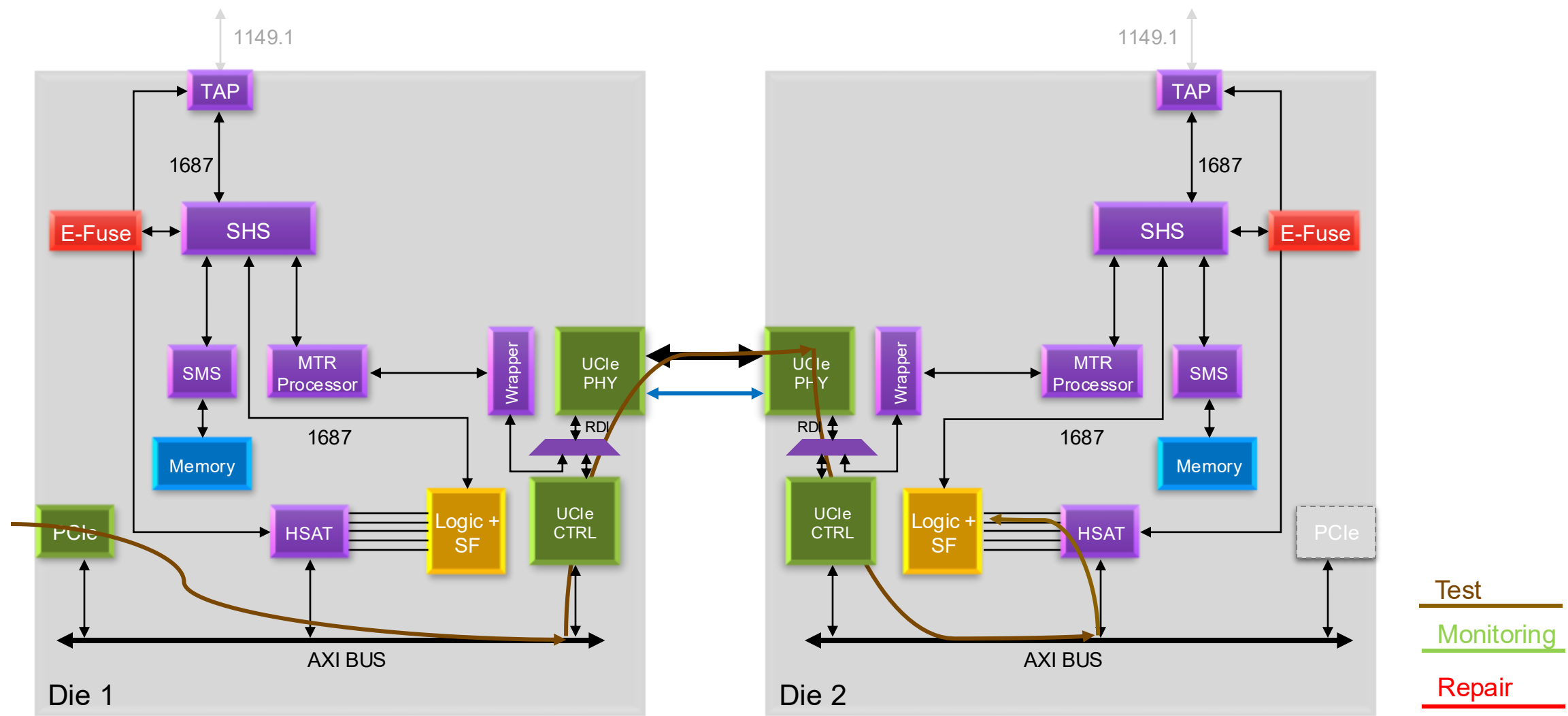
Data Lane Repair



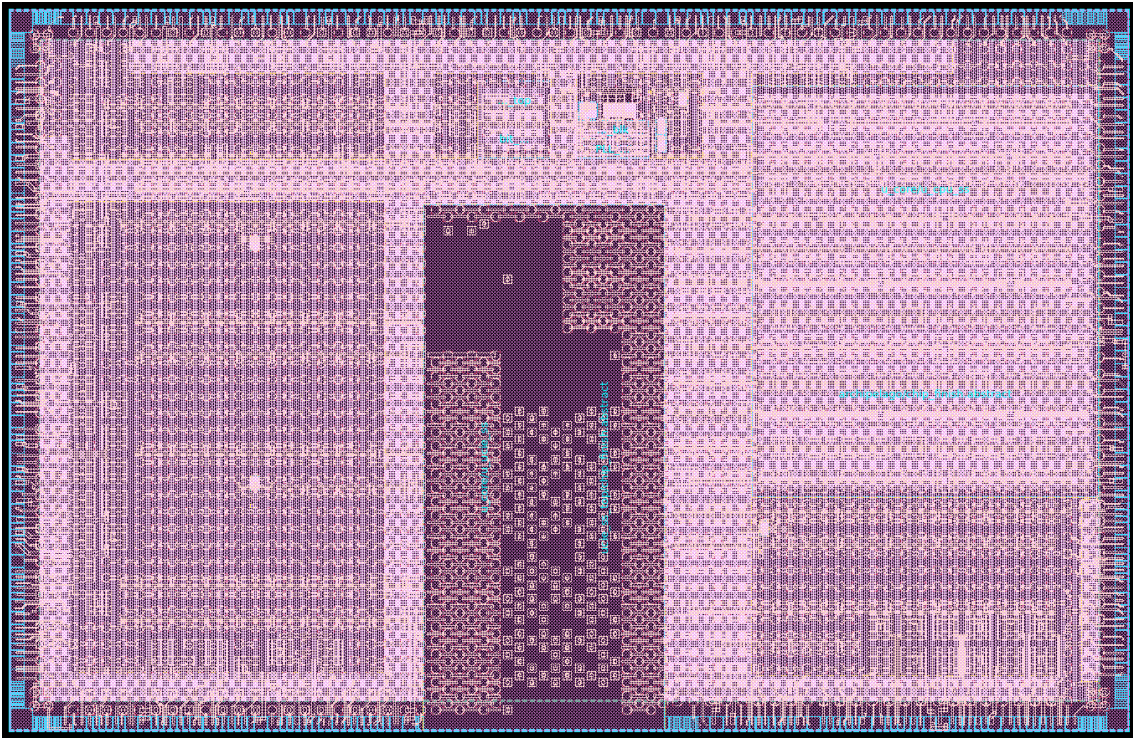
UCIe MTR Architecture with Embedded SI Monitors (SIM)



UCIe MTR & High-Speed Access & Test (HSAT) IPs for Multi-Die System Logic Test

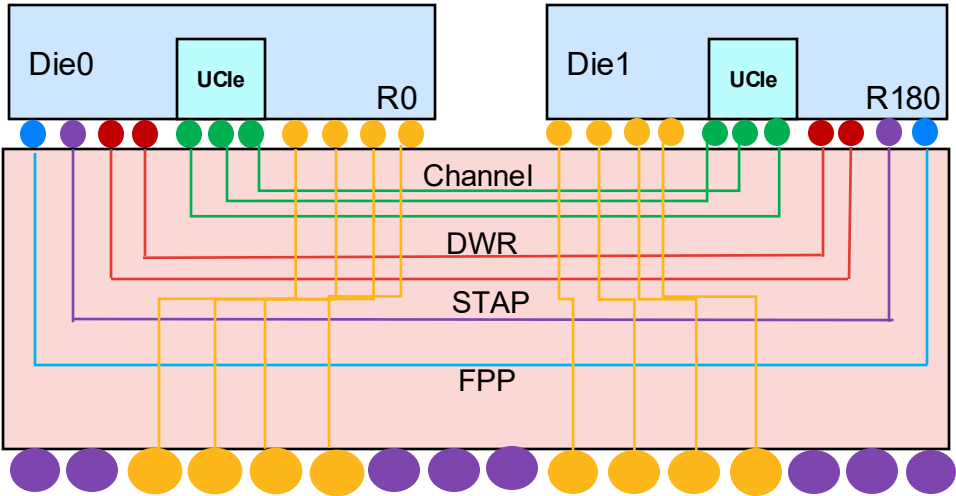


Chiplet Physical Design

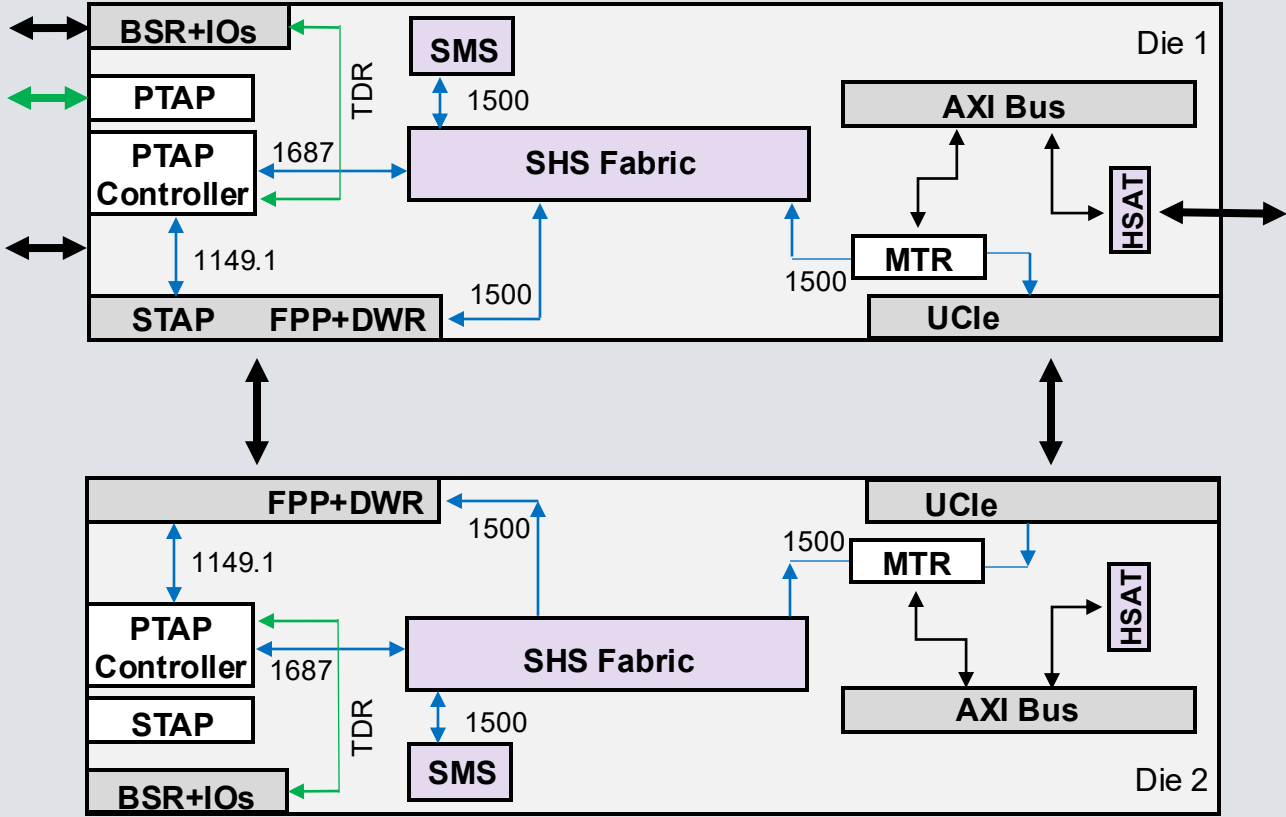
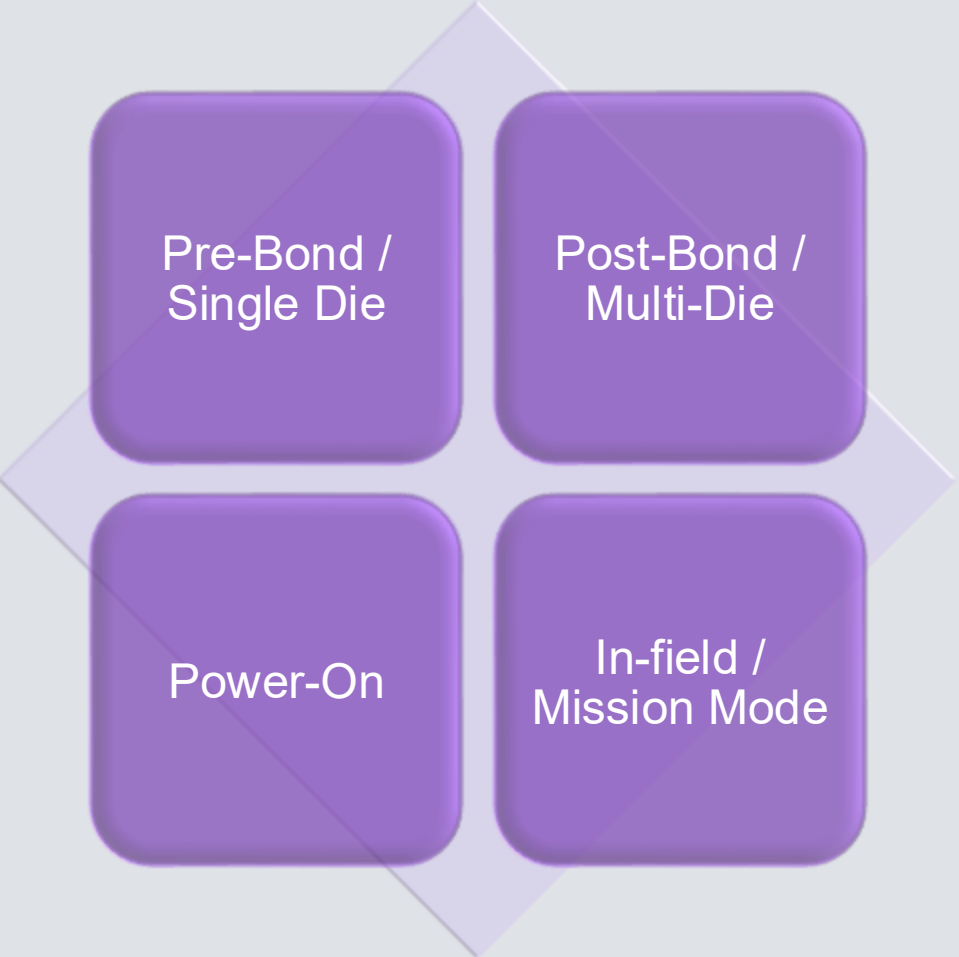


Design Details

Technology	N3P
# of Metals Used	15M+AP
Physical Die Size	4mm x 2.68mm
µBump Pitch	45µm (Post Shrink)

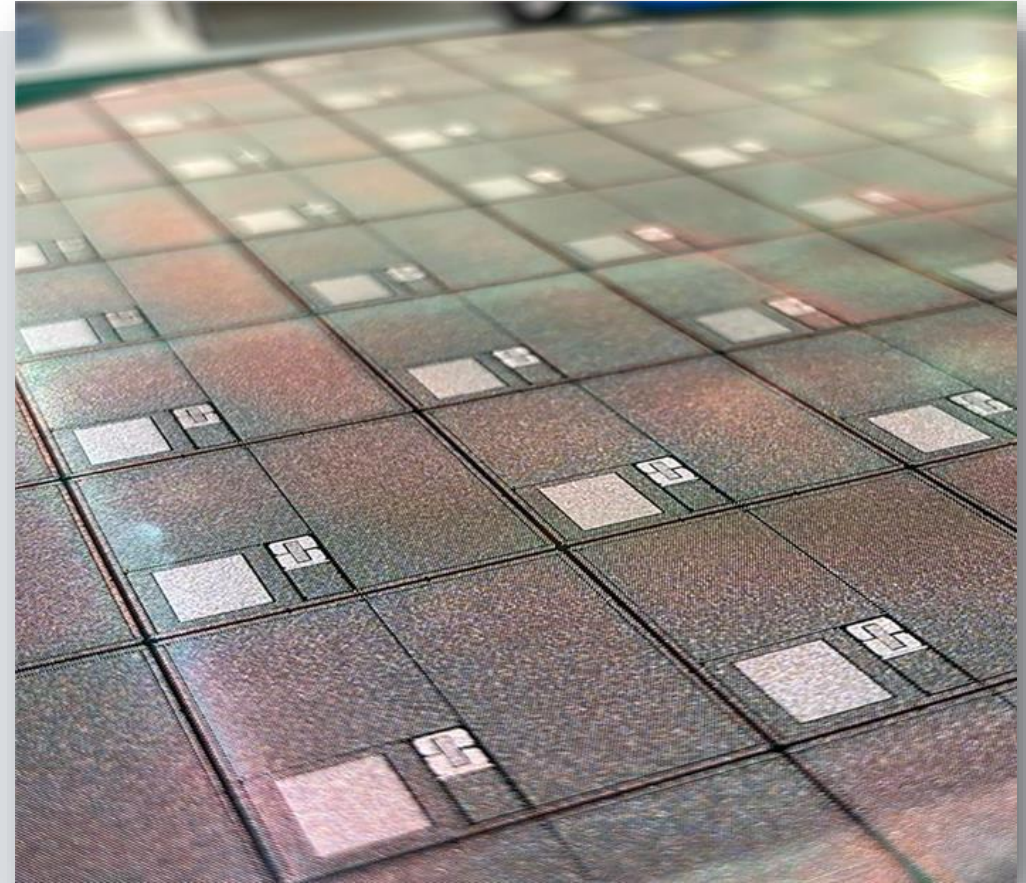


Multi-Die Demo Vehicle Monitoring Test, and Repair in Four Lifecycle Scenarios



Silicon Results High level Objectives

- Show leadership in Multi-Die IP and foundry collaboration in advanced packaging
- Develop Multi-Die reference flow for monitoring, test, debug & repair across silicon lifecycle, showcasing KGD/KGS
- Demonstrate silicon proof point for complete interconnect, logic & memory test, repair and monitoring:
 - N3P on CoWoS-S
 - UCle PHY with eSIM, MTR, HSAT, CDM
- Improve IPs and methodologies from pre/post silicon project execution learnings:
 - Readiness for multi-die bring-up
 - Multi-die DV environment
 - True Multi-die Solution with comprehensive learnings (timing/ICV/Interposer/SI/PI)



Thank You